Topologies, Losses, and Applications in Switched-Capacitor Converters

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by

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Abstract

Topologies, Losses, and Applications in Switched-Capacitor Converters

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Switched Capacitor Converters (SCC) are a family of DC-DC switched-mode power converters comprised of capacitors and switching networks; some include inductance for resonant operation. Features such as the absence of large magnetic components and efficient voltage conversion at lighter loads make this type of converter suitable for on-chip implementation. In addition, technological advances in capacitor and switch manufacture make SCC a suitable candidate for medium- and high-power applications. SCC have a basic deficiency, however: the inherent energy loss resulting from capacitor charging and discharging processes. This basic deficiency was analyzed and generic loss modeling methodology of SCC operated in open loop was developed and verified by simulation and experiment. The proposed approach is unified, covering both hard and soft switched SCC, capable of describing both conduction and switching SCC losses and compatible with switches of resistive behavior, such as MOSFETs and/or voltage drop behavior such as bi-polar transistors or diodes. An important feature of this model is that the losses are expressed as a function of the average currents through the capacitors. Since these currents are linearly proportional to the output current the final
expression is a function of simple parameter, the output current, rather than complicated voltage difference.

Accurate information regarding the system’s open-loop response is essential in the design of the system controller and closed-loop response. To this end, a behavioral circuit average model of SCC was developed. The proposed method is not only capable of successfully reconstructing an average behavior of SCC, but also, being an average circuit, it is transparent to the switching action of the circuit. The resulting behavioral average circuit can be analyzed by any network analysis method, or evaluated numerically with a numerical software package. An important attribute of the developed model is that it is generic and compatible with most hard switched SCC systems, either standing alone or as part of a larger, more complicated system. This attribute was evaluated with a hybrid converter, which combines a switched inductor Boost system cascaded with a switched capacitor 1:3 multiplier. The theoretical predictions of the model were compared with numerical simulations in PSIM and laboratory experiments in various operation modes such as CCM and DCM of switched inductor part and different capacitor charging profiles of SCC.

The model developed in this work can be used to assess the effect of the operational conditions of SCC, such as switching frequency and duty cycle, on the expected losses and large and/or small-signal response. That being so, the model can help in the optimization of SCC systems and their control to achieve high efficiency, proper dynamic response and the desired regulations.

**Keywords:** Switched capacitor converter, power converter, DC-DC converters, modeling, average model, dynamic, static, analysis, conduction losses, switching losses, SCC, soft switching, resonant converter, small-signal, large-signal, hybrid converter.
Dedicated to my beloved mother,
Anna.
Her love, support, and guidance
sustain me every day.

Посвящается моей любимой Мамочке,
Анне Лазаревне.
Её любовь, поддержка, и наставления
помогают в течение всей моей жизни.
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Many thanks

Michael Evzelman
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<tr>
<td>AC</td>
<td>Alternating Current</td>
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<tr>
<td>CC</td>
<td>Complete Charge</td>
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<tr>
<td>CCM</td>
<td>Continuous Conduction Mode</td>
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<tr>
<td>CCM-NC</td>
<td>Continuous Conduction Mode and No Charge</td>
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<tr>
<td>DC</td>
<td>Direct Current</td>
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<td>DCM</td>
<td>Discontinuous Conduction Mode</td>
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<tr>
<td>DCM-CC</td>
<td>Discontinuous Conduction Mode and Complete Charge</td>
</tr>
<tr>
<td>EEPROM</td>
<td>Electrically Erasable Programmable Read-Only Memory</td>
</tr>
<tr>
<td>EQSCC</td>
<td>Equalizing Switched Capacitor Converter</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
</tr>
<tr>
<td>FSL</td>
<td>Fast Switching Limit</td>
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<td>GSIM</td>
<td>Generic Switched Inductor Model</td>
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<tr>
<td>HV</td>
<td>High Voltage</td>
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<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>KCL</td>
<td>Kirchhoff’s Current Law</td>
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<tr>
<td>MOSFET</td>
<td>Metal-Oxide-Semiconductor Field-Effect Transistor</td>
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<tr>
<td>MPP</td>
<td>Maximum Power Point</td>
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<tr>
<td>MPPT</td>
<td>Maximum Power Point Tracking</td>
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<td>NC</td>
<td>No Charge</td>
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<td>PC</td>
<td>Partial Charge</td>
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<tr>
<td>Abbreviation</td>
<td>Full Form</td>
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<tr>
<td>PV</td>
<td>Photo Voltaic</td>
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<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>RMS</td>
<td>Root Mean Square</td>
</tr>
<tr>
<td>SC</td>
<td>Switched Capacitor</td>
</tr>
<tr>
<td>SCC</td>
<td>Switched Capacitor Converters (refers to both singular and plural)</td>
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<tr>
<td>SMPS</td>
<td>Switched Mode Power Supplies</td>
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<tr>
<td>SSL</td>
<td>Slow Switching Limit</td>
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<tr>
<td>TI</td>
<td>Texas Instruments</td>
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<tr>
<td>VLSI</td>
<td>Very Large Scale Integration</td>
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<td>ZCS</td>
<td>Zero Current Switching</td>
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<td>ZVS</td>
<td>Zero Voltage Switching</td>
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Chapter 1  Introduction

1.1. Switched Capacitor Converters (SCC)

Switched capacitor converters (henceforth referred to as SCC for plural and singular) are a family of switched mode power supplies. A distinctive property of SCC is the use of capacitors as a main energy transfer component as opposed to switched inductor converters that use inductors. Several attributes favor the SCC in some power conversion applications over their inductor-based counterparts. For example, SCC excel in efficient electricity conversion from one voltage to another at light loads. Additionally SCC are integration-friendly systems because of the inductor absence. Integration of power inductors on chip still pose severe technological challenge. It is worth mentioning that modern capacitors have higher power and energy densities than their inductor counterparts.

Historically SCC have evolved from simple voltage multipliers that were used for supplying high voltage pulses to the load [1]. The first capacitor-based continuous converters began to appear in the 1970s [2]. Over time, with the evolution of microelectronics, capacitor-based converters were used to boost on-chip low voltages for reprogrammable memory applications such as EEPROM [3] and later Flash memory [4-6], and are known by the name “Charge Pump” [7]. Nonetheless, there were a few other applications for charge pumps such as generation of the voltages required by the RS232 standard [8]. The motivation for choosing charge pumps over the inductor-based converters was mainly because charge pumps are miniaturization-friendly, relatively simple systems comprised of capacitors, diodes, and two phase-shifted clocks. The output of these systems is generally unregulated, with some fixed voltage gain, making them easy to implement and relatively failsafe. Alternative, more complicated applications, such as high-power or regulated converters, were considered of theoretical value only.

Over the past few decades, technological improvements to switches and capacitors as well as the evolution of the charge pumps has introduced a new family of power converters, the SCC. This family includes much more sophisticated converters with regulation capabilities which process higher power levels. Discrete commercial devices have begun to appear, such as TI’s TPS60311 and previously owned by National (lately acquired by TI) LM3352. These devices have several conversion ratios, external flying capacitors, and high efficiency at predefined operation conditions. Previously, these characteristics were the sole territory of switched inductor converters.

With the expansion of SCC systems into higher-power applications, resonant technology was adopted
Similarly to the switched inductor converters, the aim of resonant technology is to reduce the switching losses, i.e. perform zero current switching (ZCS). Although introducing inductors into SCC could be seen as canceling out some of the above-mentioned advantages, it should be pointed out that the main energy transfer component is still a capacitor, whereas the inductor is required for resonance only. In many cases, this inductor is so small that the parasitic inductance of the component connections is sufficient.

1.2. CONSTRUCTION OF SCC TOPOLOGIES

SCC in its basic form is a DC to DC power converter that consists of capacitors and switches [12]. Some SCC families also include an inductive element for resonant operation [9, 10]. The converter can be unidirectional or bidirectional and can have any number of inputs, outputs or both [13]. The basic SCC cell is shown in Fig. 1.1a. It has a “flying,” or switched, capacitor, and a network of switches that connects the capacitor to the ports of the SCC and/or other capacitors. The name, flying, reflects the nature of the capacitor, which is connected to different ports during the SCC operation. Subsequently its common mode to ground voltage can change during the operation, as in the case of the doubler converter in Fig. 1.1b.

A full SCC system can be built around a single SCC cell, or can contain a large number of cells interconnected depending on the purpose of the converter: step-up, step-down, inverting, etc. Moreover the converter can be based on a number of sub-converters connected in series or in parallel, or a combination of the two [14]. Parallel, or interleaved, structures have an advantage in reducing the ripple of input/output port of the converter, and the disadvantage is the larger number of components and the requirement for a more advanced controller. Some more advanced converters have sophisticated switch networks, which allow more than a single conversion ratio with the same SCC stage. An example of such a system is an SCC with binary or Fibonacci resolution, built around three basic SCC cells, as in Fig. 1.2 [15-18]. This converter is capable of achieving eight different conversion ratios for binary and 13 for Fibonacci resolution.

Fig. 1.1: (a) Basic SCC cell, (b) Doubling SCC - Doubler.
The conversion ratio in SCC is set by controlling the switch network. The network connects the capacitors in predefined structures to other capacitors, the input, and output ports. Each predefined structure creates a capacitor charging/discharging path known as a sub-circuit. These structures or sub-circuits are each activated for a time interval, which is named the switching phase. Switching phases are changed periodically, transferring the charge. Proper converter operation requires that each flying capacitor will participate in at least two switching phases, charging and discharging; that requirement ensures charge balance across the capacitors.

1.3. SCC BASIC PRINCIPLES OF OPERATION

Ideally, lossless SCC will charge its capacitors to the voltage of the charging source, and discharge into the load maintaining the same voltage. Ideal DC voltage transfer ratio of SCC is relatively simple to calculate following the connection of the flying capacitors in the SCC. For the doubler example of Fig. 1.1b the converter is operated in two phases. First, the switches $S_{1a}$ and $S_{1b}$ are conducting and the capacitor, $C$, will charge to $V_{in}$. Then $S_{1a}$ and $S_{1b}$ are turned off, and $S_{2a}$ and $S_{2b}$ are turned on, which connects the capacitor in series to $V_{in}$ and discharge to $V_o$. Consequently the output will be twice the input voltage. This basic operation of charge and discharge is shared among the SCC family, although as highlighted in Section 1.2 the charge and discharge can be carried out in more than two switching states – sub-circuits.

SCC converters are divided into two major families: soft switched SCC and hard switched SCC. Soft switched SCC include an inductive element to generate sinusoidal current waveforms as further discussed in Chapter 2. Sinusoidal waveforms are cut at zero crossing either by a series diode or by a control algorithm. In this way the switching occurs at zero current, resulting in minimal switching losses. In hard switched SCC the switching losses are expected to be high at higher switching frequencies. The problem of which converter type has better overall performance in terms of conduction
and switching losses, and how to evaluate these losses in each converter based on the structure and operation, is the primary objective of this research program.

1.4. **Basic Concepts and Literature Survey of Modeling and Analysis Methods**

A. **Modelling of losses**

The issue of SCC analysis has been tapped by many researchers. Analyses of charge pump SCC date back to 1976 [7]. In that work analysis of Dickson’s charge pump is carried out, transfer function is derived and a basic model circuit is presented, but the analysis is limited to diode-based designs. Other analyses follow the same path of dealing with particular topology [19-25].

Generic analyses that treat SCC as a family began to appear in the 1990s. Good examples are [26-28], but the breakthrough came in 1995 [29]. A fundamental analysis that presented the conversion ratio and operation limits was introduced. The basic circuit shown in Fig. 1.3 was found to be a suitable model for SCC loss calculation. The analysis treated two-phase SCC only, however, and closed solution for SCC equivalent resistance, which represents the SCC losses, was derived for part of the possible operation modes, namely the complete charge (CC) mode: (1.1)

\[
R_o = \frac{p}{q} \frac{T_s}{C}
\]

(1.1)

where \( R_o \) is the output resistance according to the model in Fig. 1.3, \( p \) and \( q \) are positive integers that depend on the converter topology, \( T_s \) is the switching period, and \( C \) is the flying capacitance value.

\[
\begin{align*}
\text{Switched Capacitor DC/DC Converter} \\
\text{Fig. 1.3: DC model of SCC.}
\end{align*}
\]
A summary of hard switched SCC development up to that time was issued in 2001 [30]. Later studies presented more detailed closed-form solutions for two efficiency limits named the slow switching limit (SSL) and the fast switching Limit (FSL) [31, 32]. Soft switched SCC were first recognized as part of the SCC family in [9, 33], and both families were analyzed in [34], but these works dealt with particular topologies. A more generic analysis of soft switched SCC was carried out in [35].

Breakthrough, and unification of both hard and soft switching SCC analysis was done in [36, 37]. An efficiency solution for the complete operation range of the SCC was presented, but it refers to voltage difference between the capacitor and the charging/discharging source, which is a rather complicated parameter. In addition the solution introduced for soft switched SCC is based on a first harmonic approximation. Later studies present state-space averaging application for SCC analysis, and the generation of complex matrices involved in the process [38, 39], but although this approach gives precise results, it is prone to at least two deficiencies. First, it is possible to encounter non-inverting matrices that will prevent the equations and the circuit from being solved. The other is the disconnection of the solution from the loss mechanism, i.e. the source of the losses is not clear. Creation of a straightforward, generic, and unified SCC loss model that will be intuitive to the user is one of the major objectives of this thesis (Chapter 2).

B. Dynamic response

In addition to average static response the accurate dynamic response of a system is essential in the design of a system controller.

When the static response of a system is investigated, it is assumed that the system’s transition is instantaneous or transition bandwidth is much higher than the bandwidth of interest. A DC model is sufficient for describing the static response of a system. An example of a DC or static model is given in Fig. 1.3. The transfer function of the DC model is equal to a constant (or series of constants). Fig. 1.5a shows an example of a DC model's (Fig. 1.3) static response to the step in input voltage. As can be observed, the output, $V_o$, immediately follows the input, $V_{in}$, after the application of step in input voltage at the time, $T_{step}$.

Dynamic response of a system takes into account time, frequency, and/or other parameters, which influence the behavior of the system. To describe dynamic response, differential equations are required. Dynamic response considered as a transfer function from variable/s, or port/s to another variable/s, or port/s of the system, is generally referred to as input and output. When modeling a system, it is
convenient to create a model that describes the dynamic response with respect to a particular parameter, such as time; the rest of the system variables are assumed to be invariant. This significantly simplifies the model and allows evaluation of complicated systems. An example of a dynamic model of the unity gain SCC, which is further discussed in Chapter 4, is shown in Fig. 1.4. This model is good for evaluation of transfer function from $V_{in}$ to $V_o$, and applicable to variations in time and frequency. The dynamic response of the circuit model in Fig. 1.4 is shown in Fig. 1.5b. The excitation signal, as in the static model case, is the step in input voltage. Contrary to the static case, however, the output, $V_o$, does not immediately reach the new value, but rather has a first-order, time-varying response.

Linear systems are the easiest candidates to model. Dynamic models of linear systems, such as the one shown in Fig. 1.4, have an amplitude-independent response. Nonlinear systems, however, are dependent on the excitation signal’s amplitude, phase, etc. For example, bipolar transistors have three operation modes: cut-off, linear, and saturation, and the mode of operation is dependent on the amplitudes of the signal applied to the transistor [40, 41]. So depending on the excitation signal, the behavior of the transistor can change drastically: it can be either a current conductor or a current isolator. This behavior change as a function of operation point is a general characteristic of nonlinear systems. A dynamic model that correctly describes a nonlinear system needs to include the information on system behavior at every single operation point. A dynamic model of this type is known as the “large-signal” model of the system.

The intricate relationships in the large-signal model of nonlinear systems are often very difficult and even impossible to solve. In addition, since controller design is based on evaluation of the system behavior at a particular operation point, an application of the small-signal modeling approach was proved as a good solution, such as the case with bipolar transistor analysis [40, 41]. The small-signal modeling approach is based on the assumption that the perturbations of the modeled variable are sufficiently small, so that the operating point is kept virtually constant. Following this assumption, after location of the operation point, linearization can be applied and the large-signal model converted to a small-signal linear model around that operating point.

![Fig. 1.4: Dynamic model for evaluating $V_o/V_{in}$ for time and frequency response.](image)
There are some studies which deal with SCC dynamic response [42, 43], but these studies are concentrated on particular topologies, supplying the solutions for local problems using state-space averaging analysis. Although the SCC average static behavior was analyzed in numerous earlier studies, as outlined in this section, the issue of dynamic response of SCC has not yet been properly addressed. A generic model capable of reproducing dynamic and static behavior, including small-signal and large-signal response, which is compatible with a large number of SCC is not yet available. The challenge is to describe the correct model circuit configuration and express model parameters, such that the small-signal perturbations as much as the change in operation point are taken into account. This issue is one of the major questions dealt with in this work (Chapter 4).

C. Hybrid converters

Another issue is the systems that contain switched capacitor and switched inductor stages, i.e. hybrid systems. The connection can be either parallel (interleaved), or cascaded as shown in the example in Fig. 1.6 [44]. The basic version includes an inductor with an active switch S, similar to the basic boost stage, cascaded with a switched capacitor doubler, similar to that of Fig. 1.1b, consisting of a single flying capacitor C₁, and based on diodes. The Capacitor C₂ is the output filter, and R_L is the load resistance. This basic converter exhibits inverted output voltage and double the voltage gain of a bare boost converter.
Although these systems are popular in applications that require large conversion ratios, only limited literature is available, which covers static gain analysis [45], dynamic analysis of a particular topology [44], or large-signal analysis only [46]. A generic average model of hybrid PWM switched inductor and switched capacitor converters that is capable of reproducing static and dynamic behavior, including small- and large-signal responses, is not yet available, which was one of the aims of this work.

1.5. RESEARCH OBJECTIVES AND SIGNIFICANCE

The objectives of this work are aimed at tackling the fundamental SCC issues in three interrelated major directions.

1. Expanding our understanding of losses in hard [30, 47] and soft [34, 35, 48] switched SCC systems: namely, probing their origin, developing a unified approach to modeling and analyzing them and, on the basis of the results, creating guidelines that could help designers to meet efficiency goals.

2. Studying the dynamics of SCC systems [49, 50], large- and small-signal response, modeling and simulation techniques and tools.

3. Investigating hybrid switched-capacitor and switched-inductor advanced converters, loss modeling, and dynamic response [44-46].

The contribution of this thesis is primarily new analytical concepts, approaches, and tools (mathematical models, simulation circuit models, theoretical relationship, generic characterizations, and design guides) that better describe the intricate static and dynamic parameter relationships in SCC systems and their comparison with other switch mode converters. These are certainly expanding our understanding of the SCC systems and conceivably have practical uses by designers and users of switch mode converters in general and the SCC technology in particular. The results provide not only more natural and straightforward analysis methods, but also highlight the operation conditions which will lead to better design and potentially improved dynamic performance of SCC systems.
This thesis addresses fundamental issues of modeling and analysis of SCC and SCC systems. The thesis can be divided into two general areas: Chapter 2 and Chapter 3 address issues of SCC losses and creation of fundamental SCC model, and Chapter 4 and Chapter 5 investigate SCC systems’ dynamic response. Earlier versions of some of the technical content of this thesis have been presented in a number of journal and conference articles. Chapter 2 is based on [51], Chapter 3 is the extension of Chapter 2 and a summary of [52]. Chapter 4 is based on [53] and earlier results given in [54], Chapter 5 is based on [55] and applications chapter, Chapter 6, is based on [56, 57].

In this study the following subjects were investigated: modeling techniques of SCC, conduction losses of hard and soft switched SCC, limits and operation ranges, switching losses of hard switched SCC, modeling the dynamic response of hard switched SCC, modeling hybrid converters, implementation of SCC models in simulation software packages, and optimization and design procedures of SCC.

The basic deficiency, inherent conduction losses, of switched capacitor converters (SCC) is reevaluated in Chapter 2 to form a unified and generic SCC model that covers all possible operation modes of SCC, including hard and soft switching. The evaluation was done theoretically, and tested by simulations and experiments. The theoretical solution obtained is of closed form for all operational modes of the SCC. In this investigation, a new modeling approach was developed in which the losses are referred to the load current, a circuit parameter which is relatively easy to calculate as opposed to capacitors' voltage difference used in previous publications. With the approach developed, the losses of SCC can be conveniently represented by an equivalent resistor at the output terminals of the SCC since the losses are already calculated as a function of the output current. The resultant SCC model is simple and intuitive. It consists of a voltage source, called the “target voltage” (the no-load SCC output voltage), the load, and the series equivalent resistor. With this model, SCC operation limits in terms of the losses were derived and optimal operation region was determined. It was found that in addition to a soft switching operation mode, the hard switching operation can be divided into three modes with respect to the capacitor’s charge/discharge current profile. The modes are: “Complete Charge” (CC), that is, the classical mode in which the current reaches exponential asymptote; “No Charge” (NC) while the current is practically constant within the switching instance; and “Partial Charge” (PC) is the mode in between the CC and NC operation modes. The model was thoroughly tested on unity gain, soft and hard switched converters, a 3:1 step down divider and inverting SCC.

In Chapter 3 the new modeling methodology that was developed in Chapter 2 is extended to include
switching losses. An important extension was made to include the losses associated with the finite transitions of the switching devices such as MOSFETs. Unique linear approximation enabled the calculation of the switching losses, and presented them in an intuitive form, which was not possible earlier because of the complexity of exponential expressions and the absence of the fundamental model. Switching losses evaluation was derived theoretically and validated by simulations and experiments. The investigation revealed that in CC operation mode (when the capacitor is charged to the full voltage and then discharged to zero) the effect of switching transition has no impact on the SCC losses. The theoretical model was verified experimentally on an inverting SCC with adjustable switching transition times.

Accurate information on the system’s open-loop response is essential in the design of system controllers to obtain a desired closed-loop response. To this end, a behavioral average circuit model of SCC was developed. The proposed method is able to reconstruct successfully an average behavior of SCC, and is transparent to the switching action of the circuit. The resulting behavioral average circuit can be analyzed by any network analysis method, or evaluated numerically with numerical software package. In this study, the fundamental loss model developed in Chapter 2 was extended to include the dynamic properties of the SCC. The theoretical results of the model were verified by numerical simulations and by experiments. Numerical validations were carried out on two different simulation packages, PSIM and OrCAD PSpice, which represent two different simulation approaches, time-domain simulation and frequency-domain simulation, respectively. The properties tested were the static response, large-signal response, and small-signal behavior of the control-to-output and input-to-output transfer functions. The details are covered in Chapter 4.

The modeling approach of Chapter 4 was applied to evaluate the dynamic features of a hybrid converter that combines a switched inductor Boost (PWM) system cascaded with switched capacitor 1:3 multiplier. The switched inductor part was modeled by average modeling as developed in [58, 59], and the SCC multiplier using the model developed in Chapter 4. The theoretical predictions of the model were compared with numerical simulations in PSIM and laboratory experiments, in various operation modes such as CCM and DCM of switched inductor part, and different capacitor charging profiles of SCC. The details are given in Chapter 5.

During the research program that was carried out a knowledge base for SCC simulation tools was developed. One of the important attributes of the developed SCC model is the equivalent resistance. It was found that this resistance needs to vary during the run time of the simulation. Two implementations
of variable resistors in simulation were developed: dependent current source and nonlinear element. These solutions cover major modern simulation software packages, making it possible to simulate SCC circuits using the model for practically any simulation package that includes dependent sources.

Averaging of any switched converter presents a challenge in terms of merging two (or more) operation phases into a single average circuit. This is especially challenging in the case of flying capacitors that in many converters do not have common potential, yet the charge needs to be transferred to and from the capacitor. To overcome this obstacle a behavioral circuit named “DC Transformer” was adopted. The circuit consists of dependent sources, and has no inductive elements as does the real transformer. Using this element, continuous and concurrent charge and discharge of the capacitor is possible from two (or more) ports or other capacitors, which do not necessarily have common potential points. Also simulation initialization rules are summarized for two of the popular, modern simulation packages PSIM and OrCAD PSpice. The details of the simulation tools can be found in Chapter 4 and Chapter 5.

Out of the wide range of possible applications of the results of this thesis, two examples are presented in Chapter 6. The first example deals with the issues related to hard switched SCC, such as design of active devices, their resistances, and effective ways of choosing the optimal components. The questions of optimal operation mode, impact of switching frequency, the role of real and equivalent resistances and their mutual relationship are discussed. Finally, design guidelines for optimal performance in terms of efficiency are presented. The other example, applied to PV panel equalization modules, presents design guidelines from the very beginning of the decision to use an SCC, followed by the design alternatives for optimal operation mode, and finally considerations of particular component selection in soft switched resonant SCC. Both examples are followed by numerical calculations and experimental validations of the design.

Conclusions are drawn in Chapter 7 summarizing the work.
Chapter 2  Fundamental modeling approach of conduction losses

2.1. INTRODUCTION

Switched Capacitor Converters (henceforth referred to as SCC for plural and singular) suffer from a fundamental power loss deficiency which makes their use in some applications prohibitive. Nonetheless, the SCC do have some noticeable advantages, such as the absence of magnetic components and VLSI compatibility, which make their use in some applications preferable. The power loss has been traditionally explained as being owed to the inherent energy dissipation when a capacitor is charged or discharged by a voltage source or another capacitor [19, 27, 30, 60]. Two types of SCC have been considered in the literature, hard and soft switched SCC. The soft switched SCC employs a small series inductor to achieve zero current switching [10, 14, 33-37, 48, 61-63]. Previous studies that analyze losses in SCC covered the hard switching case [19, 22-31, 38, 60, 64, 65], or the soft switching case [33-35]. A comparison between the two was carried out in [36, 37] which applied the first harmonics approximation to analyze the soft switching case in a unity SCC converter. In this work a generic, scalable and intuitive model that is applicable to both hard and soft switched SCC and a closed-form solution is derived for the two cases. The major advantage of the model presented here is that it expresses, in a modular and expandable approach, the SCC losses as a function of the average current passing through each flying capacitor during each switching phase. Since these currents are linearly proportional to the output current, the individual losses of each subcircuit derived by the proposed model can be linearly added to obtain the total loss of complex topologies such as multi-capacitors and multiphase SCC. The model is valid for cases where the subcircuits of the converter can be described or approximated by a first-order RC network. Furthermore, the model is applicable to SCC that include diodes since diode losses are also expressed as a function of average currents. The model could be used as a tool for the examination of new theoretical concepts, as a designer's aid [57], or as an educational tool for understanding the intricate loss mechanism in SCC and in capacitor charging and discharging in general [66]. An additional feature of the proposed model is its seamless compatibility with circuit simulation software packages. This is because the model is developed in terms of average equivalent circuits rather than state space equations [38, 39, 67-69].
2.2. MODEL DERIVATION - THE CONCEPT

It has been previously shown that any SCC operating in open loop can be represented as a voltage source denoted as the target voltage, $V_T$, connected in series with an equivalent system resistance, $R_e$, that expresses the losses (Fig. 2.1) [26, 29, 31, 37, 38, 61, 64]. This model is applicable to cases in which the charge and discharge of the flying capacitors can be represented by RC, or RLC for the resonant SCC networks. This model does not apply to cases in which the flying capacitor(s) is charged by a current source to facilitate output voltage control [20, 70-74]. The target voltage of the equivalent circuit (Fig. 2.1) refers to the no-load output voltage of the converter and can be evaluated for a given switched capacitor converter by a set of algebraic equations. The equivalent resistance of the equivalent circuit, as developed further in this chapter, expresses the conduction losses of the converter caused by the current that passes via the series resistances in the capacitors’ charge/discharge paths. Switch drive losses, losses owed to stray capacitances [75, 76] and other parasitic losses, owed for example to a shoot-through, are beyond the scope of this work, except for diode losses, which are considered in Section 2.6 and switching losses that are evaluated in Chapter 3 [52].

The proposed model is based on dividing the SCC into switching phases according to the operational modes. This division results in subcircuits, indexed $i$, for each operational phase. For example, in a simple unity converter (Fig. 2.2a), there are two operating modes, the charge mode $i = 1$ and the discharge mode $i = 2$. Each of these charge/discharge processes can be represented by the basic, generic, instantaneous RC circuit of Fig. 2.2b (henceforth referred to as “the basic RC circuit”), in which $\Delta V_i$ is the initial voltage across the switch $S_i$ just before closure, $R_i$ is the total resistance of the loop (switch resistance $R_{S_i}$ and capacitor’s ESR) and $C_i$ is the total capacitance of the loop. It should be pointed out that the currents in the basic RC circuit of Fig. 2.2b are instantaneous, $i(t)$, and that the basic RC circuit is valid both for the charge and discharge processes when a capacitor is

![Diagram](image)

Fig. 2.1: SCC generic average equivalent circuit.
Chapter 2 - Fundamental modeling approach of conduction losses

Fig. 2.2: Unity SCC and the basic charge/discharge RC subcircuit: (a) Unity SCC – switching circuit, (b) The basic and generic, instantaneous RC subcircuit.

connected to a voltage source or to another capacitor. The basic RC circuit of Fig. 2.2b, however, is valid only if the subcircuits can be represented, or approximated, by a first-order system. Such an approximation will be acceptable in the 1:1 SCC of Fig. 2.2a if $C_o \gg C_f$. The latter is universally assumed, albeit sometimes implicitly, in previous SCC modeling approaches [36, 60, 77]. In the soft switching SCC, additional components will appear such as the total inductance of the loop, $L_i$.

Each of the switching phases which are represented by the corresponding subcircuits is responsible for a power loss, $P_i$, which is owed to the power dissipated by the total subcircuit resistance, $R_i$, during the operating cycle of the subcircuit. This power loss of each subcircuit, $P_i$, can then be referenced to the output current, which serves as a common reference for all subcircuits' currents in the converter. This reflection to the output side is possible thanks to the fact that each subcircuit's average current is linearly proportional to the average output current [26, 29, 31]. It should be noted that the phrase "subcircuit's average current," which is also termed in this work "average subcircuit's capacitor current" or “capacitor average current,” refers to the total charge transferred in the subcircuit to/from a capacitor during the switching interval $T_i$, of phase, i, divided by the total switching period, $T_s$. Clearly, a given capacitor will be involved in at least two subcircuits such that it will be charged and discharged periodically by the subcircuits' “capacitor's average currents” which will sum up to zero in steady-state condition [53, 54].

If we apply the proportionality constants, $k_i$, that relate the average subcircuits' currents to the average output current [26, 29, 31], the losses of the subcircuits can be expressed as a function of the output current. This allows the representation of the losses in each subcircuit, i, as a partial equivalent resistance, $R_{ei}$, which represents the contribution of the $i^{th}$ subcircuit to the total equivalent resistance of the converter (Fig. 2.3). Repeating the independent calculations for each switching phase,
Chapter 2 - Fundamental modeling approach of conduction losses

Fig. 2.3: SCC generic average equivalent circuit that shows the contribution of the partial subcircuits' equivalent resistances \( R_e \) to the total equivalent circuit \( R_e \). (In the unity SCC example (Fig. 2.2a), \( R_e \) is the loss contribution of charge subcircuit and \( R_{e2} \) is the loss contribution of discharge subcircuit.)

... (continued from previous context)

along with the switches and capacitors, SCC systems may include diodes [7, 10, 22, 30, 68, 69, 78-82]. The extension of the SCC equivalent model to take into account the losses contributed by the diodes is based on the same concept as described above for the equivalent resistance. Namely, the loss of each diode in each subcircuit is calculated independently as a function of the average subcircuit's current in each switching phase. The losses are then expressed as a function of the output current via the proportionality coefficients \( k_i \). As a result, the diodes’ losses can be emulated by a voltage source, \( V_D \), in series with \( R_e \). This extension is further discussed and illustrated in Section 2.6.

The proposed modeling approach can handle a dual phase as well as multi-phase SCC and is valid for asymmetrical switching duration of the subcircuits. It is assumed however that each of the subcircuits could be represented by a first-order RC circuit for the hard switching case and a simple, under-damped second-order RLC circuit for the soft switching case.

2.3. EQUIVALENT RESISTANCE CALCULATION: HARD SWITCHING CASE

The generic equivalent RC circuit of Fig. 2.2b represents each out of \( i \) operational phases of the hard switched SCC. The energy loss, \( E_{R_i} \), dissipated in the subcircuit's total resistance, \( R_i \), as a result of charge/discharge current flow \( i(t) \) during the time interval \( T_i \) is calculated by integrating the instantaneous power \( p(t) = i^2(t) \cdot R_i \) for the duration of \( T_i \). The basic, first-order RC circuit of Fig. 2.2b has an exponential current waveform, and the integration result takes the form of (2.2),

\[
R_e = \sum_{i=1}^{m} (R_{e_i})
\]
\[ E_{R_i} = \frac{\Delta V_i^2 \cdot C_i}{2} \cdot (1 - e^{-2\beta_i}) \]  
(2.2)

where \( \beta_i = T_i / R_i C_i \).

The charge \( q_i \) transferred during time interval \( T_i \) to/from a capacitor \( C_i \) is calculated to be:

\[ q_i = \Delta V_i \cdot C_i \cdot [1 - e^{-\beta_i}] \]  
(2.3)

The charge \( q_i \) transferred to/from a capacitor, during the subcircuit’s operating time \( T_i \), is used to define the “average subcircuit's capacitor current,” \( I_{C\text{av}_i} \), during phase \( i \) (averaged over the total switching cycle \( T_s = 1 / f_s \)):

\[ I_{C\text{av}_i} = \frac{q_i}{T_s} = q_i f_s \]  
(2.4)

Rearranging (2.3) and (2.4) to express the voltage difference \( \Delta V_i \) as a function of average capacitor current during phase \( i \), one finds:

\[ \Delta V_i = \frac{I_{C\text{av}_i}}{f_s C_i \cdot [1 - e^{-\beta_i}]} \]  
(2.5)

Substituting (2.5) into (2.2) results in an expression for the energy dissipated in the RC subcircuit \( i \), during the switching period \( T_i \) as a function of the average subcircuit's capacitor current \( I_{C\text{av}_i} \).

From (2.2)–(2.5) we find:

\[ E_{R_i} = I_{C\text{av}_i}^2 \cdot \frac{1}{f_s} \cdot \frac{1}{2 f_s C_i} \cdot \frac{(1 + e^{-\beta_i})}{(1 - e^{-\beta_i})} \]  
(2.6)

The power loss as a function of the average subcircuit's capacitor current during phase \( i \), of periodically charged or discharged RC subcircuit, with switching frequency \( f_s \) can now be evaluated as:

\[ P_{R_i} = I_{C\text{av}_i}^2 \cdot \frac{1}{2 f_s C_i} \cdot \frac{(1 + e^{-\beta_i})}{(1 - e^{-\beta_i})} \]  
(2.7)

The average subcircuit's capacitor current during phase \( i \) can be expressed as a function of the average output current, \( I_o \), [26, 29, 31].

\[ I_{C\text{av}_i} = k_i \cdot I_o \]  
(2.8)

where \( k_i \) is the proportionality factor that is calculated by KCL taking into account the charge balance equations for all of the SCC switching capacitors as exemplified and detailed in [26, 29, 31, 64] (an additional example of the proportionality factor calculation is given in Section 2.5 sub-section C. and
demonstrates the extension of the methodology to more complex cases).

From (2.8) and (2.7), the power loss of $i^{th}$ subcircuit could be expressed as a function of common reference, the average output current of the SCC (2.9).

\[
P_{R_i} = I_0^2 \cdot \left( k_i^2 \cdot \frac{1}{2f_s C_i} \cdot \coth \left( \frac{\beta_i}{2} \right) \right)
\]  

(2.9)

The form of (2.9) resembles the classical expression of resistive power dissipation ($P = I^2 \cdot R$) and thus, the expression in brackets (2.9) represents an equivalent resistance. That is, expression (2.10) is the equivalent resistance, $R_{e_i}$, of the $i^{th}$ operational phase of the hard switched SCC, as discussed in Section 2.2:

\[
R_{e_i} = k_i^2 \cdot \frac{1}{2f_s C_i} \cdot \coth \left( \frac{\beta_i}{2} \right)
\]  

(2.10)

2.4. EQUIVALENT RESISTANCE CALCULATION: SOFT SWITCHING CASE

The generic charge/discharge subcircuit of the soft switching case is represented by the corresponding RLC circuit of Fig. 2.4a. At this point, an ideal diode (zero forward voltage) is assumed and the impact of the diode forward voltage on the losses is detailed in Section 2.6. The energy loss, $E_{R_i}$, dissipated in the subcircuit's total resistance, $R_i$, as a result of charge/discharge current flow during the time interval $T_i$ (Fig. 2.4b) is calculated by integrating instantaneous power $p(t) = i(t) \cdot R_i$ during $T_i$. The generic second-order RLC circuit of Fig. 2.4b has a sinusoidal current waveform and the integration result is found to be:

\[
E_{R_i} = \frac{\Delta V_i^2 C_i}{2} (1 - e^{-2\pi \zeta_i}) \quad \text{or} \quad E_{R_i} = \frac{\Delta V_i^2 C_i}{2} (1 - e^{-\frac{\pi}{4Q_i^2}})
\]  

(2.11)

where:

\[
\omega_0_i = \frac{1}{\sqrt{L_i C_i}} \quad Q_i = \frac{1}{R_i C_i \cdot \omega_0_i} = \frac{\omega_0_i \cdot L_i}{R_i} \quad a_i = \frac{R_i}{2L_i} \quad \omega_{di} = 2\pi \cdot f_{di} = \sqrt{\frac{\omega_0^2}{\omega_0^2 - \alpha_i^2}} \quad \zeta_{di} = \frac{\alpha_i}{\omega_{di}}
\]  

(2.12)

It should be noted that (2.11) is valid for oscillatory RLC circuits, i.e. when the quality factor $Q_i > 1/2$. It is also assumed that the time interval $T_i$ of the $i^{th}$ phase is always larger than or equal to half the period of the damped resonant frequency of the basic RLC circuit, (i.e. $T_i \geq T_{\omega_{di}} / 2$, where $T_{\omega_{di}}$ is the period of
Fig. 2.4: Resonant charge/discharge process: (a) The basic and generic instantaneous RLC circuit; (b) Current waveforms: Straight (red) trace – resonant current waveform with no diode; Dashed (blue) trace – actual capacitor charging current waveform with blocking diode.

the damped resonant frequency and is equal to \( T_{\omega_d} = 1/f_s = (2\pi)\omega_{d_i} \) (Fig. 2.4b), and that the ideal diode D (Fig. 2.4a) blocks the reverse current (after \( t = T_{\omega_d} / 2 \) Fig. 2.4b).

The charge \( q_i \) transferred during time interval \( T_i \) to/from a capacitor \( C_i \) is calculated to be:

\[
q_i = \Delta V_i \cdot C_i \cdot (1 + e^{-\pi \xi_i})
\]

(2.13)

On the other hand, the transferred charge \( q_i \) is related to the average subcircuit’s current (averaged over the total switching period \( T_s = 1/f_s \), \( I_{C_{av_i}} \) by:

\[
q_i = \frac{I_{C_{av_i}}}{f_s}
\]

(2.14)

Comparing (2.13) and (2.14) and solving the voltage difference \( \Delta V_i \) results in (2.15), which is a function of the average subcircuit’s capacitor current during the phase \( i \).

\[
\Delta V_i = \frac{I_{C_{av_i}}}{f_s C_i \cdot (1 + e^{-\pi \xi_i})}
\]

(2.15)

By substituting (2.15) into (2.11) the energy dissipated in an RLC subcircuit as a function of the average subcircuit’s capacitor current is obtained. From (2.13)-(2.15) the energy loss as a function of average subcircuit’s capacitor current is found to be:
The power loss as a function of the subcircuit's average capacitor current during phase $i$, of a periodically charged or discharged RLC subcircuit, with frequency $f_s$ can therefore be expressed as:

$$P_{R_i} = I_{C_{av_i}}^2 \cdot \frac{1}{f_s} \cdot \frac{1}{2f_sC_i} \cdot \frac{(1-e^{-\pi \zeta_{di}})}{(1+e^{-\pi \zeta_{di}})}$$ (2.17)

It should be noted that (2.17) is correct for $T_i \geq \frac{T_{on}}{2}$. The optimal operating condition (lowest power dissipation) is when $T_i$ equals half of the period of the damped resonant frequency of the basic RLC circuit (i.e. $T_i = \frac{T_{on}}{2}$). If we apply the hyperbolic tangent function, (2.17) can be expressed as:

$$P_{R_i} = I_{C_{av_i}}^2 \cdot \frac{k_i^2}{2f_sC_i} \cdot \tanh\left(\frac{\pi \cdot \zeta_{di}}{2}\right)$$ (2.18)

This leads to the definition of the partial equivalent resistance $R_{ei}$ of the soft switched SCC owed to the losses of subcircuit $i$, as discussed in Section 2.2:

$$R_{ei} = k_i^2 \cdot \frac{1}{2f_sC_i} \cdot \tanh\left(\frac{\pi \cdot \zeta_{di}}{2}\right)$$ (2.19)

Equation (2.19) can also be expressed in terms of $i^{th}$ RLC subcircuit quality factor, $Q_i$:

$$R_{ei}(Q_i) = k_i^2 \cdot \frac{2Q_i^2 \cdot \pi \cdot R_i}{\text{df}_i} \cdot \tanh\left(\frac{\pi}{\sqrt{4Q_i^2 - 1}}\right)$$ (2.20)

where $\text{df}_i$ is the ratio of switching frequency to the $i^{th}$ RLC subcircuit damped resonant frequency:

$$\text{df}_i = \frac{f_s}{f_{d_i}} = \frac{f_s \cdot R_i C_i}{2} \cdot \sqrt{4Q_i^2 - 1}$$ (2.21)

Examination of the power loss in the hard and soft switching cases (2.9) (2.18) reveals that they can both be expressed as a resistor loss (2.10), (2.19) - (2.20), as shown in previous publications for the hard switching case [26, 29, 31, 36-38, 64]. The above analysis shows that the total equivalent resistance $R_e$, of the converter is in fact the sum of the partial equivalent resistances for "m" switching phases, $R_{e_1}, R_{e_2}, \ldots, R_{e_m}$, (2.1) (Fig. 2.3). The value of the equivalent voltage source $V_T$, often referred to as the "target voltage" of the converter is the open circuit voltage of the SCC, that is, the no-load output voltage.
2.5 Examples

A. Unity gain hard switched SCC

The model's simplicity and its intuitive application are demonstrated by considering a 1:1 SCC. The analysis is carried out under the assumption that $R_{S1} = R_{S2} = R_S$. ESR is assumed to be negligibly small, $C_o >> C_f$, $T_{1,2} = 1 / 2f_s$, and $C_o R_L >> T_{1,2}$. It is further assumed that the SCC is in steady state for which the proposed static model is relevant. The hard switched version of the SCC is first analyzed (Fig. 2.5). The SCC is divided into two phases, charge phase $i = 1$ (Fig. 2.6a) and discharge phase $i = 2$ (Fig. 2.6b). Each of the switching subcircuits presented in Fig. 2.6 is reduced to the basic charge/discharge RC circuit of Fig. 2.2b, and $R_i$, $C_i$, $k_i$, and $\beta_i$ are calculated for $i = 1,2$:

$$R_{1,2} = R_S + ESR; \quad C_{1,2} = C_f; \quad \beta_{1,2} = \frac{1}{2f_s \cdot R_{1,2} C_{1,2}} = \frac{1}{2f_s \cdot (R_S + ESR) \cdot C_f}$$  \hspace{1cm} (2.22)

The value of the proportionality constants $k$ can be obtained by simple charge considerations. Under steady-state condition, the average subcircuit's capacitor current during the charge state is equal to the average subcircuit's capacitor current during the discharge state. Furthermore, the average subcircuit's capacitor current during discharge (Fig. 2.6b) is equal to the average output current. Consequently, all the average currents are equal and hence $k_{1,2} = 1$.

![Fig. 2.5: Simple hard switched 1:1 SCC, switching circuit.](image)

![Fig. 2.6: Hard switched 1:1 SCC operation phases: (a) Charge, (b) Discharge.](image)
Applying (2.10) \( R_{e_i} \) is calculated for \( i = 1, 2 \):

\[
R_{e_i}(RC) = \frac{1}{2f_s C_f} \cdot \coth \left( \frac{\beta_{1,2}}{2} \right)
\]

and the total equivalent resistance for unity SCC according to (2.1) and Fig. 2.3 is:

\[
R_e(RC) = \frac{1}{f_s C_f} \cdot \coth \left( \frac{\beta}{2} \right), \quad \beta = \frac{1}{2f_s \cdot (R_S + ESR) \cdot C_f} \quad (2.24)
\]

B. Unity gain soft switched SCC

The soft switched SCC case (Fig. 2.7) is also analyzed by dividing it into two phases, the charge phase \( i = 1 \) (Fig. 2.8a) and the discharge phase \( i = 2 \) (Fig. 2.8b). Each of the switching subcircuits presented in Fig. 2.8 is reduced to the simple charge/discharge RLC circuit of Fig. 2.4a, and \( L_i, R_i, C_i, k_i \) and \( Q_i \) are calculated for \( i = 1, 2 \):

\[
R_{1,2} = R_S + R_{ind} + ESR; \quad L_{1,2} = L; \quad C_{1,2} = C_f; \quad Q_{1,2} = \frac{1}{(R_S + R_{ind} + ESR) \cdot \sqrt{\frac{L}{C_f}}} \quad (2.25)
\]

The average subcircuit's currents relationship in the soft switched converter is identical to the hard
switched case and again \( k_{1,2} = 1 \). Therefore, (2.20) \( R_{e_i} \) is calculated for \( i = 1, 2 \):

\[
R_{e_i,\text{(RES)}} = \frac{2Q^2_{1,2} \cdot \pi \cdot R_{1,2}}{df_{1,2} \cdot \sqrt{4Q^2_{1,2} - 1}} \cdot \tanh\left(\frac{\pi}{2\sqrt{4Q^2_{1,2} - 1}}\right)
\]

(2.26)

Hence, the total equivalent resistance for soft switched unity SCC according to (2.1) and Fig. 2.3 is:

\[
R_{e\text{(RES)}} = \frac{4Q^2_{1,2} \cdot \pi \cdot R_{1,2}}{df_{1,2} \cdot \sqrt{4Q^2_{1,2} - 1}} \cdot \tanh\left(\frac{\pi}{2\sqrt{4Q^2_{1,2} - 1}}\right)
\]

\[
Q_{1,2} = \frac{1}{(R_S + R_{\text{ind}} + \text{ESR}) \sqrt{L/C_f}}; \quad df_{1,2} = \frac{f_s \cdot R_{1,2} C_f}{2} \cdot \sqrt{4Q^2_{1,2} - 1}
\]

(2.27)

C. \textit{Step down 3:1 hard switched SCC}

The extension to higher-order SCC is demonstrated by considering a step down 3:1 converter (Fig. 2.9) [83] that includes two phases as shown in Fig. 2.10a,b. It is assumed that the circuit is symmetrical, i.e. \( R_{\text{ds,on}} \) of all the switches are equal (denoted \( R_s \)), all the capacitances of flying capacitors are equal (denoted \( C \)) and their ESRs are also equal (denoted ESR). ESR\(_o\) is assumed to be negligibly small, \( C_o >> C_f \), and \( C_o R_L >> T_{1,2} \). Under these assumptions, serially connected capacitors of Fig. 2.10a and the parallel flying capacitor branches of Fig. 2.10b can be combined into a single capacitor and resistor assembly as in Fig. 2.10c and Fig. 2.10d respectively. This is because the initial voltages of the parallel capacitors (Fig. 2.10b) will be close to each other, since in the complementary switching phase (Fig. 2.10a) they are charged/discharged by the same current. The components of the serial circuit of Fig. 2.10a are therefore represented by a single capacitor (\( C/2 \)), a single ESR resistor (\( 2 \cdot \text{ESR} \)), and a single switch resistance (\( 3R_{\text{ds,on}} \)), as shown in Fig. 2.10c. The parallel branches of Fig. 2.10b are therefore represented by one capacitor (\( 2C \)), one series resistor (ESR/2), and one switch resistor (\( R_{\text{ds,on}} \)) as shown in Fig. 2.10d. These simplifications overcome the limitation of a first-order circuit per subcircuit for which the proposed model is valid. It should be noted that the circuits of Fig. 2.10c,d are further reduced to a basic RC subcircuit of Fig. 2.2b and for the purpose of equivalent resistance calculation the total subcircuit resistances and capacitances are derived in (2.30) and (2.31).
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Fig. 2.9: Step down 3:1 SCC, switching circuit.

Fig. 2.10: Step down 3:1 SCC operation phases: (a) Phase 1; (b) Phase 2; (c) Simplified subcircuit of phase 1; (d) Order reduction of the subcircuit of phase 2; Arrows: average subcircuits’ currents.

The \( k_i \) coefficients, which represent the ratio between the average subcircuit’s current and the average output current at steady state, are found by Kirchhoff’s Current Law (KCL) and capacitor charge balance at steady state, as described in [26, 29, 31] and exemplified in [31] and [64]. It should be noted that the present analysis follows the approach, applied throughout this work, in which the average current of each subcircuit is defined as the charge transferred in the subcircuit divided by the complete switching cycle period, \( T_s \). The average subcircuits’ currents, \( \bar{I}_1...\bar{I}_4 \), and the average output current, \( \bar{I}_o \), which flows through the load resistor \( R_L \) are marked with arrows in Fig. 2.10. Matrix (2.28) summarizes
the relationships between the currents. The two first rows are capacitors’ $C_{r1}$ and $C_{r2}$ charge balance equalities, the third row is the KCL equation of the network shown in Fig. 2.10b, and the last, fourth, row is the contribution of the two phases to the output current $I_o$. It is worth mentioning here that the two subcircuits share the output port (Fig. 2.10a,b), and the charge transferred per switching cycle by the average currents $\bar{I}_1$ and $\bar{I}_4$ together to the output port is equal to the average output current.

$$\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 0 & 1 & 1 & -1 \\ 1 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \bar{I}_1 \\ \bar{I}_2 \\ \bar{I}_3 \\ \bar{I}_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ I_o \end{bmatrix}$$ \hspace{1cm} (2.28)

The average currents matrix equation (2.28) has a unique solution (2.29) for capacitors’ average charge/discharge currents, $I_i$, ($i = 1, 2, 3$).

$$\bar{I}_1 = \bar{I}_2 = \bar{I}_3 = \frac{1}{3} I_o$$ \hspace{1cm} (2.29)

This implies that the ratio between the first subcircuit’s current (Fig. 2.10c) and the average output current is $k_1 = \bar{I}_1/I_o = 1/3$ (Fig. 2.10a,c). For the second subcircuit (Fig. 2.10d) because of the merger of two capacitors, $C_{r1}$ and $C_{r2}$, which carried $I_o/3$ each, $\bar{I}_2$ and $\bar{I}_3$ (Fig. 2.10b,d), $k_2 = \bar{I}_2/I_o + \bar{I}_3/I_o = 2/3$.

The total equivalent capacitances of the subcircuits for phases 1 and 2 are:

$$C_1 = \frac{C \cdot C_o}{2 \cdot C_o + C} , \quad C_2 = \frac{2 \cdot C_o \cdot C}{C_o + 2 \cdot C}$$ \hspace{1cm} (2.30)

The total resistances of the subcircuits are:

$$R_1 = 3R_S + 2ESR; \quad R_2 = R_S + ESR/2$$ \hspace{1cm} (2.31)

Defining $T_1$, $T_2$ as the duration of the first and second phases, we can express $\beta_1$ and $\beta_2$ as:

$$\beta_1 = \frac{T_1}{R_1 C_1} = \frac{T_1}{(3R_S + 2ESR) \left( \frac{C \cdot C_o}{2 \cdot C_o + C} \right)} ; \quad \beta_2 = \frac{T_2}{R_2 \left( \frac{ESR}{2} \right) \left( \frac{2 \cdot C_o \cdot C}{C_o + 2 \cdot C} \right)}$$ \hspace{1cm} (2.32)

The partial equivalent resistances for each phase can thus be expressed as:

$$R_{e_1} = \left( \frac{1}{3} \right)^2 \cdot \frac{1}{2f_S^2} \cdot \left( \frac{C \cdot C_o}{2 \cdot C_o + C} \right) \cdot \coth \left( \frac{\beta_1}{2} \right) ; \quad R_{e_2} = \left( \frac{2}{3} \right)^2 \cdot \frac{1}{2f_S^2} \cdot \left( \frac{2 \cdot C_o \cdot C}{C_o + 2 \cdot C} \right) \cdot \coth \left( \frac{\beta_2}{2} \right)$$ \hspace{1cm} (2.33)

and the total equivalent resistance of the converter is:

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\[ R_e = \frac{1}{18f_sC_{o}} \left\{ (2C_o + C) \cdot \coth\left(\frac{\beta_1}{2}\right) + 2(C_o + 2C) \cdot \coth\left(\frac{\beta_2}{2}\right) \right\} \]  \hspace{1cm} (2.34)

For infinitely large output capacitor \( C_o \), the output equivalent resistance \( R_e \) is reduced to:

\[ R_e = \frac{1}{9} \cdot \frac{1}{f_sC} \left\{ \coth\left(\frac{\beta_1}{2}\right) + \coth\left(\frac{\beta_2}{2}\right) \right\} \]  \hspace{1cm} (2.35)

where \( \beta_1 = \frac{T_1}{C(1.5R_S + ESR)} \); \( \beta_2 = \frac{T_2}{C(2R_S + ESR)} \).

Being a 3:1 step-down converter, the target voltage, \( V_T \), is in this case: \( V_T = V_{in} / 3 \).

### 2.6. Diode Conduction Losses

The extension of the SCC equivalent model to include the losses contributed by diodes is demonstrated by considering an inverting 1:1 SCC (Fig. 2.11), which operates in two phases as shown in Fig. 2.12. Each of the switching subcircuits of Fig. 2.12 is reduced to the basic charge/discharge RC circuit of Fig. 2.2b that includes a diode, and \( R_i, \, C_i, \, k_i, \) and \( \beta_i \) are calculated for \( i = 1,2 \) as:

\[ R_i = R_S + ESR; \quad R_2 = R_S + ESR; \quad C_i = C_f; \quad C_2 = \frac{C_f \cdot C_o}{C_f + C_o} \]  \hspace{1cm} (2.36)

![Fig. 2.11: Inverting 1:1 SCC, switching circuit.](image)

![Fig. 2.12: Hard switched inverting 1:1 SCC operational phases: (a) Charge, (b) Discharge.](image)
\[
\beta_1 = \frac{1}{2f_s(R_s + ESR)C_f}; \quad \beta_2 = \frac{1}{2f_s(R_s + ESR) \left( \frac{C_f \cdot C_o}{C_f + C_o} \right)}
\]

(2.37)

The average current of the load is transferred by the flying capacitor, \( k_{1,2} = 1 \). Applying (2.10) \( R_e \), we can calculate for \( i = 1, 2 \):

\[
R_s = \frac{1}{2f_s C_f} \cdot \coth \left( \frac{\beta_1}{2} \right); \quad R_e = \frac{1}{2f_s \left( \frac{C_f \cdot C_o}{C_f + C_o} \right)} \cdot \coth \left( \frac{\beta_2}{2} \right)
\]

(2.38)

and the total equivalent resistance for the inverting SCC according to (2.1) and Fig. 2.3 is:

\[
R_e = \frac{1}{2f_s C_f} \left[ \frac{\coth \left( \frac{\beta_1}{2} \right) + \frac{C_f + C_o}{C_f} \cdot \coth \left( \frac{\beta_2}{2} \right)}{2} \right]
\]

(2.39)

Diode conduction losses are modeled by adding to the generic equivalent circuit a voltage source \( V_D \) (Fig. 2.13) that is equal to the sum of the forward voltage drops, \( V_{f_i} \), of all the diodes in the circuit multiplied by their proportionality constants \( k_i \), which relate the average subcircuit's current through each diode to the output current.

\[
V_D = \sum_{i=1}^{m} \left( k_i \cdot V_{f_i} \right)
\]

(2.40)

Since in this inverting SCC \( m = 2 \), \( k_{1,2} = 1 \), and assuming equal diodes \( V_{f_1} = V_{f_2} = V_f \), one finds: \( V_D = 2V_f \), where \( V_f \) is the average voltage drop across a single diode. Being an inverting 1:1 SCC, the target voltage \( V_T \) in this case is: \( V_T = -V_{in} \) (Fig. 2.13). \( V_D \) is also of negative polarity to correctly introduce the power loss for the negative current that will flow.

Fig. 2.13: SCC generic average equivalent circuit including diode losses.

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2.7. LIMITS OF OPERATING MODES

The behavior of SCC at the boundaries has been previously derived for the hard [29, 31, 36, 64, 66] and soft switching [36] cases. For the sake of completeness, we present the limits by applying the loss expressions developed in this study.

Analysis of the loss expressions for the hard switched case reveals that the losses of a given SCC depend on the value of (2.13) for each of the subcircuits. This value depends, in turn, on the operating mode of the SCC and in particular on the value of $\beta_i$, which will determine if (1) the charging/discharging process is completed within $T_i$ with the current waveform shown in Fig. 2.14a (denoted here as the CC case), (2) the charging is partially completed (PC) and has the current waveform that is presented in Fig. 2.14b, or (3) the current will be about constant (Fig. 2.14c) and the capacitor will have a practically constant voltage (denoted as No Charging – NC).

The modes of operation (CC, PC, or NC) depend on the value of $\beta_i$, namely on the relationship between $T_i$ and $R_iC_i$. The behavior of the function (2.10) can be conveniently examined by considering its asymptotic values when $\beta_i << 1$ and $\beta_i >> 1$.

The asymptotic value for the NC case $\beta_i << 1$ ($T_i << R_iC_i$) is:

$$R_{e,i,(NC)} = R_{e,i} \left|_{\beta_i << 1} \right. = \left\{ k_i^2 \frac{R_i}{f_sT_i} \right\}$$

(2.41)

and for the CC case $\beta_i >> 1$ ($T_i >> R_iC_i$):

$$R_{e,i,(CC)} = R_{e,i} \left|_{\beta_i >> 1} \right. = \left\{ k_i^2 \frac{1}{2f_sC_i} \right\}$$

(2.42)

Since $\beta_i$ is a function of $R_i$, the general expression (2.10), which is applicable to the PC case, is clearly

![Diagram showing charge/discharge current waveforms: Complete Charge - CC mode, Partial Charge - PC mode, No Charge - NC mode.](image_url)

Fig. 2.14: Charge/Discharge instantaneous current waveforms: (a) Complete Charge – CC mode; (b) Partial Charge – PC mode; (c) No Charge – NC mode.
dependent on the switch resistance. Similarly, the losses in the NC case (2.41) are also dependent on the switch resistance. Hence in these operating regions the switch resistance will affect the efficiency. In contrast, expression (2.42) implies that in the case of the complete charge (CC), the switch resistance does not influence the losses. The same resistance-independent result is obtained by an energy balance calculation, when a capacitor is charged to the full value of the charging voltage source. The behavior of $R_e$ over the full range of the charge/discharge regions (CC, PC, and NC) is given in Fig. 2.15 which presents the normalized equivalent resistance of a single charge or discharge subcircuit, derived from (2.10) and normalized by the factor $\frac{1}{m \cdot k_1^2 \cdot R_i}$ and assuming symmetrical operation (the same switching duration for each of the m subcircuits) (2.43).

$$R_e^* = \frac{R_e}{m \cdot k_1^2 \cdot R_i} = \frac{\beta_i}{2} \cdot \coth \left( \frac{\beta_i}{2} \right)$$

(2.43)

The curve can be approximated by two linear sections (Fig. 2.15), one for high betas and one for low betas. For the high beta cases, which correspond to the CC mode (2.42), $1/fC$ is a dominant term forcing the equivalent resistance to increase linearly as beta increases. In the case of low betas (which correspond to the NC zone (2.41)) $R_e$ is maintained constant because of the convergence of (2.43) to a constant value (2.41) as beta approaches zero. It can thus be concluded that when the switching duration is greater than the time constant of the subcircuit (corresponding to large betas) the equivalent resistance

![Fig. 2.15: Normalized equivalent resistance.](image-url)
is independent of the switch resistance but heavily dependent on $T_i$, and thus the switching frequency. In this region, the lower the switching frequency, the greater will be the losses (for the same average subcircuit’s current). The lesser loss at short switching times is a direct outcome of the fact that in this case (Fig. 2.14c), the charge/discharge RMS current is smaller than in the exponential case (Fig. 2.14a), which prevails in the longer switching time. When the switching time is much shorter than the time constant of the circuit, the current is practically constant during the switching time and hence the RMS value is the lowest one possible. For the non-symmetrical case, the RMS currents of each phase are not equal and the total equivalent resistance will reach higher values as depicted in Fig. 2.16 for the two-phase, hard switched, unity converter.

It has been suggested in [64, 84] that the values of $R_e$ around the breakpoint of the curve shown in Fig. 2.15 can be approximated by an empirical equation (2.44) that applies the boundary values of $R_e$, (2.41) and (2.42), that were derived earlier [29, 31, 36, 64, 66].

$$R_{ei} = \frac{p R_e^{i \text{(NC)}} + R_e^{i \text{(CC)}}}{p}$$

(2.44)

where $p = 2$. In a following study [85], however, Makowski reexamined the approximation by comparing it with (2.10) and showed that a better fitting is obtained when $p = 2.54$. An example of the fitting accuracy is given in Fig. 2.17.

![Fig. 2.16: Dependence of the equivalent resistance on the duty cycle (D) as a function of normalized frequency in a two-phase, hard switched unity SCC.](image-url)
Similarly to the hard switching case, the loss expression for the soft switched converters was evaluated in this study as a function of the output current (2.19), (2.20) which implies that the total equivalent resistance of the SCC also follows the simple addition concept as depicted in Fig. 2.3, as proposed in this work. Expression (2.20) reveals that the losses are a function of three key parameters: \( R_i \), which is the subcircuit’s resistance, \( df_i \), which is the ratio between the switching frequency, \( f_s \), and the damped resonant frequency, \( f_{di} \), of the RLC subcircuit, which we call the “frequency ratio”, and \( Q_i \), which is the RLC subcircuits’ quality factor. The dependence of the normalized RLC subcircuit’s equivalent resistance, \( R^* \) (2.45), on the quality factor \( Q_i \), with \( df_i \) as a parameter is depicted in Fig. 2.18, where:

\[
R^* = \frac{R_{ei}}{k_i^2 \cdot R_i} = \frac{2Q_i^2 \cdot \pi}{df_i \cdot \sqrt{4Q_i^2 - 1}} \cdot \frac{\tanh(\frac{\pi}{2\sqrt{4Q_i^2 - 1}})}{\frac{\pi}{2\sqrt{4Q_i^2 - 1}}}
\]  

(2.45)

Fig. 2.18: Dependence of the normalized RLC subcircuit’s equivalent resistance on the subcircuit's quality factor (\( Q_i \)) with frequency ratio (\( df_i \)) as a parameter.
Fig. 2.18 reveals that the normalized equivalent resistance is a weak function of Q, once the quality factor is above three. The frequency ratio, however, has a strong effect on the equivalent resistance (Fig. 2.18). This is because the rms current of the subcircuit increases as \( df_i \) becomes smaller (\( df_i = f_s/f_{di} \)). The increase in \( R_e \) can be used, as in the case of the hard switched SCC, to regulate the output voltage. This can conveniently be done by controlling the switching frequency \( f_s \). To maintain soft switching, the boundary \( T_i \geq \pi/\omega_{di} \) must be observed.

The highest efficiency in the soft switched SCC is thus reached when two conditions are met: (1) the value of the quality factor is at least 3 and, (2) the switching duration \( T_i \) is matched to half damped resonant period, \( T_i = \pi/\omega_{di} \).

For the high-quality factor case, condition (a) - \( (Q_i \gg 1) \), the expression of the equivalent resistance (2.20) can be significantly simplified. Applying Taylor’s series extension one finds that \( \tanh(x) \) can be approximated by \( x \), when \( x \) approaches zero. A further simplification is obtained by approximating the term of \( (4Q_i^2 - 1) \) as \( 4Q_i^2 \), and consequently (2.20) can be approximated by expression (2.46):

\[
\lim_{Q_i \to \infty} R_e = k_1^2 \cdot \frac{2Q_i^2 \cdot \pi \cdot R_i}{df_1 \cdot \sqrt{4Q_i^2}} \left( \frac{\frac{\pi}{2} \cdot \sqrt{4Q_i^2}}{2 \cdot \sqrt{4Q_i^2}} \right) \tag{2.46}
\]

which can be expressed as:

\[
\lim_{Q_i \to \infty} R_e = k_1^2 \cdot \frac{\pi \cdot R_i}{4 \cdot df_1} \tag{2.47}
\]

In the case of a symmetrical 1:1 SCC \( (k_{1,2} = 1) \), with matched frequencies for both phases \( (f_{d(1,2)} = f_s, \ df_{1,2} = 1) \), the limiting value for each of the subcircuits takes the form:

\[
\lim_{Q_i \to \infty} R_e = k_1^2 \cdot \frac{\pi \cdot R_i}{4 \cdot df_1} = \frac{1}{2} \cdot 5R_i \tag{2.48}
\]

The results of the special 1:1 SCC case (2.48) are similar to those presented in [36], which were derived by applying the first harmonic approximation. The more general expression, which is applicable for any Q value above \( \frac{1}{2} \), is given in (2.20), and the limiting equivalent resistance value for any RLC-based SCC is expressed by (2.47).
2.8 Verification by simulation and experiments

The analytical expressions developed in this study were checked against simulation and experimental results. Output voltage measurements were used as an indicator for conduction losses of the converter, applying the fact that the efficiency of SCC is given by:

$$\eta = \frac{V_o}{M \cdot V_{in}} = \frac{V_o}{V_T}$$

(2.49)

where $\eta$ is an efficiency, $V_{in}$ is an input voltage, $M$ is the conversion ratio of the SCC, $V_T$ is a target voltage of SCC, ($M \cdot V_{in} = V_T$), and $V_o$ is an output voltage (Fig. 2.1), [19, 20, 25, 29, 30, 57, 60, 61, 65, 66, 69]. It should be mentioned here that (2.49) is correct under the assumption that switching losses [52] and substrate capacitive leakage currents [76] and other extraneous effects are negligible compared with the average current transferred by the SCC. Furthermore, charge flow paths within the converter that are not directly transferring charges from input to output [86] may also cause the efficiency value to deviate from (2.49). Hence, the measurement of the output average voltage while the output ripple is relatively low reflects the amount of losses in SCC:

$$\frac{P_{Loss}}{P_{in}} = \frac{P_{in} - P_o}{P_{in}} = 1 - \eta = 1 - \frac{V_o}{V_T}$$

(2.50)

where $P_{in}$ is the input power, $P_o$ is the output power and $P_{Loss}$ is the conduction losses. Consequently:

$$P_{Loss} = P_{in} (1 - \frac{V_o}{V_T})$$

(2.51)

Furthermore, the value of $V_o$ is in fact determined by $R_e$, since:

$$\eta = \frac{R_o}{R_e + R_o} = \frac{V_o}{V_T}$$

(2.52)

and hence:

$$R_e = \frac{R_o (V_T - V_o)}{V_o}$$

(2.53)

Fig. 2.19 presents simulation and model results for the step-down 3:1 hard switched SCC shown in Fig. 2.9. The equivalent resistance was calculated with Eq. (2.34). SCC parameters were set as: $V_{in} = 36V$, $C_{f1,2} = 22\mu F$, ESR = 100m$\Omega$, $C_o = 560\mu F$, ESR$o$ is negligible, $R_L = 12\Omega$, $R_{ds,on} = 100m\Omega$, $f_s = 100kHz$ and dead time of 100ns. Model-derived and step-by-step full circuit simulation output voltage was found to be 11.8V, which corresponds to 2% losses (calculated from (2.50)).
Fig. 2.19: Simulated and model results of hard switched 3:1 step-down SCC: Upper traces - output voltage. Lower trace - capacitor current ($C_f$).

Fig. 2.20a depicts simulation and model results of a soft switched 1:1 unity converter (Fig. 2.7): $V_{in} = 24\, V$, $L = 2.3\, \mu H$, $C_f = 1\, \mu F$, ESR = 70mΩ, $C_o = 560\, \mu F$, ESR$_o$ = 38mΩ (assumed to be zero for simulation and model evaluation), $R_L = 91\, \Omega$, MOSFETs IRF840 with $R_{ds\_on} = 0.85\, \Omega$, $f_s = 100kHz$ and dead time of 100ns. The experimental waveforms for this soft switching case are presented in Fig. 2.20b.

Fig. 2.20: Soft switched 1:1 unity converter waveforms: (a) Simulation and model, (b) Experimental.
The simulated and model-derived output voltage was 21.96V, which represents 8.5% loss, and the measured output voltage in this case was 22V, which corresponds to a loss of 8.333% (2.50). Model equivalent resistance was calculated by (2.27).

The inverting SCC, as presented in Fig. 2.11, was evaluated under asymmetrical operation, at a duty cycle of 0.8. The SCC parameters were as follows: $V_{in} = 12V$, $C_t = 22\mu F$, $ESR = 100m\Omega$, $C_o = 560\mu F$, $ESR_o = 38m\Omega$ (assumed to be zero for simulation and model evaluation), $R_L = 12.1\Omega$, $f_s = 60kHz$ and dead time of 100ns. Based on the datasheet and operational conditions, the average forward diode voltage drop of MBR320P diodes was estimated to be around 0.35V. The switches were: $S_1$ - SMU10P05, $S_2$ - SMU15N05 with $R_{ds, on}$ of 0.28 and 0.1Ω respectively. The power associated with drive and control of the inverting prototype is not included in the efficiency calculations presented here. Rise and fall times of the switches were approximately 100ns, significantly shorter than the switching period, and that being so switch transition-associated losses (switching losses) are neglected in the efficiency calculations [52]. Model equivalent resistance was calculated with (2.39) and model equivalent diode voltage source was calculated with (2.40). Simulation and model results are presented in Fig. 2.21a and experimental results in Fig. 2.21b. Model-derived output voltage was found to be -9.95V, which represents a loss of 17.1%, and the step-by-step simulation result yielded -9.84V, a loss of 18%; experimentally measured output voltage was -9.81V, corresponding to 18.25% loss.

An additional example of equivalent resistance and loss calculation and its experimental validation in a multi-phase, multi-capacitor, extended binary SCC is described in [15, 83]. Furthermore, a recently proposed SCC [87-89] can be approximated by first-order RC subcircuits and can thus be analyzed by the proposed approach, which can also be applied to hybrid converters that include both a switched inductor and a switched capacitor sections [55, 90].

2.9.DISCUSION AND CONCLUSIONS

The loss analysis approach developed in this work resulted in a unified model that describes conduction losses of the subcircuits in hard and soft switched SCC cases. Closed-form solutions were derived and checked against complete (cycle-by-cycle) simulation and experimentally.

An important feature of the proposed model is that it is based on the SCC subcircuits’ average capacitor currents. This enables a systematic procedure for modeling multi-phase and multi-capacitor SCC systems over the complete range of operation (CC, PC, and NC) for hard switching cases and for any switching frequency (provided that $T_i \geq T_{o,q} / 2$) for soft switched cases. The proposed model is
applicable to SCC topologies for which the subcircuits can be described by a first-order network. As demonstrated in this chapter, however, subcircuits of practical SCC, which do not appear to meet this first-order requirement, can still be approximated as first-order networks and can thus be analyzed by the proposed modeling approach.

Another unique feature of the model is its ability to handle hard and soft switched SCC topologies that include diodes, topologies that are often referred to as “charge pumps” or “voltage multipliers.” This capability is automatically achieved because the analysis is based on the average currents in the subcircuits, which are the pivotal parameters for calculating diode loss.

The proposed model applies a new concept, “the equivalent resistance of a subcircuit” $R_{eq}$, which is a measure of the dissipative component defined in terms of the average subcircuit’s current. Since the average subcircuit currents are linearly proportional to the output current, the subcircuits’ equivalent

---

Fig. 2.21: Hard switched inverting 1:1 SCC waveforms: (a) Full circuit (cycle by cycle) simulation and model calculation; (b) Experimental.
resistance can be considered as the basic components of the total equivalent resistance of the system (Fig. 2.3). Since the losses of each subcircuit are evaluated independently, the contribution of each subcircuit is rendered clear and intuitive. This could help to optimize SCC designs by trimming the fundamental parameters that affect the losses. That is, the ratio between the subcircuits’ switching time $T_i$ and the time constant $R_iC_i$ in hard switching, and the quality factor and the ratio between the switching and the resonant frequencies in the soft switched case. In addition, since the model is based on the equivalent circuit approach rather than the state-space averaging model methodology, it is seamlessly compatible with general-purpose circuit simulators and can be used to explore various output voltage regulation schemes [15, 91-93], and to develop average simulation models [53-55, 94].
Chapter 3  Switching losses

3.1. INTRODUCTION

Two types of SCC have been considered in the literature; hard switched and soft switched. The soft switched SCC use a series inductor to achieve zero current switching [34, 36, 37, 48]. Inductor insertion creates resonant current waveform, which is cut using diodes or appropriate control scheme exactly at zero crossing. As a result switching losses are negligible in this operation mode. In hard switched SCC, however, there is no mechanism to ensure zero current/voltage switching, and investigation of possible losses resulting from switch transitions is required. Earlier studies [26, 28, 29, 31, 34, 36-38, 48, 51, 57, 64, 66, 83], considered only conduction losses in SCC circuits and neglected switching losses. It has been postulated that there is no need to add the switching losses since they are part of the charge/discharge process and, as such, already included in the calculated losses. As revealed in this work, this conjecture is correct if during each switching phase the charge/discharge process is completed. That is, for cases where the equivalent time constant of the subcircuits is lower than the switching durations. When, however, the charge/discharge process is incomplete, switching losses need to be added. The reason for this is that during the rise and fall times of the current, the instantaneous losses are larger than when the switch is in the “on” state because the effective resistances during these durations are higher than the switch resistance in the “on” state. The objective of this part of the work is to delineate the contribution of the switching process to switching losses in hard switched SCC systems.

The analytical approach pursued here follows the concept introduced in Chapter 2 [51, 83], in which the losses are expressed as a function of the average current passing through each flying capacitor. Since these currents are linearly proportional to the output current, the losses can easily be related to the output current of the SCC. The proposed model can be applied to derive the losses of SCC with multiple capacitors. The analysis presented here is an approximate analysis that is based on the assumption that the rise and fall times are substantially shorter than the switching phase duration. This assumption leads to simple and comprehensible expressions that can be intuitively understood and help to clarify the issue of switching losses in SCC.
3.2. APPROXIMATE ANALYSIS OF SCC LOSSES INCLUDING THE SWITCHING TRANSITIONS

The fundamental SCC analysis of Chapter 2 presents SCC operation modes and describes the source of the conduction losses. Nonetheless, switching loss-related observations based on the fundamental model can be made. From Fig. 2.15, Fig. 2.17 and from (2.41), (2.42) it can be concluded that on the one hand, in the classical case (the CC operation mode), SCC conduction losses are independent of the charge/discharge loop resistance, \( R_i \) (2.42). The waveform and, consequently, the switch rise and fall times have no impact on the losses. On the other hand, in the NC operation mode the impact of \( R_i \) on the SCC losses is obvious (2.41). Here (NC mode) the rise and fall times of the switch will affect the losses since they introduce a significant change in the current waveform and, consequently, in its RMS value. Hence, rise and fall processes need to be taken into account when we calculate the losses.

For the sake of clarity and brevity we consider the case of a 1:1 SCC, as depicted in Fig. 3.1. The analysis is made under the assumption that the input voltage, \( V_{in} \), and output voltage, \( V_o \), are constant over a switching cycle, the switches \( S_1 \) and \( S_2 \) have “on” resistances of \( R_{S1} \) and \( R_{S2} \) respectively, the flying capacitor, \( C \), has a series loss component, \( R_{ESR} \), and the switches connect the flying capacitor, \( C \), to \( V_{in} \) and \( V_o \) during the times \( T_1 \) - charging phase \( i = 1 \) and \( T_2 \) - discharging phase \( i = 2 \), respectively. These “on” times include the rise time and fall times, \( t_r \), \( t_f \), of the switches, respectively.

The switching frequency is \( f_s \) and the switching period \( T_s = 1/f_s \). Note that because of possible dead time between switch transitions, the total duration, \( T_1 + T_2 \), may be smaller than \( T_s \). As discussed in Chapter 2, the generic charge/discharge process for each switching phase, \( T_i \), can be represented by the basic equivalent circuit of Fig. 3.2, in which \( \Delta V_{0i} \) (\( i = 1, 2 \)) is the initial voltage difference between the capacitor and the corresponding voltage source (\( V_{in} \) or \( V_o \) in the present example), \( R_i \) is the total resistance of the loop (switch “on” resistance and capacitor’s ESR), \( C_i \) is the equivalent capacitance of the loop and the initial voltage across \( C_i \) is zero, as in Fig. 3.2. The MOSFET switch, \( S \), in the model of Fig. 3.2 represents the fact that the rise and fall times of the loop current are not instantaneous.

![Fig. 3.1: Hard switched unity gain SCC.](image-url)
Depending on the relationship between the time constant, $R_iC_i$, and the switching time, $T_i$ ($T_1$ and $T_2$ in the simple case of unity gain SCC), the charge/discharge process may take one of three possible forms (Fig. 3.3) [51, 57, 66, 83].

A. The effect of the switching process when $T_i >> R_iC_i$ Complete Charge – “CC” mode:

This is the classical textbook case in which the capacitor is fully charged to $\Delta V_{0i}$ during the switching phase, $T_i$ (Fig. 3.3a). The term “average capacitor current - $I_{C_{AVi}}$” in this work means the current averaged over the full switching period, $T_s$, or, in other words, the total charge transferred to/from a capacitor divided by the total switching period of the converter. Thus, the average capacitor current, $I_{C_{AVi}}$, is related to the initial voltage, $\Delta V_{0i}$, by:

$$\Delta V_{0i} = \frac{I_{C_{AVi}} T_s}{C_i}$$

(3.1)

The energy loss in this classical case, $E_{(a)ii}$, during the switching phase $T_i$ is:

$$E_{(a)ii} = \Delta V_{0i} \cdot I_{C_{AVi}} T_s - \frac{(\Delta V_{0i})^2 C_i}{2} = \frac{(I_{C_{AVi}} T_s)^2}{2C_i}$$

(3.2)

Since the average capacitor current, $I_{C_{AVi}}$, is linearly proportional to the SCC output current, $I_o$, by a
factor \( k_i \) [29, 31, 51, 64, 83], the contribution of the switching phase, \( T_i \), to the average power loss of the SCC is:

\[
P_{(a)} = I_o^2 \left[ k_i^2 \frac{1}{2 f_s C_i} \right] \quad (3.3)
\]

and the total power loss (charge plus discharge phases) for the symmetrical 1:1 SCC \((C = C_i, k_i = 1 \text{ for } i = 1, 2)\) is:

\[
P_{(a)} = I_o^2 \left[ \frac{1}{f_s C} \right] \quad (3.4)
\]

As expected, the total power loss is independent of the rise and fall times and, in fact, of the charge/discharge current shape [29, 31, 37, 51, 57, 64, 66, 83]. As discussed in Chapter 2 and shown earlier in [51, 57, 83] the term multiplying \((I_o)^2\) in (3.4) is the output resistance of the generic SCC average model.

**B. The effect of the switching process when \( T_i \approx R_i C_i \) Partial Charge – “PC” mode**

The evaluation of this intermediate case, depicted in Fig. 3.3b and in further detail in Fig. 3.4, is carried out under the assumption that the rise and fall time intervals are relatively short compared with the “on” time, and consequently the voltage \( \Delta V_i \) across the loop resistance \( R_i \) and switch, \( S \) (Fig. 3.2), is constant during these short intervals (Fig. 3.4).

The charges transferred during rise time, \( Q_{ri} \), on time, \( Q_{oni} \), and fall time, \( Q_{fi} \) (Fig. 3.4), are:

\[
Q_{ri} = \frac{\Delta V_{0i}}{2R_i} t_{ri} \; ; \; \; \; \; Q_{oni} = \Delta V_{0i} C_i \left[ e^{-\beta_i} - 1 \right] \; ; \; \; \; Q_{fi} = \frac{\Delta V_{0i}}{2R_i} e^{-\beta_i} \cdot t_{fi} \quad (3.5)
\]

where \( \beta_i = t_{on}/(R_i C_i) \). The total charge, \( Q_T \), transferred during the time period \( T_i \) is the sum of \( Q_{ri} \), \( Q_{oni} \) and \( Q_{fi} \), and its relation to the output current as discussed in Chapter 2 is:

\[
I_o = Q_T \cdot f_s / k_i \quad (3.6)
\]

Combining (3.5) and (3.6), \( \Delta V_{0i} \) can now be expressed as a function of output current:

\[
\Delta V_{0i} = \frac{2R_i \cdot k_i \cdot I_o}{f_s \cdot \left[ t_{ri} + 2R_i C_i \left( e^{-\beta_i} - 1 \right) + t_{fi} \cdot e^{-\beta_i} \right]} \quad (3.7)
\]
The energy losses during rise time, $E_{ri}$, “on” time, $E_{oni}$ and fall time, $E_{fi}$ (Fig. 3.4), are:

$$E_{ri} = \frac{\Delta V_{0i}^2}{2R_i} \cdot t_r; \quad E_{oni} = \frac{\Delta V_{0i}^2}{2} C_i (1-e^{-2\beta_i}); \quad E_{fi} = \frac{\Delta V_{0i}^2}{2R_i} e^{-2\beta_i} \cdot t_f$$  \hspace{1cm} (3.8)$$

The total power dissipated during time interval $T_i$ is equal to the sum of $E_{ri}$, $E_{oni}$ and $E_{fi}$ multiplied by switching frequency:

$$P_{avg_i} = \Delta V_{0i}^2 \cdot \frac{f_s}{2R_i} \cdot \left( t_r + R_i C_i (1-e^{-2\beta_i}) + t_f \cdot e^{-2\beta_i} \right)$$  \hspace{1cm} (3.9)$$

Substituting (3.7) into (3.9) and tidying results in the expression for the average power loss of $i^{th}$ subcircuit operating in the PC mode:

$$P_{(b)}_i = I_0^2 \cdot \frac{k_i^2 \cdot 2 \cdot R_i}{(4R)} \cdot \frac{1}{f_s} \cdot \left( \frac{t_r + R_i C_i (1-e^{-2\beta_i}) + t_f \cdot e^{-2\beta_i}}{t_r + 2R_i C_i (1-e^{-\beta_i}) + t_f \cdot e^{-\beta_i}} \right)^2$$  \hspace{1cm} (3.10)$$

For the symmetrical unity gain SCC ($T_1 = T_2 = T_s/2$, $R = R_1 = R_2$, $\beta = 1/(2T_sRC)$):

$$P_{(b)} = I_0^2 \cdot \frac{1}{(4R)} \cdot \frac{1}{f_s} \cdot \left( \frac{t_r + R C_i (1-e^{-2\beta}) + t_f \cdot e^{-2\beta}}{t_r + 2R C_i (1-e^{-\beta}) + t_f \cdot e^{-\beta}} \right)^2$$  \hspace{1cm} (3.11)$$

Finally, when $t_{ri} = t_{fi} = 0$, the results converge to the expression found in Chapter 2 for the zero rise and fall times case (2.24).

$$P_{(b)} \bigg|_{t_r = t_f = 0} = I_0^2 \frac{1}{C_i} \cdot \frac{(1+e^{-\beta})}{(1-e^{-\beta})}$$  \hspace{1cm} (3.12)$$

\[\text{Fig. 3.4: Detailed waveforms of the PC mode ($T_i = R_iC_i$): Upper trace: voltage $\Delta V_i$ across resistance $R_i$ and the switch $S$; Lower trace: current through the capacitor, according to the notations in Fig. 3.2.}\]
C. The effect of the switching process when \( T_i \ll R_i C_i \) No Charge – “NC” mode

In this region, the current waveform is of a trapezoidal shape (Fig. 3.3c), whereas \( \Delta V_i \) is practically constant. The loss for this case was evaluated by applying the Taylor series expansion to calculate the boundary value of (3.10) when \( \beta_i \ll 1 \):

\[
P_{(c)_i} = t_0^2 \left( k_i \frac{R_i}{f_s \left( \frac{t_{ri}}{2} + t_{on_i} + \frac{t_{fi}}{2} \right)} \right)
\]

(3.13)

The total power loss for the symmetrical 1:1 converter is thus:

\[
P_{(c)} = t_0^2 \left( \frac{2R}{f_s \left( \frac{t_f}{2} + t_{on} + \frac{t_f}{2} \right)} \right)
\]

(3.14)

Here again the finite rise and fall times increase the losses. In the limiting case, when \( t_r = t_f = 0 \) and \( t_{on1} = t_{on2} = 1/2 T_s \), (3.14) reduces to the asymptotic expression of (2.41), and for the unity gain SCC of Fig. 3.1 the limit value equals \( 4R \), as expected [29, 31, 51, 64, 66, 83].

3.3. Experimental study

The analytical derivations outlined above were verified with experiments that were carried out on an SCC similar to the one described in Fig. 3.1, which included adjustable transition times (rise time, “on” time and fall time of the switches). Breadboard parameters were: \( V_{in} = 10V \), \( S_{1,2} – \text{IRF540} \), total switch ON resistance was adjusted to 750mΩ by adding a series resistor, \( R_O = 11.9Ω \), switching frequency of 5 to 150kHz, \( C_O = 470μF \) with \( R_{ESR} = 44mΩ \) (for the simulation assumed to be zero), flying capacitor \( C = 22μF \) with \( R_{ESR} = 100mΩ \) and switch rise/fall times of 50ns to 10μs. The switch in the discharging phase of the converter was driven so as to achieve a slow rise time, and the charging phase was not controlled. Gate signals and flying capacitor current for the NC mode (\( T_i \ll R_i C_i \), \( f_S = 150kHz \)) are shown in Fig. 3.5. Two current waveforms are shown for the CC mode (\( T_i \gg R_i C_i \), \( f_S = 5kHz \)). Fig. 3.6a shows the case of fast rise time of both phases with an output voltage of 5.63V. Fig. 3.6b shows the case of a significantly slower rise time in the discharge phase when the output voltage is still 5.63V, as predicted in Section 3.2.A. A comparison of experimental and calculated output voltage values is presented in Fig. 3.7. Experimental points for both fast and slow rise times coincide with the calculated values. As expected, the rise time had no impact on the losses in the CC mode – that was obtained at lower frequencies. At higher frequencies, which induced the PC and NC modes, the impact of rise time becomes more significant, increasing the losses and lowering the output voltage as the frequency goes.
up. Because of experimental limitations, the gate voltage included a dead time (Fig. 3.5, lower trace), which also increased the losses owed to the higher RMS current for a given average current. The contribution of the dead time, however, is much smaller than that of the rise and fall time.

![Fig. 3.5](image1)

**Fig. 3.5**: Experimental waveforms in the NC mode, $T_i \ll R_i C_i$, $f_s = 150\text{kHz}$: Upper trace – $S_2$ gate signal, discharging switch; Middle trace – $S_1$ gate signal, charging switch; Lower trace - Flying capacitor current.

![Fig. 3.6](image2)

**Fig. 3.6**: Flying capacitor current waveforms in CC mode with a different rise time in the discharge phase: (a) Fast rise time, $V_O = 5.63\text{V}$; (b) Slow rise time, $V_O = 5.63\text{V}$. 

Chapter 3 - Switching losses
3.4. DISCUSSION AND CONCLUSIONS

The results of this work - that were verified by simulations and experiments - clearly show that in the PC and NC modes the current rise and fall times increase the SCC losses. The additional loss phenomenon can be explained by the fact that the finite transitions reduce the effective current conduction. Hence, for the same average current, the RMS current will be higher, which results in increased losses. This loss increase needs to be taken into account in the design of SCC systems running at high switching frequencies. For the sake of brevity and clarity, the expressions for power loss were developed here in relation to the unity gain 1:1 SCC. Nonetheless, the proposed analytical approach can be applied to derive the losses of multi-capacitor and multi-phase systems [15, 16, 51, 57, 83], as well as in SCC-based DC to AC or AC to AC converters [89, 95, 96], if each of the SCC subcircuits can be described or approximated by a first-order RC system [51, 83].
Chapter 4  Dynamic analysis

4.1. INTRODUCTION

SCC, or “charge pumps,” are preferred in a number of cases because of their IC compatibility, relatively small size, and the absence of magnetic elements. SCC can be modeled as a network that is configured by the switches to a set of subcircuits that charge and discharge flying capacitors. The average behavior of SCC systems analysis, similarly to that carried out in Chapter 2, was performed in numerous earlier studies (e.g. [20, 25, 26, 30, 31, 34, 36, 83, 97, 98]), in which the expressions of the voltage transfer ratios and the expected losses were derived.

The objective of this work was to develop an average model of SCC systems that would be compatible with any circuit simulator and would be capable of reproducing not only the static, but also the dynamic behavior of the converter including the small-signal control-to-output transfer function. The proposed simulation model is in fact a translation of the analytical results of Chapter 2 [51, 83] into average equivalent circuits. That being so, the accuracy of the model is identical to the fundamental results of Chapter 2 and it is limited by the assumptions of its derivation (such that the subcircuits can be represented or approximated by a first-order RC circuit). As experienced in the case of switched inductor converters, average circuit simulation [58, 99-101] could alleviate convergence problems and provide additional information and a better insight into the simulated converter.

4.2. BASIC THEORETICAL CONSIDERATIONS

For the sake of clarity and brevity, we consider first a 1:1 unity gain SCC system as depicted in Fig. 4.1. The converter includes a flying capacitor $C_f$, with a loss component, ESR, two switches $S_1$ and $S_2$ with “on” resistances of $R_{s1}$ and $R_{s2}$ respectively, an output filter capacitor $C_o$ with ESR$_o$ and load resistance $R_o$. As the switches run at a frequency of $f_s$, the circuit toggles between two subcircuits: one during $T_1$, when $S_1$ is “on,” and the other during $T_2$, when $S_2$ is “on.”

![Fig. 4.1: A unity gain 1:1 SCC.](image)

Chapter 4 - Dynamic analysis
Each of the subcircuits can be represented by a generic charging circuit (Fig. 4.2) that includes a voltage source $\Delta V_i$ (where $i = 1$ for duration $T_1$ and 2 for $T_2$) a resistor $R_i$ and a capacitor $C_i$ with an initial condition of zero voltage [51, 83]. $\Delta V_i$ is the initial voltage difference between the capacitor and the input voltage (for $T_1$) or the output voltage (for $T_2$) just before the relevant switch is turned on. For the 1:1 converter the values are summarized in (2.22). Once a switch is turned on, the equivalent capacitor will start charging (by a positive or negative $\Delta V_i$) and a current $i_i(t)$ will build up. Depending on the relationship between the duration $T_i$ and the time constant $R_iC_i$, the current can take one of three possible shapes. For $T_i \gg R_iC_i$, the charging will be completed within $T_i$ (Fig. 2.14a); this case is denoted as CC. For $T_i \approx R_iC_i$, the charging will be partial (PC, Fig. 2.14b). For $T_i << R_iC_i$ there will be no effective charging (NC) and the current will be practically constant (Fig. 2.14c). In this latter case, the capacitor voltage will stay about constant within $T_i$ [51, 57].

As was shown in Chapter 2, the average power $P_{Ri}$ dissipated by a given subcircuit $i$ during a switching phase duration $T_i$ can be expressed as a function of the average current $I_{avi}$ in the subcircuit, (2.9), averaged over the switching period $T_s=1/f_s$. Part of this power dissipation term represents the equivalent resistance $R_{ei}$ of subcircuit $i$ (2.10).

In the light of these results, the average behavior of the instantaneous equivalent circuit (Fig. 4.2), for duration $T_i$ can be represented by a generic average equivalent subcircuit (Fig. 4.3), in which all the variables are average values (averaged over the switching period): $V_{C_{avi}}$ is the value of the capacitor voltage during the time frame $T_i$, $I_{avi}$ is the average current in the subcircuit, calculated by integrating the charge transferred in the $i^{th}$ subcircuit during $T_i$, and divided by the full switching period $T_s$, $R_{ei}$ is the equivalent resistance of subcircuit $i$, as per (2.10), and $C_i$ is the total capacitance of subcircuit $i$. 

![Fig. 4.2: The generic instantaneous capacitor-charging equivalent circuit.](image)

![Fig. 4.3: Generic average equivalent subcircuit.](image)
It should be noted that, consistently with the conventional assumption of average models, $V_{C_{av}}$ and $I_{av}$ are assumed to be constant during the switching period $T_s$. These variables, however, are still time-dependent under the normal restriction that their bandwidth is much smaller than the switching frequency of the SCC.

4.3. **THE SCC AVERAGE MODELING APPROACH**

In the light of the above observations regarding the generic average circuit behavior, one can conclude that the average current and average voltages of each subcircuit can be obtained by eliminating the switching action altogether and replacing the physical resistances with their equivalent counterparts, $R_{ei}$, for each subcircuit. The two subcircuits of the 1:1 SCC discussed here (Fig. 4.4a) can then be combined into one average circuit (Fig. 4.4b). This fusion is allowed because of the following two points. First, the average potentials of the flying capacitor $C_f$ terminals in the two subcircuits are identical. The second point is the fact that this flying capacitor connection restores the real total average current via the capacitor. That is, the capacitor is charged by subcircuit 1 and discharged by subcircuit 2. In steady state these currents are equal and the net charging/discharging current is zero. In transient or small-signal analysis the momentary charging and discharging currents may not cancel each other, which will cause the capacitor voltage to change. Hence, the average model in Fig. 4.4b not only retains the correct power dissipation of the circuit by virtue of (2.9), but also retains the dynamics of the system since the capacitors are exposed to the correct average currents that flow in the physical SCC. Considering the above the average equivalent circuit of Fig. 4.4b represents the average static and dynamic behavior of the unity gain converter of Fig. 4.1, while being transparent to the switching action.

![Diagram](image_url)

Fig. 4.4: Average equivalent circuit model of the 1:1 SCC of Fig. 4.1.
(a) Two separated subcircuits. (b) Combined subcircuits.
The average equivalent circuit (Fig. 4.4b) is linear for any given switching mode since the $R_{ei}$ values are voltage- and current-independent if $R_i$, $f_s$, and $T_i$ are kept constant (the possible change of $R_i$ when MOSFET switches are used is neglected in the present average model). The static steady-state DC values of the SCC voltage and currents can easily be obtained from the average model by simple circuit analysis or by simulation (only “Bias Point” analysis will be required). In the simple case of the unity gain SCC considered here the DC values can be obtained by inspection. At steady state the net average currents via the flying capacitor $C_f$ and the output capacitors are zero and hence:

$$I_{av_i} = I_{av_z} = I_o = I_{in} \quad (4.1)$$

This implies:

$$V_o = V_{in} \frac{R_o}{R_o + R_{ei} + R_{e2}} \quad (4.2)$$

which conforms to the classical equivalent circuit model of the SCC [51, 57, 83] that represents it as a voltage source $V_T$ ($V_T$ is the open circuit output voltage of the SCC) and an internal resistance $R_e$ (Fig. 2.1), which for the 1:1 SCC discussed here are equal to $V_T = V_{in}$ and $R_e = (R_{e1}+R_{e2})$. 

Notwithstanding the ability of the proposed model to follow the steady-state behavior of the SCC, its novelty lies in the ability to emulate the dynamic responses. Being a linear circuit, the proposed equivalent circuit model can be analyzed or simulated as is to examine the dynamic large-signal behavior at start-up and the large- and small-signal responses to input voltage or load changes. For example, a straightforward small-signal analysis can be used to yield the input ($v_{in}$) to output ($v_o$) response (audio susceptibility):

$$\frac{v_o}{v_{in}}(s) = \frac{1}{a \cdot s^2 + b \cdot s + c} \quad (4.3)$$

where the parameters $a, b$ and $c$ are:

$$a = C_f C_o R_e_1 R_e_2; \quad b = C_o (R_{e1} + R_{e2}) + C_f R_e_1 \left( \frac{R_{e2} + R_o}{R_o} \right); \quad c = \left( \frac{R_{e1} + R_{e2} + R_o}{R_o} \right) \quad (4.4)$$

An experimental validation of this transfer function is given in Section 4.6 (Model verification).

The proposed model can also be used in a simple way to evaluate the effect of a step change in the switching frequency and/or the duty cycle. This will be illustrated by considering the case of a step in switching frequency. Based on (2.10) a step in $f_s$ will cause, in general, a change in the value of $R_{ei}$. This can be represented as a switched circuit in which the equivalent resistances are replaced at the instance
of the frequency change by new values (Fig. 4.5).

The large-signal response of the resulting switched equivalent circuit of Fig. 4.5 can be derived analytically or simulated by any circuit simulator. For example, in the PSpice environment the switches will be replaced by Sbreak elements that will be controlled by voltage pulse sources (VPULSE).

In the above example the proposed average model was treated as a linear circuit or a switched linear circuit. In terms of regulated SCC, the small-signal response between the control signal and the output voltage is of interest. These nonlinear relationships can be obtained by the proposed average model but require some circuit preparation as discussed next.

4.4. CONTROL-TO-OUTPUT RESPONSE

Two basic approaches can be used to regulate the output voltage of a SCC: duty cycle control [91] and frequency control [93], including frequency hopping and dithering [15] (control methods that are based on current sources that charge one or more of the flying capacitors [71-73] are beyond the scope of this work). These methods are in fact based on the control of one or more $R_{ei}$ of the subcircuits. That is, regulation is accomplished by increasing/decreasing the losses of the SCC. This stems from the observation, as discussed in many papers, e.g. [29, 30, 66], that the efficiency, $\eta$, of SCC systems is linked to target voltage, $V_T = M \cdot V_{in}$, to output, $V_o$, voltage ratio by (2.49). Hence, for a fixed $M$, output voltage regulation is accomplished by controlling the efficiency: namely, by increasing/decreasing one or more of the equivalent resistances of the SCC which are responsible for the conduction losses [66]. This can be elucidated by considering the general equivalent circuit of the SCC (Fig. 2.1), which implies that the output voltage of an SCC can be expressed as:

$$V_o = M \cdot V_{in} \cdot \frac{R_o}{R_e + R_o}$$

(4.5)

Fig. 4.5: Average model of the 1:1 SCC for simulating a step change in switching frequency. State "a" is an initial state with equivalent resistance of $R_{ei,a}$ ($i = 1, 2$), state "b" is after the frequency step with equivalent resistance of $R_{ei,b}$. 

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Equation (4.5) explicitly shows the dependence of the output voltage on $R_e$ which, in turn, is a linear function of the subcircuits’ equivalent resistance, $R_{ei}$ [51, 57, 83].

Considering (2.10), the required adjustment of the equivalent resistance of one or more of the subcircuits for regulation purposes can be carried out by changing the switching frequency $f_s$, and/or by controlling $T_i$. For example, in the case of regulation by frequency control the relationship between the subcircuits’ equivalent resistance and the switching frequency can be expressed as:

$$R_{e_i}(f_s) = \frac{1}{2f_sC_i} \cdot \frac{(1+e^{-\beta_i})}{(1-e^{-\beta_i})} = \frac{1}{2f_sC_i} \cdot \coth\left(\frac{\beta_i}{2}\right)$$

(4.6)

where $\beta_i = 1/(mf_sR_iC_i)$.

Based on the above, modeling of the large-signal control-to-output voltage response can be accomplished by emulating the equivalent resistances of the proposed model by dependent resistors. This can be conveniently realized by dependent current sources that are a function of the voltage across them, $V_R$, and a control variable, $I_G$ (Fig. 4.6), such that $I_G = V_R/r$. In this case the emulated resistance $R$ will be equal to $r$. This dependent resistance is compatible with standard circuit simulators such as SPICE-based simulator (e.g. OrCAD PSpice [Cadence design systems, Inc., ver. 16.3]) and discrete event simulator (such as PSIM [Powersim Inc., ver. 9.0]). An example of an implementation that applies the PSpice capabilities is depicted in Fig. 4.7. In this case the switching frequency is emulated by a voltage ($V \equiv f_s$, node $V_{inj}$ Fig. 4.7), which is the variable in the expression of GVALUE (4.7). A convenient emulation factor would be $1\text{Hz} = 1\text{V}$.

Fig. 4.6: Emulation of a dependent resistor by a dependent current source, $R = r$.

Fig. 4.7: Implementation of a dependent equivalent resistance in PSpice.
The expression of the GVALUE in Fig. 4.7 will thus be:

\[
\text{EXPRESSION} = \frac{\{V(\%IN^+) - V(\%IN^-)\}}{1 + e^{\frac{1}{2V(V_{inj})R_1C_1}}} \left(\frac{1}{1 - e^{\frac{1}{2V(V_{inj})R_1C_1}}}\right)
\]

(4.7)

where \(R_1, C_1\) are the total resistance and capacitance of the subcircuit “1”, \(V(\%IN^+)-V(\%IN^-)\) is the input voltage to the GVALUE, and \(V(V_{inj})\) is the voltage of node \(V_{inj}\) (Fig. 4.7).

The (static) dependence of \(V_o\) on the switching frequency \(f_s\) can be obtained by running a DC analysis on the circuit in which the DC voltage source (Switching_Frequency, Fig. 4.7) is swept over the desired range. This same schematic can also be used to simulate the output voltage response to a step change in switching frequency. The relevant analysis in this case is TRANSIENT analysis, and the excitation source that mimics the frequency change will be \(V_{\text{Pulse}}\) (Fig. 4.7).

Notwithstanding the simulation capabilities listed above, the real power of the proposed modeling approach is the ability to obtain the small-signal, control-to-output voltage response of an SCC. This response is a prerequisite for optimal design of the compensator. Since the control-to-output voltage response is in general a nonlinear function (as evident from (2.10)), analytical derivation of this function will require extensive effort using techniques such as perturbation or linearization by differentiation. A simpler and more “user friendly” approach, however, would be to apply simulation tools to extract the required small-signal responses by taking advantage of the automatic linearization algorithm embedded in the AC analysis of SPICE. No mathematical derivation will be required in this case and the circuit (Fig. 4.4b) can be run as is to obtain the small-signal response. The relevant excitation is the VAC source (AC_Source, Fig. 4.7) and the analysis will be carried out around the operating point set by the DC source (Switching_Frequency, Fig. 4.7) that emulates the switching frequency at the operating point.

PSIM users could also easily simulate the small-signal control-to-output voltage response even though this simulator does not have a linearization capability. Instead, PSIM applies time-domain analysis to obtain the small-signal response by injecting sinusoidal signals at various frequencies over the desired range. The controlled resistor can be realized in the PSIM environment by the built-in "nonlinear element" (Fig. 11) which is in fact also a controlled current source. The current of this element is \(i = v/x\), where "\(i\)" is the current thorough the element, "\(v\)" is the voltage across the element and "\(x\)" is the control parameter.

In Fig. 4.8, \(x = V_{req\_i}\) and represents the equivalent resistance of phase \(i\). This voltage is calculated
on the fly during the simulation as a function of the control parameter (frequency, or duty cycle). The calculation can be carried out in PSIM by a "Math_Block." The example in Fig. 4.8 shows the arrangement for obtaining the small-signal response in frequency control. The operating point is set by the DC voltage source "Switching_Frequency," and the "AC_Source" provides the time domain excitation at the specified frequency range. The "Math Block" expression for emulation of $R_{e1}$ as a function of variable frequency in the 1:1 inverting SCC case (Fig. 4.10) is given in (4.8), which is the implementation of (2.10) using PSIM syntax:

$$V_{req_i} = \frac{1}{2V_{Inj} \cdot C_1} \cdot \frac{1 + e^{-\frac{1}{2V_{Inj}R_{l}C_1}}} {1 - e^{-\frac{1}{2V_{Inj}R_{l}C_1}}}$$

where $V_{req_i}$ is the output voltage of the "Math_Block," and $V_{inj}$ is the input voltage to the "Math Block." The unity gain block, "K" (Fig. 4.8), is required for signal integrity within PSIM.

"AC analysis" in PSIM is carried out by specifying the range of frequencies for the "AC_Source" using the "AC Sweep" element (Fig. 4.8). The signal generated by the "AC_Source" is added to the steady-state frequency emulated by "Switching_Frequency" DC source and fed to the "Math_Block" which calculates the equivalent resistance value that is fed to the “Nonlinear Element.” The waveforms involved are depicted in Fig. 4.9. Fig. 4.9a represents the momentary frequency (coded into voltage). Fig. 4.9b is the calculated equivalent resistance and Fig. 4.9c shows the resultant effect on the output. These time-domain signals are used by PSIM to plot the “small-signal” frequency to output voltage response.

Duty cycle-dependent signals could be generated in a similar way, with the difference that the input sources will represent duty cycle rather than frequency, and the expressions in the "Math Block" in PSIM, or GVALUE in PSpice will be a function of the duty cycle rather than frequency.
It should be pointed out that the small-signal responses could be obtained in PSIM by running it in the full switched circuit mode. That is, running the original circuit with all the switches and physical resistances. The small-signal frequency to output voltage response will be obtained in this case by modulating the switching frequency. The advantage of using the average circuit model rather than the full switched circuit is twofold. First, running time will be shorter since smaller steps would suffice. Another advantage of the average model is the transparency to the switching frequency. The full circuit will include a ripple component that might interfere with the PSIM “AC analysis.”

Experimental verifications of the small-signal responses obtained by the proposed average model are given in section 4.6 (Model verification).

4.5. Extension to more complex structures

The modeling concept outlined above can be easily extended to more complex SCC structures including multi-phase implementations as long as the subcircuits can be described or approximated by a first-order RC network [51]. Also, the model can handle SCC topologies that include diodes. This will be demonstrated by considering an inverting, two-phase 1:1 SCC (often referred to as a charge pump) (Fig. 4.10). The first modeling step, as discussed in section 4.2, is to identify the two subcircuits according to the operational phases, corresponding to the charge (i = 1, Fig. 4.11a) and the discharge (i = 2, Fig. 4.11b) durations.

Total subcircuit resistances and capacitances are calculated in Chapter 2 for both phases to be (2.36), and following (2.9) and (2.10), $\beta$-s (2.37), and equivalent resistances (2.38) are expressed.
Fig. 4.10: The demonstrated SCC (Inverting, 1:1 ratio).

Fig. 4.11: Inverting 1:1 SCC, instantaneous subcircuits: (a) Charging \((i = 1)\), (b) Discharging \((i = 2)\).

For each of the instantaneous subcircuits in Fig. 4.11 an equivalent average subcircuit is created according to Fig. 4.3, and finally these equivalent average subcircuits are connected to the complete average equivalent model circuit (Fig. 4.12). This average model is an implementation of the concepts outlined above, except that in this case there is a need to overcome the fact that the flying capacitor in the two subcircuits is indeed flying. Namely, none of its terminals share a common potential in the two circuits. This is resolved by placing the capacitor in one subcircuit and reflecting it to the other subcircuit with a “DC transformer,” which is realized by dependent sources \(E_T\) and \(G_T\) (Fig. 4.12). The relationships between currents and voltages of the “DC transformer” are given in (4.9), consistently with the notation of Fig. 4.12:

\[
\begin{bmatrix}
V_{T1} \\
I_{T1}
\end{bmatrix} = \begin{bmatrix}
n & 0 \\
0 & 1/n
\end{bmatrix} \begin{bmatrix}
V_{T2} \\
I_{T2}
\end{bmatrix}
\] (4.9)

where \(n\) is the transformation ratio between the primary and the secondary of the transformer. In the inverting 1:1 SCC (Fig. 4.10) \(n = 1\).

Fig. 4.12: Equivalent circuit-based, average model of the inverting SCC of Fig. 4.10.

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Furthermore, according to the results of Chapter 2 [51, 83], the effect of the diodes on the operation of the circuit is modeled by voltage sources $V_{D1}$ and $V_{D2}$ (Fig. 4.12). This is correct considering the fact that the proposed average model emulates the average currents in the SCC and that diode losses are a function of the average currents (assuming some equivalent average voltage across the diode while conducting). Here we neglect the incremental resistances of the diodes. The model in Fig. 4.12 is correct under the assumption $R_o >> ESR_o$ and neglects the effect of $ESR_o$ on the dynamics of the system.

The equivalent circuit of Fig. 4.12 can be used as is to simulate the large- and small-signal responses of the studied SCC. These responses can also be derived analytically by solving the state-space equations of the circuit or by Kirchhoff-Laplace equations. Analytical derivation of the control-to-output responses, however, will require extensive analytical work considering the nonlinearity of the model. Comparison of experimental results with average model simulations of this inverting 1:1 SCC is given in the next section.

4.6. Model Verification

The proposed SCC generic behavioral average circuit model was checked against full circuit simulation (Cycle-By-Cycle) carried out on two different software packages, PSIM and OrCAD PSpice, and against experimental results carried out on a laboratory breadboard. The experimental devices and parameters were as follows: Duty Cycle = 50%; Dead Time = 120ns; Input voltage $V_{in} = 12V$; Switches $S_1$ - SMU10P05, $S_2$ - SMU15N05; Flying capacitor $C_t = 22\mu F$ and $ESR = 0.1\Omega$; Output capacitor $C_o = 560\mu F$. For the inverting SCC Diodes $V_{D1}$ and $V_{D2}$ - MBR320P; and $ESR_o = 33m\Omega$ were also used. Experiments and simulations covered all operational modes: CC with $f_s = 5kHz$, PC with $f_s = 50kHz$, and NC with $f_s = 250kHz$.

Fig. 4.13 shows the input ($v_{in}$) to output ($v_o$) response (audio susceptibility) of the unity 1:1 SCC (Fig. 4.1). The figure includes the amplitude and phase responses as obtained by (1) plotting the analytical expression (4.3), which was obtained by signal analysis circuit model of Fig. 4.4, (2) results of full (switched) circuit AC analysis simulation by PSIM, and (c) experimental results. In this experimental test, higher switching noise was observed because of the reduced input capacitance, making phase readings in experiments above 1kHz erroneous. Therefore, experimental phase readings above 2kHz are omitted in Fig. 4.13.

Fig. 4.14 shows start-up transients, Fig. 4.15 depicts a load-step response, and Fig. 4.16 shows the small-signal responses of $\{v_o/f_s(f)\}$ obtained by the average model simulation and experimentally. The
small deviations of the experimental results from average model simulations are probably owed to experimental uncertainties such as errors in the exact values of the capacitances and resistances (ESR), nonlinearities, etc.

Fig. 4.13: Input ($v_{in}$) to output ($v_o$) response (audio susceptibility) of the unity SCC of Fig. 4.1. Asterisks – Full circuit simulation results; Triangles – Traces of the Average model based analytical derivation (4.3); Squares - Experimental results; Solid traces – Amplitude response; Dashed traces – Phase response.

Fig. 4.14: Start-up transients of the inverting 1:1 SCC: (a) Experimental - CC mode, (b) Full (switched circuit) simulation and model based average simulation - CC mode, (c) Experimental and average model simulation - NC mode. Please note: in (b) and (c) the traces are on top of each other.
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4.7. **Discussion and Conclusions**

The main attribute of the new modeling approach is that it is based on average modeling and that the resulting SPICE- and PSIM-compatible equivalent circuits emulate the large- and small-signal responses of the modeled SCC. The model covers all operational modes (CC, PC, and NC) and can be used to examine the effects of individual elements such as the resistance of each switch, the ESR of each capacitor, the influence of the capacitors' values and the effect of the switching frequency and duty cycle. A powerful feature of the model is its seamless compatibility with SPICE-based AC simulation in which the linearization is done by the simulator. The model is also compatible with the PSIM simulator, and similar discrete event simulators for both large- and small-signal analyses. These powerful capabilities can be used conveniently to obtain the small-signal control-to-output responses for various control methods such as duty cycle control or frequency control, or both methods combined.

Although discussed and demonstrated by a simple 1:1 SCC, the proposed modeling methodology can
be easily applied to multi-capacitor and multi-phase SCC systems such as those described in [15]. A fundamental limitation of the model is that it assumes that all subcircuits can be represented as first-order networks. This assumption leads to the closed-form solution for $R_e$ (2.10). As already demonstrated in Chapter 2 [51, 83], however, popular SCC topologies, which do not conform to the first-order requirement, can still be approximated as one, and modeled by the proposed approach. This is especially true for systems that include capacitors of the same capacitance and ESR values and switches with identical $R_{ds(on)}$.

Although this work emphasized the simulation approach, which is the fastest way to obtain final numerical results, the proposed average model is by no means restricted to this type of analysis. Once the average equivalent circuit is formulated it can be analyzed symbolically to derive the relationships of interest. This was demonstrated for the small-signal audio susceptibility transfer function (4.3). In this case, when the frequency and duty cycle are kept constant, the average equivalent circuit is linear and can be probed by any analytical technique. Considering the nonlinearity of (2.10), however, derivation of an analytical expression for the control-to-output transfer functions would require the use of some linearization techniques.

A major conclusion that emerges from the results of this study is that the average behavior of SCC systems (both static and dynamic) is a function of the equivalent resistances ($R_{ei}$) rather than the physical resistances of the SCC (ESR and $R_{ds(on)}$). In fact, based on (2.10) when $\beta_i \gg 1$ ($T_i \gg R_i C_i$, CC mode):

$$R_e \bigg|_{\beta_i \gg 1} = \frac{1}{2f_s C_i} \quad (4.10)$$

the SCC behavior will be independent of the resistive elements. On the other hand, when $\beta_i \ll 1$ ($T_i \ll R_i C_i$, NC mode) the limiting value of $R_{ei}$ will be according to (4.11),

$$R_e \bigg|_{\beta_i \ll 1} = \frac{R_i}{f_s T_i} \quad (4.11)$$

and the equivalent resistance is only a function of the resistive elements, independent of the switching frequency.

The above observation can explain the experimental and model-derived results obtained for the small-signal frequency-to-output response. As evident from the plots of Fig. 4.16, this response has a larger amplitude for the CC case (Fig. 4.16a) than for the PC case (Fig. 4.16b). This is because in the CC case the equivalent resistances are a function of $f_s$ (4.10) (Fig. 2.15), and an excitation in the switching
frequency will have a marked effect on $R_e$ and hence on the output voltage. In the NC case the equivalent resistance is independent of $f_s$ (4.11) (Fig. 2.15), and consequently the control by frequency variation will not yield any change in the output. The PC case (Fig. 4.16b), which is in between the CC and the NC cases (Fig. 2.15), will be affected by the frequency control but to a lesser degree than the case of CC. For NC operation, duty cycle control would be a good choice [92] since the equivalent resistance is a strong function of the subcircuits’ switch duration $T_i$ (4.11).

It is believed that the proposed intuitive and straightforward modeling methodology would be useful to researchers and design engineers and for educational purposes. The suggested approach can be used to gain a better understanding of SCC and charge pump behavior, to optimize the circuit and to design the control.
Chapter 5  Hybrid converters

5.1. INTRODUCTION

Hybrid converters, as referred to in this work, include a switched inductor PWM converter that is connected to an SCC [44-46]. Hybrid converters enjoy most of the advantages of the basic PWM switched inductor converters while being able to achieve much higher conversion ratios, both bucking and boosting. The major beneficial attributes of the hybrid converter are lower stress on the switches and a high total conversion gain in the CCM mode. If isolation is not required, capacitor multipliers can replace a transformer with a large-turn ratio, which exhibits significant leakage inductance and winding capacitance. These parasitic elements cause voltage and current spikes and increase losses and noise [44]. Furthermore, capacitor multipliers preclude the need for HV diodes, which normally have poorer reverse recovery characteristics. Hybrid converters are therefore good candidates for applications such as laser drivers, X-ray systems, ion pumps, electrostatic systems and many others [44]. Other applications, such as grid-connected renewable energy systems, can also benefit from the characteristics of hybrid converters. Renewable energy sources such as a single PV panel have, in general, a low output voltage, which needs to be boosted so that it is capable of injecting energy into the grid. This can be done conveniently by using hybrid converters with multiple capacitors, such as the one shown in Fig. 5.1, which is a “Boost SCCx3” with a voltage gain of six when operating in CCM at 50% duty cycle. Other examples are the converters proposed in [102, 103].

![Diagram of Hybrid Boost SCCx3 converter](image_url)

Fig. 5.1: Hybrid Boost SCCx3 converter.
Analysis of hybrid converters’ basic building blocks, the PWM and SCC, has been well addressed in numerous studies. Average analysis of PWM-based converters was developed back in the 1990s by several research groups [59, 99, 100, 104-106]. Capacitor-based power converters have also been analyzed in a number of studies during the last two decades [26, 29, 31, 38, 39, 51, 53, 54, 57, 64, 83, 85] (Chapter 2 of this work). Dynamic and static analyses of hybrid converters have only been carried out in a limited number of earlier studies, however [44, 46, 107]. The analysis in [44] derives the transfer function and the closed-form solution for the small-signal response of the three-switch high voltage converter, followed by basic extension rules. Other studies concentrated on the large-signal response of this family of converters [46]. Both of these approaches only partially cover the analysis of hybrid converters.

The objective of this work was to examine the use of average models to simulate hybrid converters based on PWM switched inductor and SCC systems that are compatible with available simulation packages and capable of reproducing the static and dynamic behavior of a converter, including the small-signal responses.

The proposed average modeling approach applies the concept of equivalent circuit models for switched inductor converters [59, 99, 100, 104-106] and SCC as developed in Chapter 2. The latter is based on the loss model described in [51, 83]. The major contribution of the research presented in this chapter, compared with previously published studies, is the fusion of two distinctive equivalent circuit models into a single equivalent circuit model, which provides a tool for evaluating hybrid converter structures. The resulting equivalent circuit model preserves the average behavior of the original nonlinear switch-mode converter, on the one hand, and, on the other hand, it is transparent to the switching action. Being a continuous analog circuit, the model can be evaluated with any network analysis method or numerical tools which include mathematical software tools and simulation software packages.

5.2. BASIC THEORETICAL CONSIDERATIONS

A. The switched inductor average model basics

Switched inductor PWM converters share a common topology-independent module (Fig. 5.2a). There are several published papers dealing with the modeling of PWM switched inductor converters [59, 99,
The model selected here is the generic switched inductor model (GSIM) (Fig. 5.2b) [59]. This model has the capability of modeling the CCM and DCM operation modes in a continuous way. For example, during simulation of the transient response the model will move seamlessly from CCM to DCM and back without the need to interrupt the simulation run and readjust the model. The GSIM includes four dependent sources that are used to interface the module with the rest of the converter. The dependent sources represent the average currents flowing into and out of the module and the dependent voltage source represents the average voltage drop applied to the inductor.

According to [59] and [106] (5.1) describes these average dependent sources:

$$
G_a = I_{Lav}; \quad G_b = \frac{I_{Lav}D_{on}}{D_{on} + D_{off}}; \quad G_c = \frac{I_{Lav}D_{off}}{D_{on} + D_{off}};
$$

$$
E_L = V_{(a,b)}D_{on} + V_{(a,c)}D_{off}
$$

where $I_{Lav}$ is the average inductor current, $V_{(a,b)}$ and $V_{(a,c)}$ are the average voltages between the points a and b and the points a and c of the GSIM (Fig. 5.2b), respectively, $D_{on} = T_{on} / T_s$ is the duty cycle, $T_s$ is the switching period and $D_{off} = 1 - D_{on}$ for the case of CCM and is given by (5.2) for the case of DCM:

$$
D_{off} = \frac{2I_{Lav}L_f_s}{V_{(a,b)}D_{on}} - D_{on}
$$

where $L$ is the inductance of the choke and $f_s = 1 / T_s$ is the switching frequency. Selection of the DCM-CCM mode can be done on the fly by calculating the two $D_{off}$ values and selecting the minimum between the DCM case, (5.2), and the CCM case, $(1 - D_{on})$ [59].

---

(a)  
![Generic switched inductor model](image)

(b)  
![Generic switched inductor model](image)

Fig. 5.2: PWM Converters (a) Common block, (b) Generic switched inductor model - GSIM.
B. SCC average model basics

The basic subcircuit of an SCC includes a flying capacitor, $C_f$, connected to its charging/discharging source, $V_s$, which could be a voltage source or another capacitor. The generic capacitor's charge/discharge process, which takes place in this SCC subcircuit, can be represented by the equivalent circuit of Fig. 2.2b, in which $\Delta V_i$ is the initial voltage difference between the capacitor and the charging/discharging voltage source of a subcircuit notated "i," $C_i$ is the total capacitance of the subcircuit $i$ and $R_i$ is the total resistance of the subcircuit $i$. It is further assumed that the capacitor is periodically charged and discharged at a frequency of $f_s$. The charge/discharge duration is $T_i$, and the charge and discharge processes are modeled as two independent subcircuits, which are analyzed separately.

The average power, $P_i$, dissipated by the subcircuit during a switching duration of $T_i$, can be expressed as a function of the average current, $I_{av_i}$, in the subcircuit (2.9), and the loss can be represented by an equivalent resistance, $R_{ei}$, of subcircuit $i$, as detailed in Chapter 2. This equivalent resistance, when included at the output of the average circuit of Fig. 2.3, will fully represent the losses during the charge/discharge process.

These results are valid for all operational modes of the SCC, i.e. when $T_i$ is larger, about equal to, or smaller than $R_iC_i$. These three situations are denoted as CC, PC, and NC, respectively. Based on these formulations, the average behavior of the instantaneous equivalent circuit for duration $T_i$ (Fig. 4.2) can be represented by a generic average equivalent subcircuit (Fig. 4.3), in which all the variables are average values as described in Chapter 4. It should be noted that each flying capacitor will appear in at least two subcircuits for an SCC with at least two phases (when charging and discharging), or in a number of subcircuits for the multi-phase SCC.

![Fig. 5.3: SCC subcircuit (a) Generic instantaneous charge/discharge circuit, (b) Generic average model.](image-url)
To form the complete model, the interconnection of the subcircuits can be carried out directly if the flying capacitor shares a common potential in all subcircuits. In other converters, such as in the case of the Boost SCCx3 circuit discussed here (Fig. 5.1), the capacitors are floating at different potentials and direct connection is impossible. This is resolved by an isolation element, a “DC transformer.” The realization of the DC transformer is explained in Chapter 4.

5.3. HYBRID CONVERTER MODELING APPROACH DEMONSTRATED BY SIMULATION IMPLEMENTATION

The fundamentals of the proposed approach are summarized by an average equivalent circuit of a hybrid converter; PWM Boost with SCC x3 multiplier (Fig. 5.1). The following sub-section A delineates the basic operational analysis of the studies topology and in sub-section B the implementation of the average modeling approach is demonstrated by simulation.

A. Basic operation principle of Boost SCCx3 multiplier

A Boost SCCx3 converter is a cascaded connection of two converters; the PWM Boost converter, encircled by the blue solid line in Fig. 5.1, and a x3 multiplier based on a switched capacitor converter, encircled by the red dashed line (Fig. 5.1). The converter is operated in two phases, according to the state of the switch “S”; phase 1 is the ON state, (Fig. 5.4a), and phase 2 is the OFF state, (Fig. 5.4b).

(1) Phase 1 begins at switch turn-on (Fig. 5.4a). The inductor current, \(I_{\text{1a}}\), rises. Flying capacitors \(C_{\text{f1}}\) and \(C_{\text{f2}}\) are charged from the output capacitors \(C_{\text{o1}}\) and \(C_{\text{o2}}\) through the diodes \(D_{\text{2}}\) and \(D_{\text{4}}\), respectively. Diodes \(D_{\text{1}}, D_{\text{3}}, \text{ and } D_{\text{5}}\) are reverse-biased. The load current, \(I_{\text{4a}}\), is supplied from the output capacitor chain \(C_{\text{o1}}-C_{\text{o3}}\).

(2) Phase 2 begins at switch turn-off (Fig. 5.4b) after the time period of \(DT_s\), where \(D\) is the duty cycle and \(T_s\) is the switching period. Capacitor \(C_{\text{o1}}\) is charged by the inductor current, \(I_{\text{lp}}\), through the diode \(D_{\text{1}}\) (regular Boost operation). Flying capacitors \(C_{\text{f1}}\) and \(C_{\text{f2}}\) charge the output capacitors \(C_{\text{o2}}\) and \(C_{\text{o3}}\) through the diodes \(D_{\text{3}}\) and \(D_{\text{5}}\), respectively. Diodes \(D_{\text{2}}\) and \(D_{\text{4}}\) are reverse-biased. In this phase, the load current, \(I_{\text{4b}}\), is also supplied from the output capacitor chain \(C_{\text{o1}}-C_{\text{o3}}\).

Neglecting the parasitics, the ideal voltage conversion ratio of the converter, \(M\), can be derived by combining the bare Boost, \(M_{\text{Boost}}\) [108], and the switched capacitor multiplier, \(M_{\text{SCC}}\) [51], conversion ratios. Full analysis, which takes into account possible voltage drops owed to the losses, can be carried out with the average model developed in the next sub-section (B).
Fig. 5.4: Hybrid Boost SCCx3 converter operational phases: (a) Phase 1 - switch is on, (b) Phase 2 - switch is off.

B. Modeling approach demonstrated by simulation implementation

The model development is demonstrated by a PSIM simulation package implementation (Powersim Inc. v. 9.0.3), as shown in Fig. 5.5. It should be noted that the proposed approach is compatible with any circuit simulator that includes dependent sources, such as PSpice, NL5, etc. The PSIM simulator was selected for demonstrating the proposed modeling approach since it is capable of simultaneously running a full circuit (cycle-by-cycle) simulation along with the small-signal (AC) analysis of the average model simulation. This facilitates side-by-side comparison of the two results. Some aspects of a PSpice implementation of SCC and GSIM average models are discussed later on in this section and more details can be found in [53, 54, 59, 106] and Chapter 4 of this work.

The module encircled in Fig. 5.5 by a solid line is the average model of the Boost section. It follows the structure of Fig. 5.2b, as configured for the Boost stage (the shorted current source, G_b, in Fig. 5.2b is absent from Fig. 5.5). For the sake of brevity, the choke, switch, and capacitors’ parasitic resistances are neglected at this point.
The SCC module (encircled by a dashed line) comprises the three serially connected capacitors ($C_{o1}$-$C_{o3}$) and the flying capacitors, $C_{f1}$ and $C_{f2}$, which are connected to the complementary subcircuits by two “DC Transformers.” The equivalent resistances, which represent the losses of each subcircuit, are implemented by the controlled resistors $R_{e1}$-$R_{e4}$. Also included in the average model are the diodes of the SCC, which were assumed to be ideal in the present case. The values of the equivalent resistors are calculated on the fly by (2.10), in which all the parameters are known except for $T_i$, which is a function of the duty cycle. The duty cycle is also the control variable of the dependent sources of the Boost section, as per (5.1) and (5.2).

In PSIM, in order to run a “small-signal” simulation, a small sinusoidal signal is used as a control signal to excite the system and the response is evaluated as the ratio of the resulting output perturbation.
to this signal for different excitation frequencies. In the demonstrated system, the excitation includes a DC component to set the operating point (DC duty cycle) plus a sinusoidal source (\(D_{AC}, D_{DC}\)) to generate the combined signal \(V_{inj}\) (Fig. 5.6). In the proposed model, the excitation signal (duty cycle perturbations) affects all dependent sources of the Boost module and all the variable resistors in the SCC module. That is, the control signals of these dependent elements are a function of the duty cycle via eqs. (5.1), (5.2) and (2.10). It is thus required that these expressions be evaluated on the fly and that the results are fed to the control port of the dependent elements. In the model presented here, the calculations are performed by mathematical blocks of PSIM, which are represented by blocks “m” in Fig. 5.6. All the constants are made accessible to the math blocks by being defined in a “Parameter File” block, whereas variables that are modified on the run are connected to the math blocks by wires. These include the current duty cycle \(V_{inj}\), the average current of the inductor \(I_{Lav}\), and the voltages \(V_a\), \(V_b\), and \(V_c\). These are then used to calculate the current control signals of the dependent elements, \(G_a, G_b, G_c, Req_1\_cal, Req_2\_cal,\) and \(Req_3\_cal\) (Fig. 5.5). This means the duty cycle excitation will affect all dependent elements in order to emulate the behavior of the physical system. Clearly, the model shows only the average values of the variables and is transparent to the switching duty cycle. Nonetheless, in the PSIM environment, “small-signal” analysis is carried out in the time domain and the frequency-dependent data are gathered by carrying out the analysis for specified signal frequencies and then displaying the result in a conventional small-signal response plot.

Fig. 5.6: PSIM implementation of the average control model.
The PSIM example given above represents an implementation of the proposed modeling approach in the discrete event simulator environment, which lacks the option of small-signal (AC) analysis. SPICE-based simulators such as OrCAD PSpice that include AC analysis have a built-in linearization procedure that converts a nonlinear system, such as the one discussed here, to its linearly approximated circuit around the operating point [106]. The implementations of the proposed average model in SPICE-based simulators follow the procedure shown above, with two exceptions: 1. the excitation will be a (phasor) AC source and 2. the analysis will be an AC analysis that includes the linearization preprocessing by the simulator, which is a procedure that is transparent to the user. The equivalent circuit model of the Boost SCCx3 will be similar to that in Fig. 5.5, with some minor changes as discussed in Chapter 4.

5.4. EXPERIMENTAL AND SIMULATION MODEL VALIDATION

The dynamic average modeling approach of hybrid PWM SCC systems was verified by cycle-by-cycle (full, switched circuit) simulation and experimental results. The Boost SCC x3 converter of Fig. 5.1 was selected as a representative hybrid PWM SCC system. Simulations were carried out on the PSIM package, and experimental trials on a Boost SCCx3 laboratory prototype. It should be noted that the “cycle-by-cycle simulation” referred to here means the simulation on the full switched circuit described in Fig. 5.1, as opposed to the “average model simulation” that means a model calculation based on the average circuit of Fig. 5.5.

To address the different operation modes of the hybrid converter, two sets of experiments were carried out. The first was the evaluation of the converter in the “Continuous Conduction Mode” of the Boost part, and the “No Charge” operation mode of the SCC part (CCM-NC) [51, 57]. In this case, the experimental prototype parameters, which were also used in the simulations and average model calculations, were as follows: input voltage, \( V_{in} = 9.61 \text{V} \), switching frequency, \( f_s = 105.6 \text{kHz} \), large-signal (operation point) duty cycle, \( D = 48.2\% \), small-signal (injection) duty cycle, \( d_{AC} = 0.17\% \), main inductor, \( L = 2\text{mH} \) and load resistance, \( R_{out} = 500\Omega \).

The second evaluation of the converter was in the “Discontinuous Conduction Mode” of the Boost part and the “Complete Charge” operation mode of the SCC part (DCM-CC). Experimental prototype parameters for this case, which were also used in the simulations and average model calculations, were as follows: input voltage, \( V_{in} = 10\text{V} \), switching frequency, \( f_s = 15\text{kHz} \), large-signal (operation point) duty cycle, \( D = 50\% \), small-signal (injection) duty cycle, \( d_{AC} = 0.1\% \), main inductor, \( L = 312\mu\text{H} \) and load resistance, \( R_{out} = 1\text{k}\Omega \).
The common parameters for both prototypes were the MOSFETs ($R_{ds,on}$ is assumed to be zero in simulation trials), IRF540, all the capacitors (electrolytic), $C = 100\mu F$, ESR of all the capacitors, 225m$\Omega$ and all the diodes (assumed to be ideal for the simulation trials), MUR420.

The steady-state output voltage values obtained by simulation and experimentally were as follows. For the CCM-NC operation modes: average model simulation 54.3V, full cycle-by-cycle simulation 54.3V and experimental results 50.9V. For the DCM-CC operation mode: average model simulation 67.9V, full cycle-by-cycle simulation 67.9V and experimental results 65.1V.

The AC response of the laboratory prototype Boost SCCx3 converter was measured by a network analyzer (Core Technology Group, Model: SA-10). The results for the CCM-NC operation mode are presented in Fig. 5.7a, and the results for DCM-CC operation mode are presented in Fig. 5.7b. Experimental data were compared with the average model calculation and with cycle-by-cycle simulation results (Fig. 5.8) for the CCM-NC operation mode, and (Fig. 5.9) for the DCM-CC operation mode. These results represent the control-to-output response, ($v_o/d(f)$), of the Boost SCCx3 system. Some mismatches, such as a lower steady-state voltage, more heavily damped response in the experimental response.

![Amplitude and Phase](image)

**Fig. 5.7:** Experimental results of the control-to-output response of a Boost SCCx3 hybrid converter: (a) CCM-NC operation mode, (b) DCM-CC operation mode.
Fig. 5.8: Control-to-output response of Boost only and hybrid converter operated in CCM-NC mode: (a) Amplitude response; (I) Hybrid: “X” experimental, “O” cycle-by-cycle simulation, “-” average model; (II) Boost only: “Δ” cycle-by-cycle simulation, “-” average model, (b) Phase response of hybrid converter: “X” experimental, “O” cycle-by-cycle simulation, “-” average model.

results and the phase lag of the experimental system at lower frequencies, as observed in Fig. 5.8, are owed to the omission of the switch and inductor loss components in the present discussion. The distortion of the results at frequencies below 1Hz in Fig. 5.7b is owed to the input band-pass filter of the network analyzer that has a cut-off frequency of 0.5Hz.

5.5. DISCUSSION

The average circuit model presented in this work is an extension of previously published average models of switch mode systems. As such, the model is compatible with CCM and DCM operation modes and capable of seamless sweeping between them, as is the GSIM model it is based on [59]. It is compatible with all operational modes of SCC - CC, PC, and NC [51, 53, 54, 57]. The model provides an insight into the operation of hybrid converters and can be used to analyze the effects of circuit parameters such
as values of the components in the static and dynamic responses. The proposed modeling methodology could be useful to researchers and design engineers and for educational purposes. The average model can help in the optimization of hybrid converters and, particularly, in their control in order to achieve desired regulations. Furthermore, the model can be used to delineate the contribution of each section to the total response. For example, the plots in Fig. 5.8 can be used conveniently to investigate the difference between the dynamic responses of the bare Boost, the SCC, and the total hybrid system. With the proposed model, the impact of capacitors’ ESR on the output voltage can be evaluated (Fig. 5.10) in a fast and easy way. It should be noted, however, that the average model of SCC, as developed in Chapter 2, assumes that flying capacitors’ charge/discharge path is, or can be approximated by, a first-order RC circuit. In the present analysis, this approximation is satisfied when the impedance of the output capacitor chain \(C_{o1}-C_{o3}\) is much lower than that of the load resistor \(R_{out}\) (Fig. 5.1).

![Amplitude response](image1.png)

![Phase response](image2.png)

**Fig. 5.9:** Control-to-output response of hybrid converter operated in DCM-CC mode: (a) Amplitude response; “X” experimental, “O” cycle-by-cycle simulation, “-” average model, (b) Phase response of hybrid converter: “X” experimental, “O” cycle-by-cycle simulation, “-” average model.
Fig. 5.10: Predicted output voltage for Boost SCCx3 operated in CCM-NC mode, as a function of duty cycle for $V_{in}=10V$: solid trace—capacitors’ ESR=50mΩ, dashed trace—capacitors’ ESR=1Ω.

A Boost SCCx3 system was selected for the experimental and simulation tests. This was in order to maintain a fair model evaluation under different conditions, in terms of gain achieved by the hybrid converter and of the stresses that the components of the system are exposed to compared with the bare Boost converter. The stresses in a hybrid converter (in comparison with the bare Boost converter) are somewhat released by the SCC multiplying stage. This allows selection of much more moderate components, such as switches or output capacitors that are required to withstand only one-third of the output voltage while carrying the same current. The diode in a bare Boost converter operated at a high boost ratio will be exposed to an extreme reverse recovery current because of the large input-output voltage difference. Moreover, operation at duty cycles close to unity will result in very high currents through the diode and, hence, a momentary high forward voltage. These factors will significantly reduce the overall Boost efficiency in comparison with the hybrid converter.

5.6. CONCLUSIONS

This work presents a unified behavioral average circuit model of hybrid converters. These converters include PWM-controlled switched inductors paired with SCC systems and are useful in high gain applications. An implementation of the model using current simulation software packages is proposed and demonstrated on a PSIM simulator for a Boost SCCx3 multiplier converter.

The model was found to be useful for calculating and simulating average static, dynamic, and small-signal responses of hybrid converters. The model is valid for all operation modes of the SCC and for
operation in CCM and DCM modes of switched inductor converters.

The proposed average circuit model was verified by full circuit simulations and experimentally, and good agreement was found between the results. The minor discrepancies probably appeared because this model did not take into account diode voltage drops and switch resistances. This resulted in a less damped response of the full simulation and of the model’s calculated results. It should be noted that a basic limitation of the model is the assumption that the capacitors’ charge/discharge processes could be approximated by first-order RC subcircuits (Chapter 2).
Chapter 6  Applications

6.1. HARD SWITCHED SCC OPTIMIZATION PROCEDURE

Switched capacitor converters have become very popular during the last decade. One of the main dilemmas in the design of SCC is the size of the active switches, which of course affects the cost of the converter. The classical approach of presenting SCC losses is to express their efficiency as a function of the voltage transfer ratio independent of switch resistances (2.49) [109]. Expression (2.49) might give the impression that SCC can operate with any switch resistance, contrary to the common-sense view which predicts lower efficiency when the switch resistances are large. This apparent paradox is examined in this work by theoretical analysis, simulation and experimental results, which delineate the role of switch resistance in SCC operation, and present SCC design guidelines to achieve optimal performance in terms of efficiency.

An analytical method that assists in the selection of optimal switch resistances for SCC is based on the fundamental model developed in Chapter 2. The method enables optimal SCC parameter optimization including switching frequency, capacitor sizes, and switch resistances. The proposed approach can handle two and multi-phase SCC, takes into account different capacitances and/or switch resistances which are operational in each switching phase, and considers asymmetric phase timing. The proposed analysis method is demonstrated on two representative hard switched SCC and shown to be robust and reliable.

A. SC parameter optimization method

SCC can be operated in a regulated or unregulated mode. In the case of an unregulated converter equivalent resistance, $R_e$, will be determined by the required efficiency of the SCC. In this case the lower $R_e$ the higher will be the efficiency since $R_e$ forms a voltage divider with the load (Fig. 2.1) and the efficiency will be according to (2.52). In the case of a regulated SCC, regulation is achieved by increasing $R_e$. The limiting case is when the converter is supposed to sustain a voltage equal to $V_T$ which can be accomplished only if $R_e$ is equal to zero. In some commercial SCC this limitation is overcome by multiple target voltages which cover a wide input-to-output voltage range at a higher efficiency. In such cases, the change from one target voltage to another is dependent on $R_e$. The change is carried out when the SCC can no longer sustain the required output voltage and, to remedy this, the SCC switches to
another target voltage. This of course will increase the loss according to (2.49). Hence, in the regulated case, \( R_e \) determines in fact the maximum efficiency that the SCC will have over the input/output voltage ratio range. It is thus evident that the \( R_e \) will be set in each case by the required specifications and desired performance of the SCC. Once the \( R_e \) is set, the required switch resistance can be determined as discussed in the following.

As an example, we consider a case of a divide by two SCC (Fig. 6.1) and assume that the required specifications are according to Table 6.I. The worst case is clearly when the input voltage is at its minimum (4V) and the output power is at its maximum (1W). For this case \( V_T \) is 2V and the required output is 1.8V and the maximum current is 550mA. This implies that \( R_e \) should not exceed 0.36\( \Omega \) (Fig. 6.2).

![Fig. 6.1: Divide by two SCC.](image)

![Fig. 6.2: Equivalent circuit of divide by two SCC.](image)

**TABLE 6.I - DESIGN EXAMPLE: SYSTEM REQUIREMENTS**

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range ( V_{in} )</td>
<td>4 to 5.5VDC</td>
</tr>
<tr>
<td>Output voltage (minimum) ( V_o )</td>
<td>1.8VDC</td>
</tr>
<tr>
<td>Nominal output Power</td>
<td>1W</td>
</tr>
<tr>
<td>Switching frequency range</td>
<td>50 to 150kHz</td>
</tr>
<tr>
<td>Switching capacitor range ( C_f )</td>
<td>0.1 to 22( \mu )F</td>
</tr>
</tbody>
</table>
Assuming a large enough output capacitor, equal time intervals for each sub-circuit, and n = 2 sub-circuits (charge and discharge), the equivalent resistance takes the following form:

\[ R_e = \sum_i (R_{e,i}) = \frac{1}{4} \frac{1}{f_s C_f} \cdot \coth \left( \frac{\beta}{2} \right); \quad \beta = \frac{1}{2f_s C_f (2R_s + ESR)} \]  \hspace{1cm} (6.1)

This relationship is plotted in Fig. 6.3 as a function of R_i - the total resistance of phase i, (ESR+2R_s) in our case) with \((f_s C_f)\) as a parameter. By drawing a horizontal line at the required value of R_e (0.36\,\Omega in this example) one can identify the various combinations of \((f_s C_f)\) and R_i that are possible. For example, selecting the \((f_s C_f)\) product of 0.7 will compel the use of switches of maximum 0.17\,\Omega. On the other hand, selecting a larger capacitor or higher frequency and enlarging the \((f_s C_f)\) product will permit the use of smaller and hence lower cost switches with higher resistance of around 0.36\,\Omega.

**B. Simulation and experimental study**

To illustrate the proposed design method, an inverting SCC presented in Chapter 2 is considered (Fig. 2.11), with target requirements as summarized in Table 6.II.

For this topology \(k = 1\), and assuming equal charge and discharge time periods \((t_1 = t_2 = 1/(2f_s))\), the expression for \(R_e\) takes the form of (2.39), and its parameters are summarized in (2.37). The required minimum equivalent resistance value, per the system requirements as summarized in Table 6.II, was calculated by (2.39) and by taking into account diode voltage drop, [51, 83], to be 1.92 \,\Omega.

![Fig. 6.3: \(R_e\) as a function of \(R_i\) with \((f_s C_f)\) as a parameter.](image-url)
Switches $S_1$ and $S_2$ could be chosen to be of different resistances when, for example, P-Channel MOSFET for $S_1$ and N-Channel MOSFET for $S_2$ are used. To illustrate the design steps for different switch resistances, we analyze the equivalent resistances for each phase, i.e. capacitor charge and discharge processes separately, and then accumulate the results to the total equivalent resistance (Fig. 2.3). The expressions for the equivalent resistance of the charge - $R_{e1}$ and discharge - $R_{e2}$ phases are summarized in (2.38), with parameters presented in (2.36) and (2.37). Fig. 6.4 presents the equivalent resistances $R_{e1}$ and $R_{e2}$ as a function of real resistances $R_1$ and $R_2$ for different ($f_sC_f$) values. Once ($f_sC_f$) is chosen, $R_1$ and $R_2$ can be selected such that the sum of $R_{e1}$ and $R_{e2}$ will be equal to the required $R_e$ (1.92Ω in this example).

For the experimental design a ($f_sC_f$) value of 2.2 was selected, which translates into 22μF capacitor ($C_f$) at 100kHz switching frequency. $R_1$ and $R_2$ were chosen to be 0.6 and 0.4Ω, resulting in $R_{e1}$ and $R_{e2}$

![Figure 6.4: $R_e$ as a function of $R_s$ and ESR for (a) charge and (b) discharge phases.](image-url)

### Table 6.II - Experimental System Parameters and Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage $V_{in}$</td>
<td>12 to 14VDC</td>
</tr>
<tr>
<td>Output voltage amplitude $V_o$ (not lower than)</td>
<td>10VDC</td>
</tr>
<tr>
<td>Nominal output power</td>
<td>~ 10W</td>
</tr>
<tr>
<td>Nominal switching frequency</td>
<td>100kHz</td>
</tr>
<tr>
<td>Switching capacitor selection range $C_1$</td>
<td>0.1 to 100μF</td>
</tr>
<tr>
<td>Duty cycle</td>
<td>~ 50%</td>
</tr>
<tr>
<td>Dead time</td>
<td>150ns</td>
</tr>
<tr>
<td>Approximate diode voltage drop $V_d$</td>
<td>0.35V</td>
</tr>
<tr>
<td>$C_o$</td>
<td>470μF</td>
</tr>
</tbody>
</table>

Fig. 6.4: $R_e$ as a function of $R_s$ and ESR for (a) charge and (b) discharge phases.
$R_{c2}$ of 1.2 and 0.8Ω respectively (Fig. 6.4), which brings the total equivalent resistance - $R_e$ to comply with the requirement of approximately 2Ω. Switch resistances $R_{s1} \approx 0.5\Omega$ and $R_{s2} \approx 0.3\Omega$ were found by subtracting the ESR value, $ESR = 0.085\Omega$ according to (2.36) from $R_1$ and $R_2$.

The proposed design was evaluated mathematically, simulated in PSIM ver. 7.0.5, and tested experimentally on a breadboard with the following components: switches $S_1$ - SMU10P05, $S_2$ - SMU15N05 with 0.28 and 0.1Ω respectively at room temperature, diodes $V_{D1}$ and $V_{D2}$ - MBR320P, with forward voltage drop of approximately 0.35V at room temperature and nominal converter current. The results are summarized in Table 6.III. The comparison of experimental results and theoretical predictions under nominal load and switch resistance ratio between P-channel and N-channel of 3.5:1 respectively and switching-phase loop resistances $R_1$ and $R_2$ ratio of 1.5:1 are presented in Fig. 6.5. Stars in the figure represent experimental operating points of the converter. N-channel resistance - $R_{s2}$ was measured to be around 0.2Ω and P-channel resistance - $R_{s1}$ around 0.55Ω, the major difference between these values from datasheet specifications is the operation temperature of the switches under nominal load.

Fig. 6.5: Experimental waveforms.

### Table 6.III - Mathematical, Simulation and Experimental results

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Theoretical ($R_e$ based)</th>
<th>PSIM Simulation (Cycle-by-cycle)</th>
<th>Experimental (Measurements)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_e$</td>
<td>$</td>
<td>V_o</td>
<td>$</td>
</tr>
<tr>
<td>12Ω</td>
<td>10V</td>
<td>10.1V</td>
<td>9.9V</td>
</tr>
<tr>
<td>20Ω</td>
<td>10.6V</td>
<td>10.65V</td>
<td>10.64V</td>
</tr>
<tr>
<td>30Ω</td>
<td>10.92V</td>
<td>10.95V</td>
<td>10.87V</td>
</tr>
<tr>
<td>50Ω</td>
<td>11.18V</td>
<td>11.2V</td>
<td>11.14V</td>
</tr>
<tr>
<td>100Ω</td>
<td>11.39V</td>
<td>11.39V</td>
<td>11.36V</td>
</tr>
</tbody>
</table>

Chapter 6 - Applications
C. Conclusions

Design guidelines and rules for selection of the hard switched SCC components were proposed. The direct dependence between switch resistances and the equivalent resistance of SCC was emphasized, and the apparent paradox that stems from (2.49) was clarified.

Two SCC topologies were analyzed mathematically and by simulation and a breadboard SCC was build and tested experimentally to verify the theoretical conjectures. The mathematical analysis predictions were found to be in good agreement with simulation and experimental results.

6.2. APPLICATION OF THE MODELING APPROACH FOR DESIGNING PV PANELS EQUALIZING SCC

One of the recently emerging applications for SMPS is PV panel energy-harvesting. Full or partial shading of PV panels, which are part of a serially connected array, limits the power that can be extracted from the installation [110, 111]. One of the ways to restore the power is to introduce a parallel converter to each pair of adjacent panels in the chain, such that the panel with the lower insolation and consequently lower current will be replenished by its neighbors. In this approach the maximum power point (MPP) tracking (MPPT) is done by a centralized unit, which also interfaces the energy to the grid [112-114]. The equalization and MPPT functionality could be per module or on a sub-module level, such as shown in [115]. Some other approaches to equalize the panels are based on the centralized low voltage bus [116, 117]. In this case each of the PV modules, or sub-modules of the PV are connected to an isolated bidirectional DC-DC converter, which in turn is tied to a common low voltage bus, and fulfills the function of MPPT per module/sub-module. The excessive power is transferred to the low voltage bus, and then redistributed between the PV panels according to the power/shading level.

The control of the equalizing converter is a rather complicated task. It can, however, be significantly simplified by approximation. Approximating the variation of PV element MPP voltage to be negligible for different insolation levels, and the MPP voltage has a broad peak, so some minor deviations from MPP voltage will have minimal impact on the output power [118, 119]. To summarize, the major task of the equalizing converter is to equalize the voltages of the adjacent panels.

Adjacent panel equalization has been previously tackled in [120, 121] with a Buck-Boost inductor-based converter. In this work, an alternative approach using a resonant switched capacitor converter was investigated. SCC is an excellent candidate for voltage equalization, since the expected efficiency is high when the input and output voltages are close to each other (2.49) [51, 53, 54, 57, 66, 83, 94]. Selection of operation mode, evaluation of expected losses, and design guidelines are presented below.
A. Selection of operation mode

As shown in Chapter 2 and further in Chapter 4 the SCC can be represented by an average model consisting of a DC Transformer with series-equivalent resistances, $R_{e1}$ and $R_{e2}$, that represent the losses during the charging and discharging phases (Fig. 6.6). The equivalent resistance is a convenient parameter of the SCC since it relates the losses to the average current passing through the converter rather than to the instantaneous currents during charging and discharging. That is, the conduction losses can be calculated by $(I_{av})^2 R_e$, where $I_{av}$ is the average current at the output (or input in case of a unity gain SCC). In the case of EQSCC, $I_{av}$ is the differential current, $I_{D_{avg}}$ that flows through the converter as a part of current replenishing process of the shaded panel.

For the hard switched SCC, the total equivalent resistance can be expressed as [51, 57, 83]:

$$R_e = R_{e1} + R_{e2} = \frac{1}{2f_s C_f} \cdot \coth \left( \frac{\beta_1}{2} \right) + \frac{1}{2f_s C_f} \cdot \coth \left( \frac{\beta_2}{2} \right) ; \quad \beta_i = \frac{T_i}{C_f \cdot R_i}$$

(6.2)

The value of the equivalent resistance, which will determine the SCC loss, depends on the operational mode of the SCC, namely, the shape of the charging/discharging current (Fig. 2.14). The lowest possible value of equivalent resistance is achieved in the NC mode, as can be seen in the plot of normalized equivalent resistance ($R_{ei}^* = R_{ei} / R_i$) for a single subcircuit of a unity gain SCC as a function of beta (Fig. 2.15). In this case $\beta_i << 1$, i.e. the switching time is very short compared with the SCC subcircuit.

Fig. 6.6: Average model of an EQSCC connected to two PV panels.
time constant. Since in this case the average and RMS currents are nearly equal (Fig. 2.14c), the losses are the lowest possible. The other limit is the CC operation mode (Fig. 2.15). In this mode the equivalent resistance is frequency-dependent and increases with the increase of $\beta_i$. This mode is much less efficient, because of the exponential, spike-like nature of the current, which flows in the SCC subcircuits (Fig. 2.14a). It is thus evident that from the power loss perspective, NC operation is preferred since it ensures the lowest possible $R_e$. Operating in the deep NC mode ($\beta_i \ll 1$) is undesirable, however, since it requires either very large capacitors or very high switching frequencies with no added value. In fact, the optimal operating point is $\beta_i = 1$, for which $1 / 2f_iC_i = R_i$. At this operating point, $R_e$ is very close to its minimum value ($R_e \approx 4.3R_i$ for the unity gain SCC), and the figure of merit $f_sC_i$ is at its lowest. High switching frequency can thus be selected to reduce the size of the capacitor. High switching frequency has its own downside, however, which is an increase in switching losses that will increase the effective $R_e$. Other issues that need to be taken into account are that smaller capacitors may not have the low enough ESR required to achieve the power loss goal and that operating at high frequency may induce resonant, rather than exponential, currents because of parasitic leakage inductances. Resonant currents that are synchronized to the switching frequency are beneficial since they offer low losses and ZCS operation.

The resonant operation mode is induced when the charging/discharging paths include inductors, which can be either intentionally inserted or simply parasitic. Soft switching (ZCS) is achieved when the “on” time of each subcircuit matches the half period of the resonant current. In this case, the charging/discharging capacitor current will be of a sinusoidal nature. The equivalent resistance of a unity gain SCC operating in this mode is (2.27), with the parameters given in (2.25) [51, 83].

The minimum equivalent resistance value of $R_{ei} \approx (\pi^2R_i/4)$ is achieved for ($Q > 3$) [51, 83], and hence the minimum achievable equivalent resistance for unity gain SCC is approximately $5R$, where $R$ is the loop resistance of each subcircuit (assumed to be equal).

Fig. 6.7 presents the dependence of the normalized equivalent resistance ($R_{ei}^* = R_{ei} / R_i$) of a single RLC subcircuit on the quality factor. It is assumed in this plot that the switching period matches the damped resonance frequency. It is evident that quality factors higher than three (Fig. 6.7, point B) do not contribute to any further reduction of the equivalent resistance. Furthermore, once the loop resistance and switching frequency are set, higher $Q$s call for larger inductors and are thus undesirable. Very low quality factors, below 0.8, result in higher equivalent resistances and, consequently, higher
losses. Hence, the optimal operation point is between the two limits and around $Q_i \approx 1$ (Fig. 6.7, point A). At this value, the equivalent resistance and consequently the losses are very close to their minimum possible value.

It should be mentioned that although operation in the soft switching mode is preferable, because of the lower switching losses, an inductor is required to maintain a desired quality factor. This requirement enlarges and complicates the system unless sufficient inductance is already present in the system’s components, layout, and interconnections (which was the case in the present work). Another issue to consider is the control implementation. Efficient operation in soft switching mode requires precise turn-off when the current reaches zero. This can be achieved either by inserting diodes to block the oscillation in the reverse direction, which will result in additional diode conduction losses, or by employing zero current sensing for control.

**B. Selection of component values**

As in any other design case, the selection of the components’ values for the soft switched SCC is not definitive but, rather, has some degrees of freedom. We suggest selecting first the desired switching frequency, $f_s$, taking into consideration the rise and fall times of the switches as well as gate drive losses. Considering the fact that the conduction losses of the soft switched SCC are linearly proportional to the loop resistance, it is obvious that the loop resistance must be as small as possible. This loop resistance, $R_l$, comprises the total $R_{ds(on)}$ in the loop plus total ESR of capacitors. As pointed out above, for $Q \geq 1$, $R_e \approx 5R_l$ and, therefore, $5R_l \approx P_{\text{loss(max)}}/(I_{D\text{max}}^2)$, where $P_{\text{loss(max)}}$ is the maximum power that the system is
allowed to dissipate at the maximum average differential current $I_{D(\text{max})}$. This equation can thus form the basis for the selection of $R_i$ once a decision has been made regarding the acceptable limit of power loss.

In the next step, the value of the inductance is set by assuming the lowest quality factor, $Q$, that will still ensure soft switching, i.e. $Q \approx 1$. Since $Q = \omega_0 L / R_i \approx 2\pi f_s L / R_i$ this would lead to the smallest possible inductor, given the fact that the switching frequency and $R_i$ have already been selected. The inductance of the resonant inductor can then be calculated from $L = R_i / 2\pi f_s$. Alternatively, if leakage inductance is to be used, its value should be estimated or measured. The leakage inductance must be larger than $R_i / 2\pi f_s$ since otherwise the switching frequency will need to be increased or extra inductance will need to be added in order to keep $Q$ around one. Once the value of $L$ has been selected and assuming that the bus capacitors are much larger than the flying capacitor, $C$ is calculated from:

$$C = \frac{1}{4 \cdot \pi^2 f_s^2 L} \quad (6.3)$$

Commercial capacitors then need to be chosen and their ESR evaluated against the set loop resistance $R_i$. The capacitors’ ESR needs to be smaller than $R_i$ and the difference is the allowable total switch resistances, $R_{\text{ds(on)}}$, in the loop. If this condition does not occur, the design goal needs to be achieved iteratively after adjustment of the switching frequency or the allowable power dissipation.

C. Experimental validation and conclusions

The experimental results were obtained with one EQSCC that was interfaced with two serially connected PV panels (Sharp NU-185W). The soft switching operation is evident in Fig. 6.8 that shows the capacitor current for a differential current of 2A. The equivalent resistance of the EQSCC was obtained by measuring $I_D$ and $V_2$ (Fig. 6.6), and was found to be close to 1Ω, as predicted by the design.

![Fig. 6.8: Experimental current of the flying capacitor in the EQSCC prototype. $I_D = 2A$, horizontal scale is 2μS/div., vertical scale is 2A/div.](image_url)
Experimentally measured losses of the soft switched EQSCC were found to be about 6.23W for a 2.63A differential current, which agrees well with the design objective of the experimental unit. As detailed in section 6.2.A, the losses can be reduced by lowering the total loop resistance, for example by using ceramic capacitors, which will eventually increase the overall efficiency. Considering the fact that the operation can be in the soft switching mode, the switching losses are minimal, and the conduction losses should be comparable to those found in similar approaches that use switched inductor-based equalizers [114].
Chapter 7 Conclusions

In this work a fundamental and unique modeling approach for conduction losses, switch transition losses, and dynamic response of switched capacitor and hybrid converters was developed. The model is unified, covers both soft and hard switched SCC, and provides a closed-form solution for complete range of SCC operations (CC, PC, and NC). Experimental and numerical simulation-based validation of the model was carried out. Based on a fundamental model, practical design methods and application examples are presented.

The key contributions of this work are as follows:

**Generic and fundamental average SCC model.** This model is generic and unified. In comparison with previously available models it unifies the analysis for all switched capacitor-based converters, including hard and soft switched SCC. An important feature of the proposed model is that it is based on the average capacitors’ currents, rather than on the instantaneous voltage differences. This enables a systematic procedure for modeling multi-level, multi-phase, multi-capacitor SCC, and hybrid (including switched inductor and switched capacitor) systems. Moreover, since average capacitor currents are linearly proportional to the output current, the losses are expressed as a function of output current. This feature presents a fair common measure to evaluate converters' performance in terms of efficiency, either between the SCC themselves or between SCC and switched inductor-based converters.

Another important feature of the model is the modular evaluation of the losses according to the switching phases. Since the losses of each subcircuit are evaluated independently, the contribution of each subcircuit to the converter behavior is rendered clear and intuitive. This could help to optimize SCC designs by trimming the fundamental parameters that affect the losses and dynamic response.

**Definition and closed-form solution of conduction losses for all three operation modes of hard switched SCC (complete charge, partial charge, and no charge).** This distinction between the different operation modes is key to understanding and evaluating SCC conduction losses. Compared with previous works, which dealt with either of the operation modes or presented an approximate solution, this derivation is a closed solution of SCC losses, and is valid for all three operation modes namely CC, PC, and NC. Following the theoretical analysis and experimental tests, it can be concluded that for optimal design in terms of minimum losses and price, it is advisable to target the PC operation mode as the operation point of SCC systems.
**Analysis of SCC switching losses.** SCC losses associated with switch transitions, which hitherto were not considered in SCC, were evaluated in this work, and approximate solutions found for all operation modes (CC, PC, and NC). It was found that switch transitions add to the losses while SCC is operated in PC and NC modes. This loss increase needs to be taken into account in the SCC designs running at high switching frequencies. Switch transitions have no impact on the converter losses, however, as long as the SCC is operated in CC mode.

**Dynamic average SCC circuit model.** The dynamic average circuit model will enable SCC investigators and designers to evaluate the static, large- and small-signal responses of SCC and hybrid systems. These capabilities were not previously tapped, and this dynamic model is unique. A powerful feature of the model is its seamless compatibility with SPICE-based AC simulation in which the linearization is done by the simulator. The model is also compatible with the PSIM simulator and similar discrete event simulators. Although this work emphasizes the simulation approach, which is the fastest way of obtaining final numerical results, the proposed average model is by no means restricted to this type of analysis. Once the average equivalent circuit is formulated it can be analyzed symbolically to derive the relationships of interest.

A major conclusion that can be drawn from the results of this study is that the average behavior of SCC systems (both static and dynamic) is a function of the equivalent resistances rather than the physical resistances of the SCC (ESR and $R_{ds(on)}$). Therefore, this study in general, and the closed solution for equivalent resistance particularly, plays an important role in our understanding of SCC behavior.

**To summarize,** a fundamental limitation of the model needs to be mentioned. It is assumed that all SCC subcircuits can be represented as first-order networks. This assumption leads to a closed-form solution for equivalent resistance. As shown in Chapter 2, however, in many practical systems even when the subcircuits are not of the first order they can be approximated as such.

It is believed that the proposed intuitive and straightforward modeling methodology could be useful to researchers, design engineers, and for educational purposes. The suggested approach can be used to gain a better understanding of SCC and charge pump behavior, to optimize the circuit and to design the control.
Bibliography

Bibliography


Bibliography


Bibliography
A significant feature of the model is the expression of the losses as a function of the mean currents through the cables. Since these currents are linear with the current out, the final expression of the losses is a function of a simple parameter, the current output, and not of a complex parameter, the difference in voltage between the cables, as was done in previous works.

Besides the losses, the additional question raised in this section is the dynamic response of the section. Accurate information on the system's response in an open loop is crucial for planning a control system for a converter, and for closing the feedback loop with success. To meet this need, a common model has been developed that not only replaces successfully the average behavior of a converter with a cable, but also, because it is a common model, it is transparent to the high-frequency process of the loop.

An analysis can be performed on the common model in any conventional way for electrical network analysis. For the latter, you can run a simulation on the common model using numerical software. A significant feature of the model that was developed is its genericity. The model works for converters that work in environments without soft switching, as a stand-alone converter cable, and as a part of a hybrid system. A hybrid system is a system composed of both a converter with a cable and a converter without a cable. The compatibility for hybrid systems was tested by examining a hybrid converter made of a converter with a cable—BOOST—connected to a converter without a cable.

Theoretical calculations were tested against numerical simulations in the program PSIM. By means of an experimental program, several working schemes were examined, including CCM and DCM of the part based on a cable converter, and different types of current loads of the part based on a cable converter. The theoretical results were found to match those obtained via numerical simulation and experimental (on the converter “living”).

The model developed in this work can be used to study the effects of various parameters of the converter, or of the hybrid, such as switching frequency and cycle ratio, on the expected losses, and/or on the dynamic response (small/large signal), the operating losses, the soft switching, and the current/voltage performance.

Keywords: converter cables, resonant converter, induction, converter 
DC-DC, common model, dynamic response,
תקציר

토폴וגיות, הפסדים, רישוםם במעופים מבני כבל מתמת

מאת

מיכאל יבצלמן

המחלקה להנדסת חשמל ומחשבים
אוניברסיטת בן-גוריון בנגב

ممירים מצוינים למימוש על שבב. בנוסף, השיפורים הטכנולוגיים האחרונים בייצור קבלים וממתגים קידמו את משפחת ממירי קבלים ממותגים לשמש ביישומים להספק בינוני אף הספק גבוה יחסית. יחד עם זאת, ולמרות היתרונות הבולטים, ממירי קבלים ממותגים סובלים מבעיה בסיסית חמורה, והיא הפסדים אנרגיה כתוצאה מתהליך טעינה ופריקה של קבל. בעיה בסיסית זו, והשלכותיה על עולם ממירים מבוססי קבל מתמת, הינה הנושא שנוח調べ במהלך עבודת המחקר הנוכחית.

כתוצאה מכך, פותחה שיטת מידול הפסדים גנרטית של ממירים מבוססי קבל מופעל בחוג פנים. השיטה המוצעת הינה ייחודית, ומכסה גם את הממירים המתפקדים בשיטת מיתוג רך, וגם את אלו המתפקדים ללא מיתוג רך. השיטה הינה פונדמנטלית, שלוקחת בחשבון הן את הפסדים והן את הפסדים של מיתוג, ותואמת רשתות מיתוג המורכבים של MOSFETים וממתגים המתאפיינים במפל מתח בזמן ההולכה, כמו דיודות, או התקנים בפולריים. השיטה, והמודל נבחנו בסימולציה ובאופן ניסיוני, והداولו נמצאו כטובים מאוד, התוצאות התיאורטיות עוקבות אחר הניסיוניות והן שהתקבלו בסימולציה.
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העבודה נעשתה בהדרכת
פרופ' שמואל בן-יעקב
במחלקה להנדסת והנדסת חשמל
בפקולטה למדעי הנדסה
טופולוגיות, המשלים, ויישומים בממירים מבוססי קבל מתמת

מחק ל(units) מילויlek פקיה של החידשות לקבוצת חוכר "דוקטור לפילוסופיה"

מנת

מייכל יבלום

חותש לשירות יזימה ברסיטית בגוריוון בנגב

אישור המנהלים

פרופסור שמואל בן-יעקוב

פרופסור הוגו גוטרמן

אישור דיקן בית הספר ללימודי מחקר מתכדמים ע"ש קרייטמן

يوم שישי, 3 בספטמבר 2013