EFFICIENT POWER DELIVERY AND VOLUME REDUCTION OF SWITCHED-MODE CONVERTERS IC

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE MSc. DEGREE

By: Eli Abramov

Supervised by:
Dr. Mor Mordechai Peretz
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October 2016
העברת ספק ייעול והקטנת ממירים של ממירים

ממחזנים על שבב

חורר וגמיה של מטורניר של קבוצת חוג אחר

נואת: אלי אברמוב

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October 2016
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תקציר

העבודה עוסקת בממירים ממוזערים בעלי נצילות גבוהה במעגלים משולבים עבור מגוון רחב של אפליקציות, על ידי ביצוע אופטימיזציות ברמת השער והארכיטקטורה, תוך הדגשת היתרונות של שילוב ממירים אלה בדור העתיד של ספקי כוח על שבב. העבודה מתמקדת בעיקר בצריכת שטח הסיליקון של ספקי כוח על שבב, בעיה אשר מגבילה את יכולת המזעור והאינטגרציה של המערכות הללו. המטרה העיקרית של העבודה היא להקטין את הממדים של מערכות ספק על שבב ולהפוך את עיבוד האנרגיה של ממירי האנרגיה. ייצור וחלוקה של מספר רמות מתח בצייד על גבי שבב, הן בהיבט השטח והן בהיבט החשמלי, זהו צעד SUPER דרכו לעבר הטכנולוגיות העתידיות של מערכות ממיריות לעיבוד הספק בתאגידים גבוהים מאוד, תוך קבלת צפיפות זרם אופטימלית למקום מטר רבוע.

אחת המטרות של העבודה היא לפתח שיטה תכנון יעילה לממירי קבלים המתאימים ל纣 חומרים על שבב. בممירי זה, העקרונות ההפכתיים במערכת, הם בתוכו של התוכןokus להפוך תכונה של למיר♋ נצילות, стоית על שבב GRSCC, עם דרגת הספק אופטימלית מציג פתרון הגיוני לגודל המערכת וה/documentation غالب על שבב, מה שמאפשר ת/drivers פשוט וזול של פתרון זה, ומעבר יותר לעבר טכנולוגית העתידית לעבר传输 הספק באינטגרציה תלת ממדית.


מטרה נוספת של העבודה היא לחקור את עקרונות האופטימיזציה ושלבי התכנון של ממיר הנקרא פיקסלי (buck) סינכרוני על שבב. במסגרת המחקר נעשו והוצגו אנליזות מפורטות של טכנולוגית TJ 0.18μm power-management ו ForeignKey של ממירحبו של שבב GRSCC, מערכות בקרה מלאה על שבב, ותוצאות מעשיות של שבב אבטיפוס שיוצר פרק זה במחקר פורסם כמאמר בכנס -IEEE Transactions on Power Electronics 2016 [3].


October 2016
הוצאות של研究报告 מתחכמות ב: שלושה פרוッシמים בנם מועדים בכנס מדעי ויוויבר בחלקון אלקטרוניקה, ופרסום בשני קנסים, הצהריים, 두 פרוッシמים בנם מועדים בכנסי ידועים בישראל, ופרסום בעיתון המודגש במעון מדעי-טכנולוגי. פרוッシום מאמר ז'ורנל ב-Transactions on Power Electronics ופרסום מאמר ז'ורנל ב-

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Abstract

This thesis addresses highly efficient and miniature power converters integrated circuit (IC) for multiple applications using architecture and circuit level optimization as well as emerging technologies. The work mainly covers the ‘real-estate’ problem of on-chip power supplies, a problem that limits the miniaturization and integration of these systems. The primary aim of this thesis is to reduce the overall volume of an on-chip power supply and to improve the energy processing of these systems. Efficient generation and distribution of multiple power supply voltages on-chip, is an extremely important step toward enabling power delivery process to provide increased current in future generation nanoscale high-performance IC, while obtaining the optimal density per sq. micron.

One objective of this thesis is to introduce an optimal design procedure for IC realization of resonant-mode switched-capacitor converters. In resonant-mode converters the dominant contributors to the total loss are the conduction loss, which can be estimated by the given implementation area, which are in proportion to the transistors’ resistances. Therefore, by optimizing the size of the transistors, the overall size of the converter, i.e. designing each device with respect to the target operating point (primarily rms current), a significant reduction of the converter size and overall system’s volume can be achieved. To reach this goal, this work presents an optimal design of a voltage regulator based gyrator resonant switched-capacitor converter (GRSCC) IC, to improve power delivery concepts for point-of-load (PoL) applications. Significant area saving highlights the benefit of the optimization method, providing a design-intuitive procedure to improve the size-efficiency factor based on the target operating conditions. Moreover, the GRSCC voltage regulator scheme with an optimized power stage demonstrates a reasonably sized solution and requires virtually no physical inductors, which making this solution simple and cost-effective, enabling smoother transition towards future 3-D power delivery approach. The research includes detailed size-efficiency analysis, behavioral description behavioral description of a GRSCC, fully monolithic control system, and experimental results of an IC prototype that has been fabricated. This part of the research has been published in the proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC) 2016 [1], and within a larger study that has been submitted to the IEEE Transactions on Power Electronics [2].

Another objective of this thesis is to study the optimization principles and design guidelines for monolithic synchronous buck converter. Within the context of this objective, detailed analysis of TJ 0.18μm power-management technology on the achievable performance of a buck IC for a target set of operating conditions has been introduced. The characteristics of MOSFET in terms of switched power devices has been explored. The outcomes of the technology analysis,
lead to gate-drive circuitry using N-type transistors only, further reducing the overall volume of the system. The research includes full efficiency analysis for a monolithic buck converter, detail the IC design considerations of an integrated power-stage for input voltage range above 10V, develop the required mixed-signal IC peripheral units (e.g. level shifting circuitry, dead-time module), and experimental results of a mixed-signal IC prototype that has been fabricated. This part of the research is a part of an extended study, introducing first of its kind a fully-integrated digital average current-mode control 12V-to-1.xV voltage regulator module, that has been submitted for presentation at the IEEE APEC 2017 [3].

In total the yields of this thesis to this date sum to: three conference publications at the most prestigious venue in the field of power electronics, two publications in the IEEE Israeli section conference, one invited talk at the most prestigious workshop for power system on-chip, and a journal publication currently in consideration for Transactions on Power Electronics.
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Acronyms and Abbreviations

IC – Integrated circuit
GRSCC – Gyrator resonant switched-capacitor converter
RSCC – Resonant switched-capacitor converter
PoL – Point of load
MOSFET – Metal oxide semiconductor field effect transistor
I/O – Input / Output
CMOS – Complementary metal oxide semiconductor
dVFS – Dynamic voltage frequency scaling
LDO – Low drop out
BJT – Bipolar junction transistor
PWM – Pulse width modulation
SiGe – Silicon Germanium
BiCMOS – Bipolar complementary metal oxide semiconductor
SCC – Switched-capacitor converter
MIM – Metal insulator metal
MOM – Metal on metal
ZCS – Zero current switching
PDM – Pulse density modulation
ASIC – Application specific integrated circuit
LDMOS – Lateral double diffused MOS
PM – Power management
HS – High-side
LS – Low-side
DUT – Device under test
BV – Breakdown voltage
RF – Radio frequency
SOA – Safe operating area

Inline References Legend

X.XX – Chapter / Section number
(X.XX) – Equation
[XX] – Reference
Fig. X.XX – Figure
Introduction

1. Introduction

1.1. IC power delivery

Before the rapid advancement of MOSFET technology, power supplies which provided current to high-performance IC were placed off-chip and connected to the IC via input/output (I/O) pins. Power supplies typically contain large passive components (inductors and capacitors), thus the size of the off-chip power supplies is large and a significant portion of the power is dissipated through the interconnections between the power supply and load circuits [4]-[10]. The power dissipated by the interconnections and I/O pins is significant when a greater number of transistor is placed on-chip, increasing the overall current demand [9]. In addition, growth of the die-size also increasing the overall consumed power[11].

Scaling CMOS has greatly lowered the power loss among the off-chip interconnect and I/O pins. Another major limitation of external power supplies is the number of dedicated power pins. Reducing the number of dedicated power and ground pins becomes of greater significance with the integration of more functional blocks onto a single IC. Additionally, power consumption is significantly reduced with the monolithic integration of the power supply. State-of-the-art of an on-chip power supply therefore implies:

1. Minimized parasitic losses since the power supply is closer to the load circuitry [4].
2. A cleaner supply voltage to the load circuitry due to the reduced parasitic impedance between the power supply and the load circuitry.
3. Reduced number of dedicated I/O pins for power and ground [11].
4. Fast line and load regulation during abrupt changes to the input voltage or output current demand [12].

The development of IC power supplies, however, is not a straightforward issue. The major limitation of on-chip power supplies is the large area requirement. Thus, area efficient IC power supply design, is the main enabler to achieve multiple integrated power supplies, generating voltages closer to the load circuits as shown in Fig. 1.1 (PoL) converter approach, while lowering parasitic losses, maintaining high efficiency and fast load regulation [12]-[16].
Introduction

Fig. 1.1  Block diagram showing typical conceptual architecture of a PoL distributed bus power system.

Continuous development in CMOS technology drives increased functionality on a single die, significantly increasing the power consumed by modern high-performance ICs. For example, over the last three decades, the power dissipated by microprocessors has significantly grown from the range of hundreds milli-Watts to the range of hundreds Watts [17]-[20]. With scaling of the minimum transistor feature size, the voltage supply has also decreased from several volts to less than 1 volt, while providing total current exceeding 10s Amps/chip [6], [9], [18]-[21].

Advances in IC technology have placed more stringent power delivery constraints at each technology generation. Delivering a high quality voltage regulation to the load circuitry has become increasingly challenging with greater power and current requirements. A high quality power supply is needed to generate the desired supply voltage connected to a power distribution network with low parasitic impedances and to effectively regulate the supply voltage to the load circuitry.

Several integrated voltage regulators topologies for high-performance ICs are reviewed in Section 1.2. Motivation, objectives and significance of the research program are discussed in Section 1.3.

1.2. IC voltage regulators

This section surveys four IC voltage regulation methodologies. Linear regulator, switched-mode converter, switched-capacitor converter, and GRSCC are discussed, respectively, in Sections 1.2.1, 1.2.2, 1.2.3, and 1.2.4. Section 1.2.3 further surveys different derivatives of switched-capacitor technology.
1.2.1. Linear voltage regulators

Linear voltage regulators approach deviates from the standard form of a simple voltage divider, these regulators are probably the most fundamental power management IC [22]-[27]. A linear regulator is a circuit that accepts a DC input voltage and produces from it a constant, well-specified lower output voltage than can be used as a supply for other circuits. They are widely used to generate high quality power supplies for sensitive analog and RF circuits due to their superb noise, output ripple, and supply rejection performance. They are also favorites in low cost low complexity applications, as they do not require an external inductor (compared to switched-mode DC-DC converters), and the circuits are relatively simple, leading to a shorter design time and lower risk associated.

Linear regulators are mainly classified as low-dropout (LDO), these topologies primarily consist of a control loop which senses the output voltage and maintains a constant output voltage within a specific tolerance regardless of its operating conditions. Fig. 1.2 shows a basic implementation of a LDO, whereas the circuit comprises of a voltage reference, an error amplifier, a power transistor and a feedback network. The dropout voltage is defined as the minimum differential voltage between input and output where the control loop stops regulating the output. The dropout voltage originates from the fact that a series pass device, a power transistor, is connected between the input and output of the regulator. The amount of dropout over the power transistor also dictates the state in which the regulator operates.

![Circuit diagram of a basic LDO voltage regulator with a PMOS pass device.](image)

The feedback network senses the output voltage, delivering a fraction of it to the error amplifier input. The error amplifier compares the voltage sample to the reference and generates an error signal which is used to drive the gate of the power transistor. The output voltage of the regulator is determined by the reference voltage and ratio of the output resistors $R_1$ and $R_2$ as
\[
V_{out} = V_{ref} \left( 1 + \frac{R_1}{R_2} \right),
\]

where \( V_{ref} \) is the reference voltage usually supplied from a bandgap reference circuitry [28], [29] and \( R_1, R_2 \) are the voltage sensing resistors.

It should be noted that the output capacitor, \( C_{out} \), is generally placed off-chip. The physical dimensions of the pass device determine the maximum amount of current which the regulator can source to the load. Since the size of a transistor is directly proportional to the current, the pass device has to be relatively large in order to deliver enough current. The width and length of the channel of a MOS transistor are determined by

\[
\frac{W_g}{L_g} = \frac{2I_D}{\mu_n C_{ox} (V_{gs} - V_{th})},
\]

where \( I_D \) is the drain current, \( \mu_n \) is the mobility of electrons near the silicon surface, \( C_{ox} \) is the oxide capacitance, \( V_{gs} \) is the gate-to-source voltage, \( V_{th} \) is the threshold voltage and \( L_g, W_g \) are the gate length and width of the pass device, respectively. Typically, the width of the power transistor in LDO regulators is in scale of millimeters, while the length is kept as small as the process allows. Due to the size of the pass device, the parasitic capacitances in the transistor are relatively large. Total capacitance at the gate can be approximated by the gate-to-source capacitance

\[
C_{gs} \approx \frac{2}{3} W_g L_g C_{ox} + W_g L_{ov} C_{ox} + C_f,
\]

where \( L_{ov} \) is the overlap between the gate and the source junction and \( C_f \) is the fringing capacitance from the gate electrode to the source.

Depending on the regulator topology, the error amplifier is either directly used to control the pass device or a buffer is placed in between the amplifier and the power transistor. The purpose of the buffer is to drive the highly capacitive gate of the pass device quickly without consuming much power. Therefore, the buffer should have low output impedance characteristics and high slew-rates to charge and discharge the gate capacitance. Whether the gate is driven by the error amplifier alone or with the buffer connected, the output of the amplifier should have a wide voltage swing in order to fully open and close the pass device.

In terms of efficiency LDOs are inferior compared to their switching counterparts, which can achieve efficiencies up to 95% [23], [24], [28]. This derives from the fact that voltage drop over a power switch is lower than the voltage drop over a series power transistor [28].
Introduction

[29]. Total efficiency of a LDO is determined by the dropout voltage and the currents ratio as follows:

\[ \eta = \frac{V_{\text{out}}}{V_{\text{in}}} \frac{I_{\text{out}}}{V_{\text{in}}(I_{\text{out}} + I_{Q})} \]  

(1.4)

where \( V_{\text{in}} \) and \( V_{\text{out}} \) are input and output voltages, \( I_{Q} \) is the quiescent current and \( I_{\text{out}} \) is the load current. The quiescent current is the difference between input and output current, which does not contribute to output power [29]-[31]. Most of the quiescent current in a LDO is consumed in biasing the error amplifier and the pass device. Neglecting the power required for the control circuitry, the efficiency of the regulator can be expressed as

\[ \eta = \frac{V_{\text{out}}}{V_{\text{in}}} \]  

(1.5)

However, when the load current is small, the maximum efficiency is limited by the quiescent current. Therefore, in order to minimize power consumption during standby, the ratio \( I_{\text{out}} / (I_{\text{out}} + I_{Q}) \) should be high. Decreasing the quiescent current however results in several design challenges in terms of transient response and stability as slew rate of the amplifier degrades and bandwidth of the regulator is significantly reduced. While linear voltage regulators may be a simple method of converting a dc supply voltage to a lower dc voltage level, the low efficiency of this approach is a serious drawback in modern power management circuits. Switched-mode converters are the perfect candidate to overcome this issue.

1.2.2. Monolithoc switched-mode converters

The aforementioned efficiency issues of linear voltage regulators, has motivated the design of switched-mode converters. These converters employ semi-conductor devices that operate as switches by being completely on (CMOS-linear region, BJT-saturation region) or completely off (cutoff). Switched-mode converters can ideally approach 100% efficiency when the parasitic impedances are eliminated [23], [24]-[26]. Switching converters are therefore the most commonly used type of power supplies due to the high power efficiency characteristics. There are primarily three types of switching converters: 1) Buck (step down - discussed in detail in this subsection), 2) Boost (step up), 3) Buck-Boost (step-up or down). A typical synchronous buck converter is shown in Fig. 1.3, whereas the high-side and low side switches are implemented as PMOS and NMOS, respectively.
The low-pass LC filter removes the high frequency harmonics of the switching node \(V_{sw}\) signal from the output voltage. The size of the passive filter determines the level of suppression of the high frequency harmonics. A large enough passive filter would effectively generate a pure DC output voltage with virtually no voltage ripple, which is the high frequency noise component of the generated output voltage due to the non-ideal nature of the LC filter. The passive inductor and capacitor are generally placed off-chip due to the significant area requirement [32]-[36]. To compensate the changes in the output voltage due to sudden changes in the load current, a dedicated controller changes the duty-ratio of the switching signal controlling the drive stages.

The output voltage of a buck converter can be expressed as follows

\[
V_{out}(t) = V_{out} + V_r(t)
\]

\[
V_{out} = \frac{1}{T_s} \int_{0}^{T_s} V_{out}(t) dt = \frac{1}{T_s} \int_{0}^{t_{on}} V_{in} dt = \frac{I_{on}}{T_s} V_{in} = DV_{in},
\]

\[
D = \frac{I_{on}}{T_s}
\]

where \(V_{out}\) is the average (DC) output voltage, \(V_r\) is the output voltage ripple caused by then non-ideal low-pass filter, \(t_{on}\) is the time the switch is on, and \(T_s\) is the switching period. The dc component of the output voltage is controlled by adjusting the duty-ratio, \(D\), and will be less than or equal to the input voltage for buck topology. The amplitude of the ripple voltage depends on both the filter characteristics and the variation of the output current demand. Additionally, the amplitude of the ripple voltage becomes larger for a finite time when the output current demand changes abruptly.
Introduction

The primary issue with a fully integrated buck converter is the large silicon area of the passive filter, which directly translates to a costly process. The work in [37] describe a fully integrated buck converter where the $LC$ filter occupies $4\text{mm}^2$ ($2\text{mm} \times 2\text{mm}$), while providing 71.3% peak efficiency. Another work [38] describes a fully monolithic buck converter in SiGe BiCMOS process including an on-chip filter, which occupies an area of more than $2.5\text{mm}^2$, and exhibits a peak efficiency of 64% at 0.8A output current. The motivation of the latter work is to establishes the foundations for three dimensional (3-D) power delivery concepts [6], [39], [41] for future microprocessors, in which the PoL converter will be vertically integrated with the processor using wafer-level 3-D interconnect technologies, as depicted in Fig. 1.4. This offers a possible solution to the problems of 2-D power delivery by dramatically reducing the interconnect parasitics. By doing so, an ultimate PoL converter configuration can be achieved, by reducing the number of power pins and facilitating multiple supply voltages. It should be noted that the size of the passive $LC$ filter can be further reduced by increasing the operating switching frequency [42]-[46], however, the efficiency and total power that can be processed is limited by the dynamic power consumption at high frequencies.

![Fig. 1.4 Conceptual representation of 3-D power delivery to microprocessor using wafer-to-wafer bonding.](image)

Another approach that have been studied over the last decade to integrate the inductor on-chip, is to implement magnetic materials on silicon [47]-[49]. These techniques are, however, currently not sufficiently cost effective. Of the several issues in fully monolithic buck converters, most of the problems relate to the inductor design [50], [51]. Due to the large area requirement, cost effective multiple PoL converters on a single die are not practical with a buck converter topology.

1.2.3. Switched-capacitor converters

Another approach for IC voltage regulator is switched-capacitor converter (SCC) technology that has demonstrated superior power density over switched-inductor converters.
Introduction

[52]-[65]. The most compelling advantage of these converters is the absence of inductors. These regulators utilize non-overlapping switches to control the charge on the capacitors which transfer energy from the input to the output. Additionally, SCCs can provide either a step down or step up in the input voltage [52]-[55]. The following subsections overview several technology options for integrated capacitors and different approaches of SCC technology.

1.2.3.1. Survey of on-chip capacitors

The performance of an IC power supply is highly affected by the technology used for integrating the charge-transfer capacitors on the chip. The density of the integrated capacitors limits the output power of the converter or more particularly its power density. Moreover, the bottom plate parasitics [56]-[58] associated with the flying capacitors affects the power transfer efficiency of the converter. Thus, an overview of the existing technologies for capacitor integration in CMOS process is presented in this subsection including MOS, MIM, MOM and deep trench capacitors. The primary trade-off of implementing on-chip capacitors is between the density of the capacitors, bottom-plate parasitics on one side and the implementation cost on the other side (defined by additional processing steps for fabrication, additional number of masks, etc.) [56]-[58].

1. MOS Capacitors: for a minimum gate length of a desired technology, the gate capacitance of MOS transistors can provide a density of tens fF/μm² [56]. The main advantage of these capacitors is low cost as they do not require any additional processing steps. However, MOSCAPs are non-linear (affected by temperature variations), can require a triple well process in case of utilizing N-type transistors. Also, they have a relatively high bottom plate capacitance (~20% variation of the targeted capacitance) due to their proximity to the substrate [56], and with scaling of technology, there has been an exponential increase in static leakage due to tunneling [59].

2. MIM Capacitors: Metal-Insulator-Metal (MIM) capacitors are supported in CMOS process by using a thin dielectric between a metal layer and a special metal layer acting as the capacitor top plate. The main advantage of the MIM capacitors is relatively low bottom-plate parasitic capacitance (~1% variation of the targeted capacitance) [57] as they are typically implemented using top metal layers. In addition, MIM caps are suitable for high voltage operation (>V_{DD}) due to higher
breakdown voltage of the metal layers. However, MIM capacitors have relatively low capacitance density 1-2 fF/μm² [57].

3. MOM Capacitors: A Metal-Oxide-Metal (MOM) capacitor is based on the fringing capacitance between dense metals in CMOS process. The main advantage of MOM caps is that they do not require any additional processing steps. However, since their density is typically low, they can be used in parallel with other types to increase the overall effective capacitance density [60].

4. Deep-trench Capacitors: have excellent capacitance density (~200 fF/μm²) and low bottom plate parasitics owing to their 3-D structure [58]. They also have a higher breakdown voltage in comparison with planar capacitors that rely on ultrahigh-k dielectric materials [61]. However, deep trench capacitors are not supported in standard CMOS process and they require additional processing steps resulting in a costly process [58], [61].

1.2.3.2. Hard switched SCC

A basic step down SCC is illustrated in Fig. 1.5. Two mutually exclusive switching networks are controlled by a two phase control signal. During phase1, Q₁ is activated while Q₂ is off, and the flying capacitor C₁ is charged with the input voltage (C_{out} is the filter capacitor), as illustrated in Fig. 1.5a. During phase2, the flying capacitor discharges to the output, resulting in 1:1 voltage conversion.

![Basic 1st order switched-capacitor converter configuration and principle of operation](image)

Fig. 1.5 Basic 1st order switched-capacitor converter configuration and principle of operation: (a) charge phase, (b) discharge state.

Many variations of the SCC exist that are able to provide multiple output levels by manipulating multiple flying capacitors, alternating between parallel, series, or mixed parallel-series connections [52], [53], [62], [63]. All of these variations have optimal
efficiency at their natural discrete conversion ratios (1:1, 2:1, etc.). When the conversion ratio is not one of the topology dictated discrete values, losses must be added to achieve the desired output voltage, reducing the efficiency [67], [68].

One of the primary issues with monolithic SCCs are the switches on-resistances. Unless the switches are optimized to target operating point, the current provided to the load passes through these resistive switches during each switching cycle [66] resulting in large conduction losses. Additionally, dynamic power is dissipated by the MOSFET switches during the charge and discharge phases’ [67]. The dynamic power losses increase with wider switch transistors whereas the conduction power losses decrease with wider transistors. A tradeoff therefore exists between the dynamic and conduction power losses. The optimal width of the switch transistors occurs when the conduction and dynamic power losses are equal [67].

Another major limitation of monolithic SCCs approach is the large die area required by flying capacitors. To reduce the required size of the flying and output capacitors, switching frequency is raised to a high level, creating multiple charges and discharges. There, the switching losses significantly increase, since SCCs are operating with hard switching. To overcome the losses caused by the hard switching [68], RSCC were developed, enabling soft switching and therefore reducing the switching losses.

1.2.3.3. Soft switched SCC

In order to reduce the switching losses, operating in a resonant mode has been suggested [69]-[71]. RSCC have many similarities to SCC at the architectural level, but differ in that they use magnetic components to facilitate resonant energy transfer, as shown in Fig. 1.6. At chip-scale, RSCCs also benefit from high capacitor density available in integrated capacitors technology (discussed in detail in 1.2.3.1) [57], but leverage a small amount of magnetic energy storage to shape the transient current waveform, tune out the reactive impedance of flying capacitors, and increase utilization of the available energy density of on-chip passive components [72]. Importantly, RSCCs require only a small amount (<10nH) of high-Q inductance to achieve substantial performance benefits [6].
Introduction

Fig. 1.6  A basic resonant (2\textsuperscript{nd} order) switched-capacitor converter configuration.

Switching at exact half-resonance period, when the current crosses a zero value, creates a sinusoidal shaped current and switching can occur at zero current, namely zero current switching (ZCS), eliminating the switching losses. This feature enables the operation in high switching frequency, further reducing the components’ size. On the contrary, lower frequency operation also improves performance for longer-channel-length devices, higher voltage, and increases the viability of moderate-bottom-plate technologies such as bulk MOS capacitors.

RSCC introduces an attractive approach for an on-chip power supply, however, it is limited conversion ratio and a discrete nature. In addition, the charge delivered from the input is not equal to the one delivered to the output. This translates into an unbalanced capacitor voltage that continues to rise every cycle [73]-[75].

1.2.3.4. Multilevel SCC

Many studies demonstrated a multiphase SCC topologies producing several conversion ratios [76]-[78]. These studies have shown that the efficiency of multiple conversion ratio SCCs can be maintained effectively over a wider input voltage range than that of a single topology converter.

An effective way to realize many target voltages is the binary/Fibonacci SCC that exhibits a widely controllable conversion ratio [79]-[81]. This multi-level approach uses a number of flying capacitors with multiple connectivity options. The capacitors are switched in between the input, the output and themselves following a specific algorithm that effectively results in the output being some fraction of the input. Using only the extended binary algorithm, for example, a converter consisting of \( n \) flying capacitors can yield \( 2^{n+1} - 1 \) conversion ratios

\[
V_{\text{out}} = \frac{1}{2^n}V_{\text{in}} \quad \rightarrow \quad V_{\text{out}} = \frac{2^{n+1} - 1}{2^n}V_{\text{in}},
\]

It should be noted that a resonant multilevel configuration can be applied, the benefits of such operation have been demonstrated in [82].
Introduction

The multilevel converter shown in Fig. 1.7a includes three flying capacitors to create 19 different conversion ratios. If the SCC is of 1st order, the duty-ratio can be tweaked to achieve only minor losses, in order to achieve a full conversion range. This results in a saw tooth efficiency trace, as seen in Fig. 1.7b, giving a relatively constant efficiency.

![Multilevel Converter Diagram](image1)

Fig. 1.7 The binary/Fibonacci converter with three flying capacitors (n=3): (a) multilevel step down topology, (b) typical efficiency graph showing multiple peaks for different conversion ratios [81].

The down side of this approach is the low achievable nominal efficiency. The number of transistors that are needed is large: all transistors must be four-quadrant, demanding a total of 8 MOSFETs per flying capacitor. Furthermore, current flows through a large and varying amount of the transistors at each state, making it hard and expensive to lower the equivalent series resistance. Additionally, in terms of overall die-size, implementing multiple flying capacitors on a single die is a major limitation of multilevel SCCs.

1.2.4. Gyrator resonant switched-capacitor converter [73]

This subsection presents a recently developed resonant switched-capacitor based converter. In contrast to traditional SCCs (either resonant or regular), the new converter disengages the efficiency of the system from the voltage gain. The converter operates as a gyrator, a voltage-dependent current source, namely gyrator resonant switched-capacitor converter (GRSCC). The GRSCC maintains soft switching for the entire operation range, and exhibits bi-directional power flow with wide voltage gains.

The topology in its generic form, as depicted in Fig. 1.8, requires bi-directional switches (Q1, Q2 and Q3) that operate in synchronous/complementary action. This is required to support bi-directional and non-inverting step-up/down operations in a single configuration.
However, for more specific cases, such as unidirectional power flow and/or specific conversion types (up or down), the number of switches and the configuration complexity can be significantly reduced.

1.2.4.1. Principle of operation

The operation of the GRSCC, shown in Fig. 1.8, is described for one steady-state charge/discharge/balance cycle and is assisted by Fig. 1.9 that illustrates the capacitor voltage, $V_C$, and the resonant tank current, $I_C$, for the case of a non-unity step-up conversion. The resistors $R_S$ in Fig. 1.8 represent the parasitic resistances in each loop and are assumed to be negligibly small in the analysis for the current and voltage conversion ratios.

By turning $Q_1$ on, a charge state (S1) is initiated, which charges the flying capacitor from the input $V_1$ in a resonant manner. At zero current, $Q_1$ is turned off and $Q_2$ is turned on (state S2) and at this point the flying capacitor discharges to the output. Since the input voltage $V_1$ and the output voltage $V_2$ have different values, only a portion of the charge is delivered to the output and results in $V_C$ that is different to its voltage at the starting point of S1. This voltage difference (neglecting parasitics) equals to twice the residual voltage of the flying capacitor. By turning $Q_3$ on (S3), the resonant tank is short-circuited. This creates the required charge-balance and reverses the flying capacitor voltage polarity such that the voltage at the end of S3 equals the voltage at the beginning of S1.
Introduction

Fig. 1.8 The gyrator resonant switched-capacitor converter configuration and operation principle: (a) charge, (b) discharge, (c) balance states.

Fig. 1.9 Typical waveforms of the flying capacitor voltage and current. Circuit parameters are: $V_{in}=20\,\text{V}$, $V_o=31\,\text{V}$, $R_s=0.15\,\Omega$, $L=5.2\,\mu\text{H}$, $C=0.25\,\mu\text{F}$.

The drawbacks of resonant SCCs as described in section 1.2.3.3 is eliminated by the addition of the 3rd balancing state that causes charge balance of the capacitor. This charge-balancing state transforms this resonant SCC into a voltage-dependent current sourcing converter that, neglecting losses, is capable of accommodating any input to output voltage gain (below and above unity).
Voltage regulation may be applied by introducing a time delay between switching states, applying a delay between consecutive sequences, i.e. pulse density modulation (PDM), or by creating packets using on-off burst mode control [75], [83].

The topology of Fig. 1.8 may be extended to operate in naturally doubling and dividing configurations, i.e. shifting the peak efficiency points to $A=2$ or $A=0.5$, respectively. An attractive option that has voltage doubling properties may also be implemented as a bridge configuration as in Fig. 1.10. For the bridge configuration, the four-quadrant switches can be replaced by conventional MOSFETs, while retaining the converter characteristics.

![Fig. 1.10](image)

Integrating the GRSCC on-chip allows operation at reasonable frequencies in the range of 10MHz without sacrificing performance, further improving the power conversion efficiency.

### 1.3. Motivation, objectives and significance of the research program

Nowadays, IC power delivery is becoming increasingly complex as the function and integration density of high-performance application specific ICs (ASIC) continue to increase. Multiple, dynamically scalable supply voltages with total current exceeding $10s A/chip$ is required by high-performance ASICs. In addition to the tight voltage regulation requirements, the area-efficiency factor of the PoL converter, is of a key importance to assure the desired performance and to be considered reasonable for commercialization.

Conventional IC power delivery methods have some fundamental limitations in meeting future IC technology needs. One of the most critical problems of these power delivery architectures is the long interconnect between the power supplies to the load. The parasitic inductance resulted from the interconnections generates large di/dt noise, forcing the use of large numbers of decoupling capacitors at various locations along the power delivery path further increasing the die-size. Additionally, as the supply voltage continues to drop and the
current slew rate keeps increasing, these decoupling capacitors become a critical design constraint and cannot meet future high-performance ICs. It will be very difficult to supply multiple supply voltages, resulting in a ‘bottle-neck’ in the advancement of the technology.

The primary objectives of this research program is to devise both size and power efficient design guidelines for integrated power supplies, enabling smoother transition towards the 3-D power delivery approach (discussed in 1.2.2).

More specifically, the objectives of the research program are:

1. To develop an optimal size-efficiency design procedure for IC realization of resonant-mode SCC IC.
2. To introduce an optimization principles and design guidelines for monolithic synchronous buck converter, and to analyze the impact of TJ 0.18μm power-management technology on the achievable performance for a target set of operating conditions.

The results of this research can directly contribute to the research and advancement of an ultra-high speed power management IC, and in particular to 3-D power supply architecture concept offering several important advantages to future technology:

1. Minimum interconnect parasitic between the power supply and the load.
2. Easy generation and distribution of multiple, individually regulated supply voltages.
3. Wide control bandwidth of high-frequency monolithic converter enabling dynamically scalable voltages.
4. Significantly reduced number of power and ground pins in the stacked die package.
5. Low cost in high quantity production and high reliability due to monolithic IC interconnectivity.
2. Optimal Design for Integrated Circuits of Switched-Resonant and Resonant Switched-Capacitors Converters

This chapter introduces an optimal size-efficiency design procedure for IC realization of soft-switched switched-capacitor-type converters. The design procedure is described in-depth through a comprehensive analysis for the origin of loss in such converters that has been carried out from a sizing perspective. It is then demonstrated by two detailed design examples. Following the size-optimization procedure, this chapter details the efficiency analysis and characteristics of a gyrator resonant switched-capacitor converter (GRSCC) operating as a voltage regulator. In area-sensitive applications, the optimization method combined with the converter’s benefits present an attractive approach for better power delivery concepts for point-of-load (PoL) applications. To verify the analytical framework two sets of bridge GRSCCs prototypes have been tested. One is an on-chip bridge GRSCC that has been fabricated in 0.18μm 5V CMOS process, according to the optimization principles detailed in this study.

It has been verified through post-layout analysis and experimental measurements of the fabricated IC. The second prototype is a discrete GRSCC that is used for further validation of the theoretical framework. Neglecting the package limitations, the IC prototype operation is demonstrated with 10 MHz switching frequency, up to 3A, 4.5 W with 3V input voltage, and the efficiency is measured to be 87%. The study has been extended to survey on effects of the package on the performance. The experimental measurements of the manufactured IC have been found to be in very good agreement with the theoretical analysis and optimization process, as well as to accurately estimate the package contribution to the system performance. In addition, a fully monolithic control system to regulate the output voltage is described and implemented on-chip by an automated synthesis process and place-and route tools.

2.1. Overview

Present-day microprocessors and other high-performance ICs require an accurate, dynamically scalable supply voltage in the range of 1V and total current of 10s A/chip. In addition to the tight voltage regulation requirements, the area-efficiency factor of the Point-of-Load (PoL) converter is of key importance to assure the desired performance and to be considered reasonable for commercialization. Improvements of the area-efficiency factor of the PoL converter may enable 3-D power delivery architectures [38], [41] where the
Optimal Design for Integrated Circuits of Switched-Resonant and Resonant Switched-Capacitors Converters

The converter is integrated with the load, significantly enhancing dynamic power delivery capabilities.

Conventional approaches to reduce the total volume of VRMs are carried out by increasing the operating frequency to the 100 MHz range [38], [41], [43]-[45]. By doing so, the integration of magnetics and the decoupling capacitors is more convenient. However, the efficiency and total power that can be processed is limited by the dynamic power consumption at high frequencies. Another area saving concept can be facilitated by resonant-mode converters [46], [84], [85]. Thanks to their soft-switching features, the efficiency of the converters is not compromised when operating at high frequency.

Switched-capacitor converter (SCC) technology has demonstrated superior power density over switched-inductor converters [52]-[55], [62], [65]. However, it lacks the capability of accurate voltage regulation without the penalty of introducing losses, and its transient characteristics are limited [63], [65], [86]-[88]. A solution that overcomes these challenges is presented in [73]. There, an additional switching state has been added to balance the charge difference between the input and output rather than introducing losses for voltage regulation, creating a GRSCC that disengages the efficiency of the system from the voltage gain. Utilizing this approach allows on-chip integration and operation at reasonable frequencies in the range of 10MHz without sacrificing performance, further improving the power conversion efficiency.

In classical designs of power processing components for VRMs, the converter’s mode of operation is considered, especially the conversion ratio to optimize the peak efficiency point to the target parameters. E.g., in a high conversion-ratio buck VRM, the lower transistor of the synchronous rectifier is dominant and would be much larger in size than the top transistor to assure optimal efficiency at the target voltage. In SCC technology, which the GRSCC is based on, using existing design tools symmetrical switch resistances are assumed for all switching states [63], [65], [87]-[91]. While appropriate for most discrete-component realizations, in area-sensitive applications (and in particular IC implementations) the efficiency characteristics of a GRSCC as a voltage regulator will be on-par to other switched-inductor based candidates, since the converter is not optimized to the target operation [92]. To overcome this, the resistance per switch should be assigned to minimize the die size at the target efficiency – this has been pursued in this study.

The objective of this study is to present an optimal size-efficiency design procedure for a resonant-mode SCC IC based on the target operating point, and to detail size-optimization
Optimal Design for Integrated Circuits of Switched-Resonant and Resonant Switched-Capacitors Converters

analysis and loss characteristics of a GRSCC operating as a voltage regulator. It is a further objective of this study to present a fully monolithic GRSCC voltage regulator that is realized by simple constant on-time Pulse Density Modulation (PDM) control (Fig. 2.1). The new VR scheme with an optimized power stage demonstrates a reasonably sized solution at much lower operating frequencies and requires virtually no physical inductors, which may be found beneficial for many applications and enable smoother transition towards the 3-D power delivery approach.

Fig. 2.1 Circuit diagram of a bridge gyrator mode resonant switched-capacitor converter.

The chapter is organized as follows: 2.2 presents a generalized size-optimization analysis oriented to a desired target efficiency. Section 2.3 provides two optimized design examples and briefly surveys the GRSCC operation. Section 2.4 describes the considerations of an on-chip implementation and monolithic delay-line based constant on-time controller. Experimental validation of the optimization methodology and the GRSCC-IC prototype are provided in Section 2.5. Finally, Section 2.6 concludes the chapter.

2.2. Size efficiency analysis

The losses of power converters can be categorized in variety of ways. In the context of this study where the main focus is at zero current switching (ZCS) resonant-mode converters, the contributors to losses are divided to conduction losses, \( P_{\text{cond}} \), which are the primary loss source [89], and other residual losses, \( P_{\text{other}} \), that include gate drive on switching losses (that may exist due to switching inaccuracy etc.) [90], [91], [94]-[97]. The total sum of the losses, \( P_{\text{loss}} \), can be generally expressed as a function of the conduction losses:

\[
P_{\text{loss}} = P_{\text{cond}} + P_{\text{other}} \approx (1 + \alpha) P_{\text{cond}}.
\]

where \( \alpha < 1 \), is an estimated factor of the additional losses.
Optimal Design for Integrated Circuits of Switched-Resonant and Resonant Switched-Capacitors Converters

The conduction losses can be described by the sum of losses from each transistor $Q_i$, expressed by its on-resistance $R_{on,Q_i}$ and the rms current $I_{rms,Q_i}$:

$$P_{cond} = \sum_{i=1}^{N} P_{Q_i} = P_{Q1} + P_{Q2} + \ldots + P_{QN}$$

$$P_{Q_i} = I_{rms,Q_i}^2 R_{on,Q_i} = I_{rms,Q_i}^2 \frac{K_i}{W_i} , \quad i = 1, 2, \ldots, N \quad (2.2)$$

where $\mu$ (mobility), $C_{ox}$ (oxide capacitance), $V_{gs}$ (nominal gate-source voltage), $V_{th}$ (gate threshold voltage), and $L_g$ (gate length) are the device’s technology-dependent constants defined here as $K_i$ ($i$ is the switch’s index). $W_i$ is the gate width which determines the transistor’s resistance alongside $K_i$. Without losing generality, the analysis of this study refers to a normalized gate length $L_g$ for all devices. Then, the area can be calculated using the width parameter alone.

For a case where some of the switches carry out more current than others, it may appear that for a defined die-size an asymmetric allocation of the of the transistors’ on-resistances results in a higher efficiency from which would be obtained by a uniform on-resistance setup. In [93], it has been shown that uniform current distribution throughout the die leads to even power dissipation resulting in minimum losses. Thus, to minimize losses each transistor should be sized based on the rms current through it. It should be noted however, that in the case of components with different structure or technology properties $K_i$ are to be used (e.g. NMOS and PMOS), a design for uniform current distribution is not sufficient to achieve minimum losses. There, the sizing should take into account the technology characteristics of each device.

The die width (and area, assuming normalized length for all devices) that is formed by summation of areas for the individual switches can be expressed as:

$$\sum_{i=1}^{N} W_i = W_{total} \quad (2.3)$$

By applying the Lagrange multipliers optimization method to minimize (2.2), and using (2.3) as the optimization constraint (full details given in the Appendix), the optimal values for $W_i$ are derived:
Optimal Design for Integrated Circuits of Switched-Resonant and Resonant Switched-Capacitors Converters

\[
\frac{W_i}{W_{total}} = \frac{I_{rms,Q_i} \sqrt{K_i}}{\sum_{i=1}^{N} (I_{rms,Q_i} \sqrt{K_i})},
\]

For convenience of viewing electrical characteristics instead of geometrical ones, (2.4) can be inverted to represent the optimal resistance ratio, defined here as \(\psi_i\), for a transistor’s size with respect to the technology characteristics and rms current:

\[
\psi_i = \frac{R_{on,Q_i}}{R_{Q,\text{total}}} = \frac{W_{total}}{W_i} = \frac{\sum_{i=1}^{N} (I_{rms,Q_i} \sqrt{K_i})}{I_{rms,Q_i} \sqrt{K_i}},
\]

where \(R_{Q,\text{total}}\) is a theoretical resistance for a single transistor which consists the overall silicon width, \(W_{total}\) and can be obtained by

\[
R_{Q,\text{total}} = \frac{P_{\text{cond}}}{\sum_{i=1}^{N} (I_{rms,Q_i} \sqrt{K_i})}.
\]

Rearranging (2.5) and (2.6), the individual resistance per-transistor is obtained as a function of \(P_{\text{cond}}\):

\[
R_{on,Q_i} = \psi_i \frac{P_{\text{cond}}}{\sum_{i=1}^{N} (I_{rms,Q_i} \sqrt{K_i})}.
\]

To account for \(P_{\text{other}}\) the individual resistances given by (2.7) can be represented as a function of \(P_{\text{loss}}\), which according to (2.1) yields:

\[
R_{on,Q_i}^* = R_{on,Q_i} (1 + \alpha) = \psi_i \frac{P_{\text{loss}}}{\sum_{i=1}^{N} (I_{rms,Q_i} \sqrt{K_i})}.
\]

It should be further noted that (2.8) describes one possible practice to accommodate the effect of the non-conductive losses on the final die size. By the addition of a die portion per device that is proportional to \(\alpha\), the optimized ratio between the losses and the die size is not significantly compromised.

Using the above analysis and observations, generalized design guidelines to obtain an optimized ratio between size and losses for resonant-mode switched-capacitor converters are summarized as follows:
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a. By the vendor’s process design kit (PDK) obtain the transistors technology-dependent parameter, $K_i$.

b. Calculate the rms current through each device.

c. Use (2.5) to calculate $\psi_i$ for each transistor.

d. Set the target efficiency $\eta$ and calculate $P_{\text{loss}}$ by:

$$P_{\text{loss}} = P_{\text{out}} \left( \frac{1-\eta}{\eta} \right).$$

(2.9)

e. Using (2.8), calculate the individual silicon width $W_i^*$ per-transistor as:

$$W_i^* = \frac{K_i}{R_{\text{on,q}}^*}.$$

(2.10)

2.3. Design examples

To demonstrate the sizing method and verify its validity, two design examples are provided. In the first example, a bridge GRSCC is presented with detailed analysis followed by theoretical observations. The second design example demonstrates the strength of the optimization procedure by considering a more complex design of a multiphase resonant SCC.

2.3.1. Bridge gyrator resonant switched-capacitor converter

The GRSCC based voltage regulator, presented in [73], has evolved from the conventional soft-switched resonant SCC configuration [97]-[101]. As in the classical bridge design of a voltage dividing SCC [52], [91], [102], the topology includes four switches and a resonant tank. In addition to the classical complementary switching states, demonstrated by Fig. 2.2a and Fig. 2.2b, a third state is added which introduces a zero-voltage resonant current path (Fig. 2.2c). This state is used to balance the residual charge of the flying capacitor, i.e. restore the flying capacitor’s voltage to its original state by reversing its polarity.
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Fig. 2.2 Bridge GRSCC configuration and operation principle: (a) charge, (b) discharge, and (c) charge balancing.

The operation of the converter shown in Fig. 2.2 is described for one steady-state charge/discharge/balance cycle and is assisted by Fig. 2.3 that illustrates the capacitor voltage, $V_C$, and the resonant tank current, $I_C$, for an arbitrary case of an uneven voltage ratio. By turning $Q_1$ and $Q_3$ on, a charge state (Fig. 2.2a) is commenced, in which the resonant tank connects to $V_{in}$ while in series with $V_{out}$, resonantly charging the flying capacitor from a voltage potential of $V_{in} - V_{out}$. After a half-resonant cycle, i.e. at zero current, the switches are turned off and followed by the complementary pair, $Q_2$ and $Q_4$ (Fig. 2.2b). At this point, the resonant tank connects in parallel to the output and discharges the flying capacitor onto the potential of $V_{out}$. In this example $V_{out} > 0.5V_{in}$, so when completing the discharge state after another half-resonant cycle only a portion of the charge is delivered to the output. This results in $V_C$ that is different from its voltage at the starting point of the charge state. By turning $Q_2$, $Q_3$ on (Fig. 2.2c), the resonant tank is short-circuited. This creates the required charge-balance and reverses the flying capacitor voltage polarity such that the voltage at the end of the balance state equals the voltage at the beginning of the charge state.

Fig. 2.3 Typical waveforms of the GRSCC.

The relationship between $I_{out}$ and $V_{in}$ follows a gyrator behavior [73] and can be expressed as:

$$ I_{out} = 2V_{in}fC, $$

(2.11)
where \(f\) is the repetition frequency of the three operating states. Voltage regulation is obtained by introducing time-delay between consecutive sequences, i.e. PDM [103], [106], meaning that \(f\) can be of any value below the resonant limitation, \(f_{\text{max}}\), of:

\[
f_{\text{max}} = \left(3\pi Z C\right)^{-1}, \quad Z = \sqrt{L/C},
\]

this yields

\[
C = I_{\text{out,max}} \left/ 2V_{\text{in,min}} f_{\text{max}} \right., \quad L = \left[\left(3\pi f_{\text{max}}\right)^2 C\right]^{-1}.
\]

Assuming a relatively high ratio between the circuit’s impedance characteristic to the loop resistance (i.e., quality factor \(Q=R_{\text{loop}}/Z \gg 5\)) of the resonant network, constant output current \(I_{\text{out}}\), and neglecting the output voltage ripple, the relationship between the states’ rms currents and the average \(I_{\text{out}}\) can be expressed as

\[
\begin{align*}
I_{\text{rms,S1}} &= \left(\sqrt{A\pi R_L/4Z}\right)I_{\text{out}} \\
I_{\text{rms,S2}} &= \left|\sqrt{A\pi R_L/4Z} - \sqrt{A^{-1}\pi R_L/4Z}\right|I_{\text{out}}, \quad \left\{ A = \frac{V_{\text{out}}}{V_{\text{in}}}, \right.
\end{align*}
\]

where \(A\) is the conversion ratio and \(R_L\) is the load resistance.

Since the converter operates under ZCS conditions, to individually identify the per-transistor contribution to these losses, the rms current of the transistors can be written as a function of (2.14) as:

\[
\begin{align*}
I_{\text{rms,Q1}} &= I_{\text{rms,S1}} \\
I_{\text{rms,Q2}} &= \sqrt{I_{\text{rms,S2}}^2 + I_{\text{rms,S3}}^2} \\
I_{\text{rms,Q3}} &= \sqrt{I_{\text{rms,S1}}^2 + I_{\text{rms,S3}}^2} \\
I_{\text{rms,Q4}} &= I_{\text{rms,S2}}
\end{align*}
\]

Assuming the transistors’ on-resistances, \(R_{\text{on,Q1}}\) through \(R_{\text{on,Q4}}\), are the dominant resistances per the loop they are active, the total power losses of the converter as a function of the conversion ratio are derived by summation of the losses as follows

\[
P_{\text{loss}} = \frac{\pi R_L}{4Z} \left[\left(R_{\text{on,Q1}}+5R_{\text{on,Q2}}+5R_{\text{on,Q1}}+R_{\text{on,Q4}}\right)A + \left(2R_{\text{on,Q2}}+R_{\text{on,Q3}}+R_{\text{on,Q4}}\right)A^{-1} - 2\left(3R_{\text{on,Q2}}+2R_{\text{on,Q3}}+R_{\text{on,Q4}}\right)\right] I_{\text{out}}^2
\]

Substituting (2.7) and (2.15) into (2.16), and after some manipulations, the efficiency of the converter \(\eta\) as a function of \(A\), \(R_{\text{nom}}\) and \(\psi\) can be expressed as
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\[
\eta = \left[1 + \frac{\pi R_{\text{total}}}{4Z} \left( \left( \psi_1 + 5\psi_2 + 5\psi_3 + \psi_4 \right) A + \left( 2\psi_2 + \psi_3 + \psi_4 \right) A^{-1} - 2 \left( 3\psi_2 + 2\psi_3 + \psi_4 \right) \right) \right]^{-1}.
\] (2.17)

Fig. 2.4 Theoretical efficiency and losses curves for a bridge GRSCC. Symmetrical (dotted lines) and optimized (solid lines) partition as a function of \( A \), for various values of \( Q \): (a) efficiency, (b) \( P_{\text{loss}} \) vs. \( P_{\text{out}} \).

Fig. 2.4a shows the resulting efficiency versus conversion ratio curves of (2.17), for several cases of on-resistance selection and compares symmetrical sizing with an optimized one. Symmetrical sizing has been plotted by setting equal values for \( \psi \) in (2.17), whereas in the optimized plot the values for \( \psi \) are set per-transistor as prescribed earlier by the design guidelines. It can be observed that, near the target voltage (\( A = 0.5 \)) where charge-balance of resonant SCC is naturally obtained, the results of both sizing methods coincide. Predicted by the initial conjecture of this study, as the conversion ratio deviates from center, a significant efficiency improvement can be observed in favor of the optimized sizing method. An even more interesting view is described by the power losses factor that is depicted in Fig. 2.4b, showing the possible power saving as a result of better area distribution between the transistors. For example, in conversion ratio of 0.75, \( Q = 10 \) and output power of 10W, 0.5W of the losses can be trimmed down for the same total area.

Given a 0.18\( \mu \)m CMOS process, technology-dependent parameters are obtained to be \( K_1 \approx 8.4\text{m} \Omega \cdot \text{m} \) and \( K_2-K_4 \approx 3\text{m} \Omega \cdot \text{m} \). Based on the IC design guidelines from Section II and the above analysis, the design example is demonstrated by 0.7W GRSCC with target values of: \( V_{\text{in}} = 3.3V \), \( V_{\text{out}} = 0.7V \), \( I_{\text{out,max}} = 1A \), \( f_{\text{max}} = 10\text{MHz} \), \( \eta \approx 87\% \). The resonant network values
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are calculated as $C \approx 17\text{nF}$ and $L \approx 7\text{nH}$. The obtained required resistances $R_{\text{on},Q1}$ through $R_{\text{on},Q4}$: 75m$\Omega$, 11m$\Omega$, 15.5m$\Omega$, 12m$\Omega$, and in terms of silicon width $W_1$ through $W_4$: 112,400$\mu$m, 346,800$\mu$m, 194,300$\mu$m, 249,500$\mu$m, respectively, while the resulting total silicon width is found to be $W_{\text{total}} \approx 903,000\mu$m. Fig. 2.5 depicts an efficiency prediction for the design example. It can be observed that for the same silicon area efficiency improvement by 5% can be obtained at nominal input voltage of 3.3V. A more noticeable benefit can be viewed in terms of overall size, where $R_{\text{on}}$ symmetrical is $\approx 10\text{m}\Omega$, resulting in approximately 30% more silicon area is required to obtain the same efficiency with the symmetrical sizing.

![Fig. 2.5](image)

**Fig. 2.5**  Theoretical efficiency curves of a bridge GRSCC as a function of $V_{\text{in}}$. Symmetrical (dotted lines) and optimized (solid lines) partition, with the target parameters: $V_{\text{out}} = 0.7\text{V}$, $V_{\text{in, nom}} = 3.3\text{V}$, $I_{\text{out,max}} = 1\text{A}$, $f_{\text{max}} = 10\text{MHz}$.

An alternative view of the devices optimization is exemplified in Fig. 2.6 for specific operating conditions of the example on hand. It shows the loss breakdown per-transistor as a function of the device’s on-resistance, where the losses have been normalized to the minimal losses that can be obtained under specified operating conditions. As can be observed, for a finite area a minimum point exists per device that exactly satisfies (2.7). Summation of the minima results it the most compact as well as efficient design per given die size.

![Fig. 2.6](image)

**Fig. 2.6**  Minimum losses per die size of the bridge GRSCC's integrated devices, with the target parameters: $V_{\text{in, nom}} = 3.3\text{V}$, $V_{\text{out}} = 0.7\text{V}$, $I_{\text{out,max}} = 1\text{A}$, $f_{\text{max}} = 10\text{MHz}$. 
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2.3.2. Multiphase Fibonacci resonant SCC

A multiphase Fibonacci resonant SCC is capable of generating multiple fractional conversion ratios with Fibonacci sequence resolution [78], [95], [108]. To achieve a desired fractional conversion ratio, a specific switching sequence that interconnects the flying capacitors with summing or subtracting action to the source and the output, is applied.

To further demonstrate the effectiveness of the optimization method, an optimized Fibonacci resonant SCC is examined by simulation and compared to the results of a symmetrical Fibonacci design. The schematic configuration shown in Fig. 2.7 includes three flying capacitors and four switching states to trim down the output voltage by 3/8 times the input voltage.

Fig. 2.7 Multiphase Fibonacci resonant SCC topology. For conversion ratio of 3/8 switching sequences are: State 1: Q1, Q5, Q6, Q10 — ON, State 2: Q2, Q4, Q8, Q9 — ON, State 3: Q4, Q5, Q7, Q9 — ON, State 4: Q1, Q3, Q8, Q9 — ON.

Validation of the optimization procedure is carried out by simulation with the following target parameters: \( V_{in} = 5V \), conversion ratio of \( A=3/8 \), \( I_{out} = 1A \), \( f_{max} = 5MHz \), \( \eta = 90\% \). The flying capacitors are chosen to be 60nF and the inductor is chosen to be 10nH. The ratios between the switches’ rms currents \( \psi_1 - \psi_{10} \) were obtained by simulation, resulting in \( R_{on,Q1} \) through \( R_{on,Q10} \): 19.5mΩ, 24.5mΩ, 72mΩ, 21mΩ, 18.2mΩ, 20.3mΩ, 40.5mΩ, 23mΩ, 20.1mΩ, 20.3mΩ. It can be seen that \( R_{on,Q6} = R_{on,Q10} \approx R_{on,Q9} \), this is due to identical rms current through the devices for the targeted conversion ratio. Fig. 2.8 depicts normalized losses over various on-resistances of the devices, it can be well observed that the point of minimum losses coincides with the values that have been obtained by the sizing procedure. For a technology-dependent parameter \( K \approx 3m\Omega \cdot m \) the resulting total silicon width is found to be \( W_{total} \approx 1.2mm \). It should be further emphasized that for the same die size the resultant efficiency of a symmetrical converter is 88% with on resistances \( R_{on,Q1} - R_{on,Q10} \approx 25m\Omega \). To obtain 90% efficiency with a symmetrical partition the total silicon width that in required is 1.4mm, which is approximately 15% overhead.
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Fig. 2.8 Minimum losses per die size of a multi-phase Fibonacci resonant SCC, with the target parameters: Conversion ratio $A = 3/8$, $V_{in} = 5V$, $I_{out} = 1A$, $f = 5MHz$.

The results in Fig. 2.9 show efficiency comparison between a symmetrical and an optimized Fibonacci resonant SCC as a function of the output current $I_{out}$. It can be observed that for the same silicon area, efficiency improvement by 2% can be obtained for the target operating values, for higher output currents it further improves. Even for complex SCC design consisting of 10 transistors, by using the IC design guidelines both minimum die area and losses are achieved.

Fig. 2.9 Efficiency curves of a multi-phase Fibonacci resonant SCC as a function of the output current $I_{out}$. Symmetrical (dotted lines) and optimized (solid lines) partition, with the target parameters: $V_{out} = 0.7V$, $V_{in} = 5V$, $I_{out} = 1A$, $f = 5MHz$.

2.4. IC implementation

2.4.1. Bridge GRSCC on-chip power-stage implementation

The selection of the transistor type depends primarily on the drive configuration. Assuming a conventional ground-referenced driver and that the input voltage is limited to
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the technology voltage $V_{DD}$, a PMOS is used for $Q_1$, while NMOSs are used for $Q_2$, $Q_3$, and $Q_4$, based on the required gate-source threshold voltage to activate the transistor.

To maximize the channel width and to increase current handling capabilities of a 5V CMOS process transistor, paralleled multi-finger cells have been realized, as shown in Fig. 2.10. The size of a device with multi-finger cells is typically defined in terms of the gate boundary $W_i = N_{fi} W_g$, where $N_{fi}$ is the number of fingers for a transistor $Q_i$, and $W_g$ is the gate width for a single finger [109]. For a generic $W_g = 50\mu m$, the NMOS (PMOS) device main characteristics are: Breakdown Voltage <9V, effective area $A_{eff} = 1mm^2$ such that $R_{on} = 2.2\Omega\cdot mm^2$ ($6\Omega\cdot mm^2$). Given the PDK $W_g$ and $L_g$ constraints, an accurate and efficient quadrilateral layout of the power-stage can be applied. It should be noted that the transistors are connected via a top metal pad, resulting a relatively low parasitic resistance of the conduction and is neglected for the design.

![Fig. 2.10](image)

**Fig. 2.10** Simplified structure of a device with paralleled multiple cells.

### 2.4.2. Driver circuitry implementation

A fully integrated circuit based on buffers with the ability to drive transistors with large gate width is implemented. Buffers logic implementation is realized by logical effort technique, including a network of three custom designed buffers for each switch. The ratio between the pull-up network and the pull-down network is $\beta = 1.5$. In the context of driving power transistors, the buffers sizing should also be considered due to the relatively higher input capacitances of the buffers chain. To assure a non-distorted input gate signal, the first inverter of the chain has been matched in size to the analog input unit. Assuming that the channel length, $L_g$, is equal along the driving chain, a ratio of 5 between the inverter units has been found sufficient. The last unit has been designed with two identical inverters to
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reduce the required area. Fig. 2.11 shows in detail a sized example of a driving stage, where \( W_{g,P} = 1.5 \cdot W_{g,N} \). It should be further emphasized that the sizing characteristics such as gate capacitances are technology-dependent, which should be taken into account to assure proper drive signal.

Since the driver stage is integrated and the control signals are all ground referenced (with gate voltage swing between 0 to 5V), neither isolation nor level shifters are required. Even for a worst case scenario where \( V_{in} = V_{DD} \), the driving circuit is still functional.

![Schematic diagram of the implemented IC drive circuitry.](image)

Fig. 2.11  Schematic diagram of the implemented IC drive circuitry.

2.4.3. *Monolithic delay-line based constant on-time controller*

A fully monolithic internal controller has been designed and implemented on-chip by an automated synthesis process and place-and-route tools to regulate the output voltage. As described in [92], regulation is facilitated using a single comparator which compares the output voltage to an internal value and triggers the GRSCC when needed.

Fig. 2.12 shows the main components of the control unit. A flip-flop based state-machine synchronically dictates the active state and out of six options: The three switching states (S1-S3), two intermediate dead-time states (D2, D3) necessary to prevent shoot-through between complementary switches, and an inactivity state (S0). The state-machine is clocked by a configurable delay-line (DL), which enables an individual predefined time length for each state. Once triggered by a comparator (unmasked only at state S0 when inactive for a predefined time value), the DL is activated and triggers the state-machine to produce the required logic sequence for the GRSCC. Fig. 2.13 shows a measured experimental gate logic sequence operating at ~3MHz produced from the monolithic DL controller.
2.4.4. Package and bonding wires limitations

On-Chip interconnections ultimately connected to the board level via IC packaging. Bond wires technique is extensively used in packaging IC designs, because of it is relatively lower cost and simple implementation [110]. Bond wires usually consist of copper, aluminum, gold or silver, while each material has its own electrical and physical characteristics. The bonding is usually farther away from the substrate and therefore has less coupling and loss at high frequencies. Still, bonding wires can be a major limiting factor in IC design, in particular for high current ICs. The thin and narrow bonding wires are a significant penalty to the conduction losses. In the context of a soft-switched converter, these are the dominant contributors to efficiency reduction. Advances in power semiconductor technology further highlight the limitations of bond wires packaging technology, since the losses contribution
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by resistances and parasitics of the package and the bond wires exceed those of the silicon die [111]. To improve performance, efficiency, and reliability of power IC designs, bond-wireless alternative interconnection techniques are preferred. Among them, Die Dimensional Ball Grid Array (D³BGA), solder bump flip-chip technology, and metal post area array technology [111]-[114]. However, these technologies require high cost specialized resources and processes. It should be noted that the packaging and bonding wires implementation are beyond the scope of this study.

2.5. Experimental and post-layout verification

Following the design procedure, an IC prototype that implements the bridge GRSCC voltage regulator has been designed and fabricated in 0.18μm 5V CMOS process. To demonstrate the operation of the IC GRSCC and to verify the theoretical analysis, the post-layout design of the power-stage and driver circuitry was verified using Cadence Spectre simulator. \( R_{on} \) of the power transistors was designed to value of \( \sim 20\text{m}\Omega \) (layout shown in Fig. 2.14). The chip consists of 11-pins and connects to a resonant tank of 2.25nH, 50nF. With the ability to operate at 10MHz, the GRSCC can produce up to 4.5W (1.5V, 3A) from a 3V input. The gate signals are transmitted through an analog input unit and buffers matching network to obtain the desired drive voltage for the converter’s power-stage. As discussed in section 2.4.3, the timing controller to regulate the output voltage, was implemented by an automated synthesis process and place-and-route tools, directly from the VHDL representation.

Fig. 2.14 Chip layout 2 mm x 1.5 mm.

Fig. 2.15 shows the flying capacitor current and voltage waveforms and the gate logic signals that were obtained by cycle-by-cycle post-layout results. The system has been tested under open-loop conditions and the waveforms verify operability of the design. The
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efficiency is measured to be 87%. Operating under the above specifications, the converter IC is capable to output power up to 4W. These results are in very good agreement with the theoretically predicted efficiency of 85%-90%.

Fig. 2.15  (a) Flying capacitor voltage and current waveforms. The circuit parameters are $V_{in} = 3V$, $V_{out} = 1.5V$, $R_{on} \approx 20m\Omega$, $C = 50nF$, $L \approx 2.25nH$; and (b) gate logic signals.

The fabricated IC prototype was packaged using 24-pin 4x4mm QFN package (the design consists of 11-pins, rest of the pins are for other designs tested by the same shuttle). A chip micrograph is depicted in Fig. 2.16a. The chip connects to a resonant tank of $C = 100nF$ and $L \approx 6nH$. The inductance is realized by stray inductances by the connection and interconnections from the chip to the flying capacitor, Fig. 2.16b depicts the IC prototype on PCB.
Experimental measurements of the packaged IC converter resistances resulted in approximately 160mΩ per loop, or effective $R_{on}$ of a single transistor is ~80mΩ. A kelvin resistance measurements to cancel out the package effect resulted in resistance of 20mΩ per transistor. These measurements clearly exhibit the bond wires and package limitations as discussed in detail in section 2.4.4, in this case by four times than the target $R_{on}$.

Considering these limitations, the best-case experimental results were obtained at maximum switching frequency of 4.5 MHz producing up to 2.25W. The actual quality factor is measured to around 2 and the resulting efficiency is measured to be 67%. TABLE I summarizes the IC prototype experimental measurements. Fig. 2.17 shows open loop experimental and post-layout results of the flying capacitor current and voltage.

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>4x4 QFN - MLP</td>
</tr>
<tr>
<td>$V_{in}$</td>
<td>3 V</td>
</tr>
<tr>
<td>$R_{on}$</td>
<td>~80mΩ</td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>1.5V</td>
</tr>
<tr>
<td>$I_{out}$</td>
<td>1.5A</td>
</tr>
<tr>
<td>Off Chip resonant tank</td>
<td>6nH, 100nF</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>4.5MHz</td>
</tr>
<tr>
<td>Quality Factor $Q$</td>
<td>~2</td>
</tr>
<tr>
<td>Efficiency</td>
<td>~67%</td>
</tr>
</tbody>
</table>
Efficiency curve of the converter IC as function of $V_{in}$ is depicted in Fig. 2.18. The experiment was carried out by varying the input voltage and manually compensating with the frequency, such that the output power and the input voltage, 2.25W and 1.5V, respectively, were kept constant. The experimental measurements tightly follow the results obtained by the simulations. As can be observed, lower efficiency can be obtained for higher input voltages. This is primarily due to higher conduction losses at higher conversion ratios.

Fig. 2.19 shows the efficiency of the converter IC as a function the output current, $I_{out}$. As can be seen, in light-load operation there is a discrepancy between the experimental and simulation results from the theoretical analysis, this is due to the resonant characteristics of the three states that are not identical, which was not taken into the theoretical model analysis.

The experimental measurements also highlighted the advantage of the GRSCC operating at light loads. Even for very light load operation at 20mA, the efficiency drops only at 4% and maintains a near constant efficiency over the entire operation range, virtually identical to the normal operation mode.
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Fig. 2.18  IC GRSCC prototype efficiency as a function of input voltage, $V_{in}$, while $R_{on} \approx 80\text{mΩ}$.

Fig. 2.19  IC GRSCC prototype efficiency as a function of load current, $I_{out}$, while $R_{on} \approx 80\text{mΩ}$.

Fig. 2.20 shows post-layout efficiency results of the IC GRSCC prototype and of an optimized IC GRSCC design with the following nominal operating conditions: $V_{in} = 3.3\text{V}$, $V_{out} = 0.7\text{V}$, $I_{out} = 1\text{A}$ operating at 10MHz. The solid line shows theoretical predicted efficiency whereas the dotted markers show the post-layout outcomes. The theoretically predictions in Fig. 20 considers additional losses $P_{\text{other}}$, in addition to capacitive related losses a real-world scenario may include further losses caused by mismatches of dead-time calibration and zero-current detect circuitry [108], [115]-[117]. Thus, to cover all the possible additional losses, $P_{\text{other}}$ was taken to account as 5% of the overall losses.

Fig. 2.20a presents theoretical and post-layout efficiency results of the IC GRSCC prototype. At nominal conversion ratio $A \approx 0.21$ the efficiency is measured to be 81%, the theoretically predicted efficiency behavior is well validated by post-layout analysis. Fig. 2.20b depicts efficiency outcomes of an optimized design (comprehensive analysis presented in section 2.3.1). It can be well observed that for the same die size in the region of the target operating values, the measured efficiency of the optimized design is higher by approximately
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5% than the symmetrical design. For higher conversion ratios the dominance of the optimized design is well noticed, while a significant area saving is achieved with the optimization routine.

![Post-Layout Results vs Theoretical](image1.png)

![Post-Layout Results vs Theoretical](image2.png)

Fig. 2.20 Post-Layout efficiency results as a function of the conversion ratio $A$ with the target parameters: $V_{in} = 3.3V$, $V_{out} = 0.7V$, $I_{out} = 1A$, $f_{max} = 10MHz$. (a) IC GRSCC at symmetrical partition $R_{on} = 20m\Omega$, (b) an optimized IC GRSCC design whereas $R_{on,Q1}$ through $R_{on,Q4}$: 75m$\Omega$, 11m$\Omega$, 15.5m$\Omega$, 12m$\Omega$.

To further validate the optimization procedure, a discrete bridge GRSCC prototype has been built and tested. Following the design procedure for the target parameters: $\eta \approx 80\%$, $V_{in} = 5V$, $V_{out} = 1.5V$, $I_{out,max} = 1.8A$ operating at maximum switching frequency of 3.5MHz. By the optimization guidelines the obtained on-resistances were $R_{on,Q1} - R_{on,Q4}$: 70m$\Omega$, 25m$\Omega$, 42m$\Omega$, 28m$\Omega$. Due to a lack of variety of discrete components, the discrete bridge GRSCC prototype has been realized with the following on-resistances: 55m$\Omega$, 30m$\Omega$, 40m$\Omega$, 30m$\Omega$. Theoretical and measured efficiency curves of the prototype as a function of the conversion ratio are shown in Fig. 2.21. It can be seen that even though the switches’ on-resistances
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are not identical, but in the range of those obtained by the design procedure, the measured efficiencies are virtually identical to the theoretical analysis over wide range of operating conditions.

![Graph showing experimental vs theoretical efficiencies](image)

Fig. 2.21 Discrete bridge GRSCC prototype experimental efficiency measurements as a function of the conversion ratio \( A \) with the target parameters: \( V_{\text{in}} = 5V, I_{\text{out,max}} = 1.8A, f_{\text{max}} = 3.5\text{MHz} \). Whereas \( R_{\text{on Q1}} \) through \( R_{\text{on Q4}} : 55\text{m}\Omega, 30\text{m}\Omega, 40\text{m}\Omega, 30\text{m}\Omega \).

2.6. Conclusion

An optimal size-efficient design methodology for IC realization of resonant switched-capacitor converters has been presented, based on the target operating conditions and physical characteristics of the integrated devices. Following the size-optimization procedure, this chapter details efficiency analysis and characteristics of a bridge gyrator resonant switched-capacitor converter operating as a voltage regulator. The optimization method has been demonstrated with two design examples, and its effectiveness is experimentally verified with a fully monolithic gyrator resonant switched-capacitor converter fabricated in 0.18\( \mu \)m CMOS process. The analysis has been meticulously verified by post-layout simulations and experiments and found to be in very good agreement with the theoretical predictions. In addition, a fully monolithic control system is described and implemented on-chip by an automated synthesis process and place-and-route tools to regulate the output voltage of the converter IC.

The experimental results highlighted the significance of packaging and bonding wires limitations. Due to the additional parasitic resistances of the packaging, the experimental tests were slightly different than the targeted. For the given package limitations the obtained measurements from the manufactured converter IC are in very good agreement with the presented optimization procedure. For various conversion ratios, post-layout analysis of both
Optimal Design for Integrated Circuits of Switched-Resonant and Resonant Switched-Capacitors Converters

symmetrical and optimized GRSCC design tightly follow the theoretical predictions. To further validate the optimization method a discrete bridge GRSCC prototype has been built and tested, and the measured results well verified over a wide range of operating conditions. The experimental measurements also further strengthen the advantages of the GRSCC ability to maintain virtually constant efficiency curve for load variations, in particular when operating at light loads. At 20mA loading, the efficiency drops only at 4%. Future work direction would include packaging and wiring optimization to assure absolute certainty of final design.

Significant area saving highlights the benefit of the optimization method, providing a design-intuitive procedure to improve the size-efficiency factor based on the target operating conditions. For the same die-size by designing optimized GRSCC IC, in the region of the target operating values 5% efficiency improvement can be obtained for the fabricated IC. Furthermore, in terms of overall die-size approximately 30% less silicon area is required to obtain the same efficiency. Combined with the topology benefits, a GRSCC voltage regulation scheme presents an attractive alternative to the switch-inductor converters, in particular in area sensitive application, and establishes the foundations for better power delivery concepts for PoL applications.
3. Optimization Principles and Design Guidelines for Monolithic Synchronous Buck Converter in TJ 0.18μm Power Management

This chapter presents analytical derivation of optimum gate width of CMOS transistors to minimize losses in monolithic synchronous buck converter. Optimized width of CMOS transistors entails use of tapered inverter chain as gate driver, which can be easily incorporated along with the optimum power-stage devices to maintain maximum efficiency of buck converter over a range of output power levels. In addition, this chapter explores an alternative driver approach, using only N-type transistors in CMOS process, the gate driver maintains both low quiescent power and area consumption by emulating the complementary operation commonly employed in tapered inverter chain. High-voltage level shifting is accomplished using a bootstrap technique, with the bootstrap diode integrated on the same die. To further optimize the converter’s efficiency a programmable dead-time module implemented by pure digital means without additional custom design is also discussed and implemented. Comprehensive analysis explores the impact of TJ 0.18μm power-management (PM) technology on the achievable performance for a target set of operating conditions. A monolithic synchronous buck has been designed and fabricated, to sustain up to 18V input voltage, delivering up to 10W of output power, and operating at 1.25MHz switching frequency.

3.1. Overview

In typical on-chip power supplies, the switches of the DC-DC converters are implemented using standard IC processes such as CMOS or LDMOS (Lateral Double Diffused MOS) processes [118], [119]. CMOS transistors are typically used if the conduction current of the switches is less than several amps [93].

Most CMOS digital circuits, implemented in CMOS processes, and designed such that the width of the transistors is minimal to minimize the delay [120]-[122], thus achieving higher operating speed. For high-efficiency CMOS power switches the transistors must have high channel width ($W_g$) to channel length ($L_g$) ratio. As the minimum channel length is twice the process feature size, the channel width must be high to reduce the on-resistance of the transistor. Unlike the digital switches, power switches are realized by using several parallel transistors (multi-fingers device as discussed in 2.4.1) and the width is chosen by optimizing the conduction and switching losses of the transistors.
The main goal of this chapter is to explore an optimal implementation of a monolithic buck power-stage with the drive circuitry including programmable dead-time module (see Fig. 3.1) using TJ 0.18μm (PM) technology. A fully digital PWM controller is also implemented, but it is beyond the scope of this study [3]. In addition, based on comprehensive power loss analysis optimum device sizing is presented. Both CMOS and LDMOS devices are characterized in terms of their own resistance and device capacitance.

The rest of the chapter is organized as follows: CMOS and LDMOS switch technology overview with the addition of TJ 0.18μm PM characteristics are detailed in Section 3.2. Optimization of CMOS transistors for high efficiency monolithic buck converter is detailed in Section 3.3. The IC implementation with emphasis on the mixed-signal and power stage design are delineated in Section 3.4. Experimental verification of the buck IC is provided in Section 3.5. Section 3.6 concludes the chapter.

### 3.2. CMOS switch technology overview

Switch based circuit techniques are rising in popularity as the value of high circuit efficiency grows. Switching circuits, like any sampled data system, must operate at a frequency higher than the bandwidth of the signal being generated [123], [124]. For example in sigma-delta type converters [123], the oversampling frequency ratio may be an order of magnitude, or more. If the desired output signal has a wide bandwidth, then the desired operating frequency may be several 10’s of MHz, and possibly much higher. The following subsections briefly surveys LDMOS device characteristics and introduces detailed FET switch model and analysis.
3.2.1. LDMOS device structure

LDMOS transistor (see Fig. 3.2) is the best suited power switch for integrated circuits thanks to its faster switching time compared to bipolar transistor and its ease of integration with CMOS technology[125]. The main constraint of power LDMOS is the reduction of the specific on-state resistance ($R_O$) for a given drain-source breakdown voltage ($BV_{DSS}$). Using these devices allows a high-voltage operation for various ICs applications, since their typical breakdown voltage is higher than the standard 5V CMOS device. The drift region of the device controls the breakdown voltage and the resulted on-resistance, the tradeoff of using a LDMOS instead of a CMOS are higher input capacitance and on-resistance and mainly larger die-size [118], [119], [125]. $R_O$ and $BV_{DSS}$ are related to the silicon material, the well-known $R_O/BV_{DSS}$ tradeoff. Due to the RESURF effect [126], there is always an optimal drift doping concentration in terms of $BV_{DSS}$ depending on the drift region architecture.

Fig. 3.2  Simplified cross-sectional view of a single-finger N-channel LDMOS structure.

Power LDMOS transistor used as a switch must survive transitions between on and off states [127]. The boundary of electrical safe operating area (SOA) is also linked with the LDMOS design considerations used to improve the $R_O/BV_{DSS}$ tradeoff, especially those concerning the channel [128].

3.2.2. FET switch device model

Many CMOS (practical for all FETs) devices intended for use as switched applications, include gate charge $Q_g$ (coulombs) as one of their specifications. This charge, when present on the gate electrode, causes an electric field to exist which forms the conducting channel between the source and drain. Taking this voltage into account leads to a change in focus from gate charge alone to the related parameter of equivalent gate-source capacitance $C_{in}$ [129]. The latter simply defined as the ratio of the gate charge to the gate-to-source voltage $V_{gs}$ developed between the gate and source with this charge present.
Optimization Principles and Design Guidelines for Monolithic Synchronous Buck Converter in TJ 0.18μm Power Management

\[ C_{in} = \frac{Q_g}{V_{gs}}. \]  

(3.1)

It is well noticed that (3.1) is clearly a large-signal characteristic, as it is defined only at a particular point. Since the application of interest is switching, this is reasonable for present purposes.

Essentially all power MOS devices are constructed by connecting multiple unit-cells in parallel [109]. For present purposes, a MOS unit-cell can be modeled as shown in Fig. 3.3. The equivalent unit-cell gate-source capacitance \( C_{in} \) has a charge on it \( Q_g \) at a gate-source voltage \( V_{gs} \), which in turn controls the channel conductance \( 1/R_{on} \) MOS devices are commonly specified by the channel on-resistance at particular values of gate-source voltage

\[ R_{on} = R \frac{1}{W_g}, \]  

(3.2)

where \( R \) can be expressed as

\[ R = \rho \frac{L_g}{h}, \]  

(3.3)

where \( \rho \) is the resistivity, \( h \) defines the height of the device, and \( L \) is the gate length. It should be noted that typically \( \rho \) and \( h \) are technology-dependent constants defined by the vendor, and only the gate length and width are controllable.

![MOSFET switch unit-cell model](image)

Fig. 3.3 MOSFET switch unit-cell model.

In terms of multiple unit-cells when \( N_f \) instances of a single unit cell are connected in parallel, the resulting equivalent input capacitance, and the channel on-resistance are found to be

\[ C_{in} = N_f C_{in,unit}, \]
\[ R_{on} = \frac{R_{on,unit}}{N_f}. \]  

(3.4)

Thus, the overall channel on-resistance is \( 1/N_f \) times the on-resistance of a single unit-cell, the net equivalent input capacitance of the total switch device is \( N_f \) times the input
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capacitance of the unit-cell, therefore, the gate charge for the complete transistor is N times
the gate charge on each unit cell, as expected.

The charge time $t_{\text{input}}$ is defined as a $RC$ time constant which is the product of $C_{\text{in}}$ and $R_{\text{on}}$

$$t_{\text{input}} = C_{\text{in}}R_{\text{on}}.$$  \hspace{1cm} (3.5)

It is desired for $I_{\text{input}}$ values to be as small as possible, since both $C_{\text{in}}$ and $R_{\text{on}}$ should be
minimized.

An approach to measure the on-resistance of a MOS device with respect to its size by
simulation, is depicted in Fig. 3.4a. By biasing the device with a small amount of voltage
(0.1V $\approx V_{\text{bias}}$), and measuring the current through the device $I_D$, $R_{\text{on}}$ can be found as

$$R_{\text{on}} = \frac{V_{\text{bias}}}{I_D}.$$  \hspace{1cm} (3.6)

It should be emphasized that this approach is solely suitable for a case that the device is
capable of conducting the desired amount of current.

![Fig. 3.4](image)

Fig. 3.4  Simplified schematic diagram for the following measurements: (a) $R_{\text{on}}$, (b) input capacitance $C_{\text{in}}$, (c) output capacitance $C_{\text{out}}$.

Shown in Fig. 3.4b a test-bench to extract the input capacitance. The total gate charge $Q_g$
can be estimated by

$$Q_g = \int_0^{T_{\text{pulse}}} I_G(t)dt ; \quad T_{\text{pulse}} = \frac{1}{f_{\text{pulse}}},$$  \hspace{1cm} (3.7)

where $I_G$ is input current charging the equivalent input capacitances and $T_{\text{pulse}}$ is the duration of the pulse. Substituting (3.7) into (3.1) yields in

$$C_{\text{in}} = \frac{\int_0^{T_{\text{pulse}}} I_G(t)dt}{V_{gs}}.$$

Fig. 3.5 shows typical input capacitances of CMOS and LDMOS devices in TJ 0.18μm
PM technology as a function of the gate width, whereas $L = 1.3μm$ and $W_g$ of a single finger
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is 50μm. $C_{\text{in}}$ is the slope of the measurements and it is product of $C_{\text{ox}}$ (oxidation capacitance) and the gate length of the devices. Assuming the gate voltage of a device is constant, $C_{\text{in}}$ and $C_{\text{out}}$ can be also obtained as a function of $C_{\square}$ as follows

$$
C_{\text{in}} = C_{\text{in}} W_g,
$$

$$
C_{\text{out}} = C_{\text{out}} W_g.
\tag{3.9}
$$

It should be noted that in some technologies $C_{\text{in}}$ values are given within the PDK. TABLE II summarizes obtained resistances and capacitances characteristics in TJ 0.18μm PM for both CMOS and LDMOS devices (N-type devices) for various gate lengths. It is well noticed that CMOS devices have better resistance and capacitance characteristics per-area than LDMOS devices. For $W_g = 500,000 \mu m$ the input capacitance of the LDMOS device is 2.2 times higher than the CMOS device.

![Fig. 3.5](image-url)  
Typical input capacitances in TJ 0.18μm PM. (a) CMOS, (b) LDMOS.
TABLE II. N-TYPE DEVICE CHARACTERISTICS

<table>
<thead>
<tr>
<th>Gate length [μm]</th>
<th>$R_{\square}$ [Ω∙mm]</th>
<th>$C_{\square, in}$ [F/μm]</th>
<th>$C_{\square, out}$ [F/μm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDMOS</td>
<td>1.3</td>
<td>6.7</td>
<td>4.10^{-15}</td>
</tr>
<tr>
<td></td>
<td>0.6</td>
<td>2.2</td>
<td>0.97 - 10^{-15}</td>
</tr>
<tr>
<td>CMOS</td>
<td>1.3</td>
<td>3.8</td>
<td>1.8 - 10^{-15}</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>5.9</td>
<td>3.2 - 10^{-15}</td>
</tr>
</tbody>
</table>

Once the characteristics of the devices are known, optimum devices sizing and attainable efficiency for a given set of operating conditions can be achieved.

3.3. Monolithic buck design procedure

This section presents an optimization procedure of a monolithic buck converter based on a comprehensive power loss analysis. It is assumed that the switching process (internal channel turning ON/OFF) is instantaneous, therefore, switching loss is solely determined by the device output capacitance and device gate capacitance. The inductor is considered ideal to enable generalization of the results.

Primary contributors to the losses of a buck converter are conduction loss $P_{\text{cond}}$, switching loss $P_{\text{sw}}$, and overlap losses $P_{\text{overlap}}$ resulted by the overlap of the current and voltage during the transition of the switches. In addition, LS body diode ($P_{\text{diode}}$) introduces extra loss that can be divided to dead-time losses which induced by LS body diode conduction during dead-times, and diode reverse-recovery loss which are due to the turnoff of the LS FET body diode. Thus, the total power loss in buck converter can be expressed as

$$ P_{\text{total}} = P_{\text{cond}} + P_{\text{sw}} + P_{\text{overlap}} + P_{\text{diode}}. $$

Since $P_{\text{cond}}$ and $P_{\text{sw}}$ are the main contributors to the total loss, in this study $P_{\text{overlap}}$ and $P_{\text{diode}}$ were not expressed with respect to the devices dimensions, hence, the total sum of the losses, $P_{\text{total}}$, can be generally expressed as a function of $P_{\text{cond}}$ and $P_{\text{sw}}$:

$$ P_{\text{total}} = P_{\text{cond}} + P_{\text{sw}}. $$

The conduction loss are considered with respect to both high-side (HS) and low-side (LS) switches, respectively, and expressed as a function of device specific on-resistance $R_{\square}$ (can be obtained by the PDK), gate width $W$, and the rms current $I_{\text{rms}}$ as
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\[ P_{\text{cond}} = P_{\text{cond,HS}} + P_{\text{cond,LS}} \]

\[
P_{\text{cond,HS}} = I_{\text{rms,HS}}^2 \frac{R_{\text{HS}}}{W_{\text{HS}}} = D \left[ I_{\text{out}}^2 + \left( \frac{\Delta I_L}{2\sqrt{3}} \right)^2 \right] \frac{R_{\text{HS}}}{W_{\text{HS}}} , \quad (3.12)\]

\[
P_{\text{cond,LS}} = I_{\text{rms,LS}}^2 \frac{R_{\text{LS}}}{W_{\text{LS}}} = (1 - D) \left[ I_{\text{out}}^2 + \left( \frac{\Delta I_L}{2\sqrt{3}} \right)^2 \right] \frac{R_{\text{LS}}}{W_{\text{LS}}} \]

where \(W_{\text{HS}}\) and \(W_{\text{LS}}\) are gate widths of the HS and LS, respectively, \(D\) is the conversion ratio \((V_{\text{out}}/V_{\text{in}})\), \(I_{\text{out}}\) is the output current, and the current ripple \(\Delta I_L\) which can be found as a function of the inductor’s peak current \(I_{L,\text{peak}}\)

\[ \Delta I_L = I_{L,\text{peak}} - I_{\text{out}} . \quad (3.13) \]

Switching loss are determined by charging or discharging the transistor’s equivalent output capacitance \(C_{\text{DS}}\), and the additional capacitance introduced by the driver circuitry, therefore, the switching loss are found to be

\[ P_{\text{sw}} = P_{\text{sw,HS}} + P_{\text{sw,LS}} \]

\[
P_{\text{sw,HS}} = \frac{1}{2} C_{\text{in,HS}} W_{\text{HS}} V_{\text{gs}}^2 f_{\text{sw}} + \frac{1}{2} C_{\text{out,HS}} W_{\text{HS}} V_{\text{in}}^2 f_{\text{sw}} \]

\[
P_{\text{sw,LS}} = \frac{1}{2} C_{\text{in,LS}} W_{\text{LS}} V_{\text{gs}}^2 f_{\text{sw}} + \frac{1}{2} C_{\text{out,LS}} W_{\text{LS}} V_{\text{in}}^2 f_{\text{sw}} \]

\[ \Rightarrow P_{\text{sw}} = \frac{f_{\text{sw}}}{2} \left( W_{\text{HS}} + W_{\text{LS}} \right) \left( C_{\text{in,HS}} V_{\text{gs}}^2 + C_{\text{out,HS}} V_{\text{in}}^2 \right) \]

where \(f_{\text{sw}}\) is the switching frequency, \(V_{\text{gs}}\) being the gate-to-source voltage swing, \(C_{\text{in,HS}}\) and \(C_{\text{out,LS}}\) can be obtained as detailed in Section 3.2.2.

By substituting (3.12), (3.14) into (3.11) the total power loss can be expressed as

\[ P_{\text{total}} = \left( I_{\text{out}}^2 + \left( \frac{\Delta I_L}{2\sqrt{3}} \right)^2 \right) \left( \frac{R_{\text{HS}}}{W_{\text{HS}}} D + \frac{R_{\text{LS}}}{W_{\text{LS}}} (1 - D) \right) + \frac{f_{\text{sw}}}{2} \left( W_{\text{HS}} + W_{\text{LS}} \right) \left( C_{\text{in,HS}} V_{\text{gs}}^2 + C_{\text{out,LS}} V_{\text{in}}^2 \right) \]

Thus, the minimum total loss with respect to device size can analytically solved using partial derivatives

\[ \frac{\partial P_{\text{total}}}{\partial W_{\text{HS}}} = 0 ; \quad \frac{\partial P_{\text{total}}}{\partial W_{\text{LS}}} = 0 , \quad (3.16) \]

solving (3.16) yields
Optimization Principles and Design Guidelines for Monolithic Synchronous Buck Converter in TJ 0.18μm Power Management

\[ W_{HS,\text{optimal}} = \sqrt{\frac{2R}{(C_{\text{in}}V_{gs}^2 + C_{\text{out}}V_{in}^2)}} \frac{\left(\frac{\Delta I_L}{2\sqrt{3}}\right)^2}{K_{\text{HS}}} \cdot \sqrt{\frac{D}{f_{sw}}} = K_{\text{HS}} \sqrt{\frac{D}{f_{sw}}} \]

\[ W_{LS,\text{optimal}} = \sqrt{\frac{2R}{(C_{\text{in}}V_{gs}^2 + C_{\text{out}}V_{in}^2)}} \frac{\left(\frac{\Delta I_L}{2\sqrt{3}}\right)^2}{K_{\text{LS}}} \cdot \sqrt{\frac{1-D}{f_{sw}}} = K_{\text{LS}} \sqrt{\frac{1-D}{f_{sw}}} \]

hence, optimum efficiency is found as

\[ \eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{total}}} = \frac{1}{1 + \sqrt{Df_{sw}} + \sqrt{(1-D)f_{sw}}} \cdot \frac{k_1}{k_2} \]

where

\[ k_1 = \frac{P_{\text{out}}}{\left(\frac{f_{\text{out}}}{R} + \left(\frac{\Delta I_L}{2\sqrt{3}}\right)^2\right) K_{\text{HS}}} \cdot \frac{\left(C_{\text{in}}V_{gs}^2 + C_{\text{out}}V_{in}^2\right) K_{\text{HS}}}{2} \]

\[ k_2 = \frac{P_{\text{out}}}{\left(\frac{f_{\text{out}}}{R} + \left(\frac{\Delta I_L}{2\sqrt{3}}\right)^2\right) K_{\text{LS}}} \cdot \frac{\left(C_{\text{in}}V_{gs}^2 + C_{\text{out}}V_{in}^2\right) K_{\text{LS}}}{2} \]

Since \( P_{\text{overlap}} \) and \( P_{\text{diode}} \) were not taken into account during the optimization steps, further optimization can be carried out by compensating the gate widths as following

\[ W_{HS,\text{optimal}}^* = K_{\text{HS}} \sqrt{\frac{D}{f_{sw}}} (1 + \alpha) \]

\[ W_{LS,\text{optimal}}^* = K_{\text{LS}} \sqrt{\frac{1-D}{f_{sw}}} (1 + \alpha) \]

where \( \alpha < 1 \), is an estimated factor of the overlap loss and LS body diode loss.

It can be therefore concluded that the an optimized efficiency of a buck converter is based on the following relationships

\[ \eta \propto \frac{1}{f_{SW}} ; \quad \eta \propto \frac{1}{\sqrt{D}} ; \quad \eta \propto W_{HS/LS} \cdot \]

The gate widths of a symmetrical design with respect to \( P_{\text{overlap}} \) and \( P_{\text{diode}} \) can be expressed and as a function of the desired efficiency by rearranging (3.15) and (3.17)
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\[ W_{Symmetrical} = W_{HS} = W_{LS} = \sqrt{2R_{on} \left( f_{SW} \left( C_{gs} V_{gs}^2 + C_{out} V_{in}^2 \right) \right)} \cdot \left(1 + \alpha \right) ; \alpha < 1 \] (3.22)

Based on the above analysis and IC design guidelines, a 5V-gated LDMOS based monolithic buck design example is demonstrated with target values of: \( V_{in} = 12V \), \( V_{out} = 1.5V \), \( I_{out} = 4A \), \( f_{SW} = 1MHz \), \( \eta \approx 83\% \). For a given current ripple of 20mA, the resulting on-resistances of the switches are: \( R_{on,LS} \approx 45m\Omega \), \( R_{on,HS} \approx 120m\Omega \), and in terms of silicon width 150,000μm and 57,000μm, respectively, while the resulting total silicon width is found to be \( W_{total} \approx 207,000μm \). Fig. 3.6 depicts theoretical efficiency prediction for the design example as a function of the total gate widths. The results imply that for the same silicon area, efficiency improvement by approximately 3% can be obtained at the target operating values. A more noticeable benefit can be viewed in terms of overall size, where approximately 25% less silicon area is required to obtain the same efficiency. Additionally, in the vicinity of large gate widths \( (W_{total} > 450,000μm) \), the results of both optimized and symmetrical methods are near identical, since the losses of the LS switch are the primary contributors to the total loss. However, choosing \( W_{total} \) smaller than the obtained by the design procedure, the efficiency of the optimized design is clearly better than the symmetrical partition.

![Efficiency Curve](image)

Fig. 3.6 Theoretical efficiency curves of a monolithic buck in TJ 0.18μm PM process as a function of the gate widths. Symmetric (dotted blue line), and optimized (red solid line) partitions, with the target parameters: \( V_{in} = 12V \), \( V_{out} = 1.5V \), \( I_{out} = 4A \), \( f_{SW} = 1MHz \).

### 3.4. Mixed-signal IC implementation

The mixed-signal IC shown in Fig. 3.1 integrates power, analog and digital circuits on one die. To satisfy proper operation, several layout constraints such as adding guard rings and isolation wells between devices are essential to reduce coupling noise and undesired
Optimization Principles and Design Guidelines for Monolithic Synchronous Buck Converter in TJ 0.18μm Power Management

holes/electrons injections. This section primarily focuses on IC implementation, design considerations of the power-stage and the digital implementation procedure.

3.4.1. Power-stage implementation

The mixed-signal IC’s synchronous rectifier power-stage is constructed by N-channel devices for both the high and low side switches. In this study, these are realized by a 5V-gated LDMOS power device. As discussed in detail in Section 3.2.1, using LDMOS allows higher voltage swing operation of a monolithic DC-DC converter, since its typical breakdown voltage is higher than the standard 5V CMOS device. Each switch has a dedicated driving stage designed with a 5V CMOS, whereas the HS transistor requires a bootstrap driver and floating level shifter configuration to overcome the limitations of a standard CMOS device breakdown voltage. Following the design procedure the power-stage’s switches have been designed symmetrically with an on-resistance of 33mΩ. The gate width of the switches is 200,000μm, obtained based on the target operating point derived from the above design example. Each switch is constructed from 4000 fingers, creating a symmetrical quadrilateral layout pattern.

3.4.2. Driver circuitry

Tapered inverter chains are commonly used to drive high load capacitance in ICs. Instead, if a single minimally sized inverter were used to drive high load capacitance, the RC time constants for charging/discharging would be high leading high propagation delay. Therefore a series of inverters are cascaded in such a way to minimize the propagation delay from the input to the output [129]-[131]. Optimally sized MOS transistors of DC-DC converters power-stage also have high input capacitances. The input capacitance can be considered as load capacitance and an inverter chain can be designed so as to minimize the propagation delay of the gate signal. In [132], an alternative driving approach based only on N-type transistors in GaN process has been presented. This section explores this approach (see Fig. 3.7) in TJ 0.18μm CMOS process. Due to better mobility per-area of an N-type device, an improved area consumption is achieved [133].
The driver’s principal of operation is based on two states: pull-up to charge load capacitance to the upper voltage rail (see Fig. 3.7b), and pull-down to discharge load capacitance to the lower voltage rail (see Fig. 3.7c).

Discharge of the load capacitance is enabled when $PWM_{DRV}$ signal is on (high logic value). At this mode, $Q_1$ and $Q_2$ are on, such that a low impedance path to ground is formed through $Q_2$ to discharge load capacitance. $Q_1$ is used to pull-down the gate voltage of $Q_3$, therefore disabling the charge of the load from the HS rail. Size optimization is required to pull-down the gate voltage of $Q_3$ and is expressed as

$$V_{gate,Q_1,\text{critical}} = V_{th} > V_{DD} \frac{R_{on1}}{R_{on1} + R_g}.$$  \hspace{1cm} (3.23)

Charge of the load capacitance is enabled when $PWM_{DRV}$ signal is off (low logic value). At this mode $Q_1$ and $Q_2$ are off, and $Q_3$ enables low impedance path between the upper voltage rail and the load capacitance.

As appose to the pull-down state, this state does not supply $V_{gate}$ with a full voltage swing ($0 \rightarrow V_{DD}$), since NMOS device is limited by its pull-up capability, therefore the maximum obtained $V_{gate}$ is
The total power consumption of the driver is obtained to be

\[ P_{\text{DRV}} = \frac{V_{\text{DD}}^2}{R_{\text{on1}} + R_g} \]  

(3.25)

From (3.25) it is well understood that choosing large \( R_g \) reduces the power loss of the driver. However, large \( R_g \) increases the charge time, since the resulted equivalent \( RC \) time constant would be high leading to high propagation delay. Fig. 3.8 depicts simulation comparison between N-type driver and the tapered inverter driver operating at 1MHz switching frequency, whereas the load capacitance is 1nF to emulate power device transitions. It can be seen that the rise and fall times are identical and equal to 3nS (optimized values \( R_g = 1k\Omega \) and \( R_{\text{on1}} = 20\Omega \)). It should further emphasized that 4.2V is sufficient to drive 5V-gated gated devices in TJ 0.18μm PM. The latter indicates that N-type driver is a perfect candidate for area sensitive applications.

\[ \text{Fig. 3.8} \quad \text{Simulated output voltage of the N-type gate driver and the tapered inverter driver operating at 1MHz switching frequency, as the threshold voltage of the transistors is 0.8V, and the equivalent load capacitance is 1nF.} \]

3.4.3. High-side level shifter

The HS transistor is driven by a bootstrap configuration to assure proper driving signals of the power-stage. By realizing such approach the voltage drop on the level shifter is potentially a full rail-to-rail voltage swing from \( V_{\text{in}}+5V \) to ground, damaging the CMOS device. One approach to overcome this issue, is designing the level shifter circuit with LDMOS devices only, which results in a significant larger die-size and higher power consumption. In this study, a merged CMOS and LDMOS approach has been employed and
Optimization Principles and Design Guidelines for Monolithic Synchronous Buck Converter in TJ 0.18μm Power Management

is shown in Fig. 3.9. The LDMOS devices $DM_1$-$DM_4$ are used in critical branches to absorb the high voltage drop. As a result, this level shifter does not require biasing circuitry for and relies on the logic rail alone. This has been accomplished by appropriate sizing of transistors $M_1$ and $M_2$ with respect to $V_{DD}$, creating a self-biased level shifter circuit.

![Fig. 3.9 High-voltage level shifter circuit](image)

The level shifter circuit is divided into three main sub-units. First, an edge detector that triggers the level-shifter whenever the PWM signal changes. Second, the shifting unit constructed by $DM_1$-$DM_4$ to absorb the high voltage drop to assure that the stress on $M_1$-$M_4$ does not exceed 5V. Finally, a differential pair that saturates the differential change between $V_P$ and $V_N$, such that the PWM signal voltage levels, $V_{DD}$ and ground, are shifted to $V_{sw}$ and $V_{sw}+5V$, respectively. The output signal of the differential pair controls the floating drive circuitry of the HS transistor.

The resistor $R_s$ is added between $V_{sw}$ and the positive branch $V_{plus}$ of the shifting unit in order to intentionally cause a slight voltage difference between the branches. By doing so, unless a real change of the PWM signal occurs, the gate of the HS transistor is normally pulled down eliminating shoot-through current scenario caused by an undesired noise. It should be noted that the offset voltage between the branches is determined by the value of $R_s$.

The matching of the differential pair’s transistors $M_9$ and $M_{10}$ primarily depends on the process variations [133]. Thus, proper layout techniques should be taken into consideration, especially isolating guard rings to further improve the noise-immunity of the diff-pair. In this design, common-centroid technique is used for the layout of $M_9$ and $M_{10}$, where $M_7$ and $M_8$ are also highly matched to achieve accurate active load operation [135].
3.4.4. Programable dead-time

To minimize the shoot-through current loss of a DC-DC converter, it is necessary to control the gate driving signals with a proper dead-time, such that the power transistors $Q_{HS}$ and $Q_{LS}$ turn on does not overlap. Another important task of the adjustable dead-time unit is to improve the efficiency of the converter [131], therefore, a programmable dead-time module based on delay-line string [136] has been developed. The string of 200 delay elements connected to an 8-channels multiplexer as depicted in Fig. 3.10. Shown in Fig. 3.10b switching behavior for three switching scenarios: (1) Dead-time too large, the body diode of the LS switch gets forward biased due to the forced inductor current. This leads to excessive losses depending on the output current $I_{out}$, the switching frequency $f_{sw}$, and the respective dead time. (2) Dead-times, which are too small or even negative, lead to high power losses, as the LS switch is not turned on with zero voltage switching (hard switching), or cross-conduction occurs as both switches are turned on at the same time. (3) The optimal switching point is achieved, when the high-side or low-side switch, respectively, turns on a very short instant before the body diode of the low-side or high-side switch starts conducting. In this case, the losses are minimal as the low-side and high-side switch are turned on with zero voltage switching. This can be achieved, if the parasitic capacitances at the switching node are fully charged and discharged by the inductor current while the low-side or high-side switch, respectively, is still turned off.

The delay time $t_{delay}$, set within an internal memory register with initial default value, and can be programmed from 1ns up to 40ns. The module has been implemented by pure digital means which will be discussed in detail in 3.4.5.
Optimization Principles and Design Guidelines for Monolithic Synchronous Buck Converter in TJ 0.18μm Power Management

![Schematic diagram of a programmable dead-time module based delay-line.](image)

**3.4.5. Digital implementation design flow**

The realization of the dead-time module and the digital PWM controller (the controller is beyond the scope of this study) relies on a digital implementation flow, using vendor’s standard cells only. The digital implementation is carried out through two main steps. In the first step, the controller’s units are in HDL. Then, each unit is synthesized using synthesis and timing verification tools into an optimized gate-level representation, given a set of design constraints (such as skew and jitter, power consumption, etc.). The layout of each unit was generated by an automated place-and-route process.

In the second step, the units have been integrated with the power and analog units, creating the finalized buck converter IC. It should be further emphasized that the dead-time and controller designs scale with the technology, such that its overall area can be significantly reduced by implementing it to a deeper sub-micron process.

**3.5. Experimental verification**

A synchronous buck converter IC has been designed and fabricated in TJ 0.18μm PM 5V CMOS process, a chip micrograph is depicted in Fig. 3.11a. The fabricated IC prototype was packaged using 28-pin 5x5mm QFN package (some of the pins are dedicated to the digital controller which is not discussed in this study), Fig. 3.11b depicts the IC prototype on PCB.
Optimization Principles and Design Guidelines for Monolithic Synchronous Buck Converter in TJ 0.18μm Power Management

To demonstrate the operation of the synchronous buck converter and to validate the design procedure principles, the mixed-signal IC has been verified with experimental and post layout results, whereas the IC connects to an external filter of $L = 2.2\mu\text{H}$, $C_{\text{out}} = 56\mu\text{F}$. $R_{\text{on}}$ of the power transistors was designed to value of $\sim 33\text{mΩ}$ (discussed in Section 3.4.1), experimental kelvin resistance measurements of the packaged IC converter resulted in approximately $120\text{mΩ}$ and $200\text{mΩ}$ for the LS and HS switches, respectively, the impact of the package and bond wires limitations are given in detail in 2.4.4. The IC was tested with two operating frequencies 1.25MHz and 620KHz, with the ability to deliver up to 10W from a 12V input, Table II summarizes the mixed-signal IC main characteristics.

**TABLE III. SUMMARY OF IC PROTOTYPE CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>5x5 QFN - MLP</td>
</tr>
<tr>
<td>$V_{\text{in}}$</td>
<td>12V</td>
</tr>
<tr>
<td>Power-stage $R_{\text{on}}$ LS/HS</td>
<td>$\sim 120\text{mΩ}$, $\sim 200\text{mΩ}$</td>
</tr>
<tr>
<td>Nominal $V_{\text{out}}$</td>
<td>1.5V</td>
</tr>
<tr>
<td>Nominal $I_{\text{out}}$</td>
<td>1.5A</td>
</tr>
<tr>
<td>Off-chip $LC$ filter</td>
<td>2.2nH, 56μF</td>
</tr>
<tr>
<td>Switching frequency $f_{\text{sw}}$</td>
<td>1.25MHz (620KHz)</td>
</tr>
<tr>
<td>Peak efficiency</td>
<td>70% (76%)</td>
</tr>
<tr>
<td>Total chip Si area</td>
<td>4.4mm²</td>
</tr>
</tbody>
</table>

(a)
The PWM control signals at operating frequencies of 1.25MHz and 620KHz for the switches are produced internally from the digital controller, which provides signals with 180ps resolution. The PWM control signals can be also obtained from an external FPGA. Switching node voltage \( V_{sw} \), output voltage and the inductor current with a duty-ratio of 0.125 at 1.25MHz and 600KHz operation are shown in Fig. 3.12a and Fig. 3.12b, respectively. Smooth low-to-high and high-to-low transitions operation can be observed, implying that the high voltage level shifter operates properly.
Efficiency measurement of the converter (excluding drive losses) at the target values (i.e. $V_{out}$=1.5V, $I_{out}$=1.5A) with 12V input and various output voltages are provided in Fig. 3.13, demonstrating a peak efficiency of 70% at 1.25MHz and 76% at 620KHz. It can be observed that in the range of 0.3A load current the efficiency is measured to be 85%. The latter can be explained by natural soft switching operation of the high-side device obtained in the region of 0.3A load current. Large enough inductor current ripple allows the current to become negative and charge the switching node capacitance in a lossless manner [137]. There is a deviation between the experimental results and the predicated theoretical analysis, the latter may be due to higher on-resistances, the transistors’ body-diode losses that were not taken into account during the design [138], and a possible high leakage current that should be further investigated.

![Efficiency graph](image)

Fig. 3.13 Experimental efficiency measurements of the converter IC for different output voltages as a function of the load current $I_{out}$ at: (a) $f_{SW}$ = 1.25MHz, (b) $f_{SW}$ = 620KHz.
Fig. 3.14 shows the efficiency measurements for 1.5V output and various input voltages to examine the converter IC efficiency in case the input voltage is unregulated. As can be observed, at 1.25MHz and $V_{in}=8V$ the peak efficiency is 80%. For load current of 5A all three curves converge towards 59%. At switching frequency of 620KHz and in the region of soft switched operation the peak efficiency of all input voltages converge to approximately 87%.

Fig. 3.14  Experimental efficiency measurements of the converter IC for different input voltages as a function of the load current $I_{out}$ at: (a) 1.25MHz and (b) 620KHz.

### 3.6. Conclusion

This chapter introduced an IC optimization procedure of MOS transistors for monolithic buck converters to achieve minimum power loss per die-area. The optimum width of power devices primarily depends on the output current of the buck converter, the operating frequency, and the conversion ratio. Comprehensive analysis explored the impact of TJ 0.18μm PM technology on the achievable performance for a target set of operating conditions.

Based on the design procedure a 4.4mm$^2$ mixed-signal IC integrating the synchronous buck converter including the drive circuitry with a digital programmable dead-time module, was designed and fabricated in TJ 0.18μm 5V CMOS process, with the ability to deliver up to 10W from 12V input. High-voltage level shifter without biasing circuitry is accomplished using a bootstrap technique, with the bootstrap diode integrated on the same die. A programmable dead-time module has been implemented on-chip by pure digital means without additional custom designs. Considering the package’s parasitics for 12V-to-1.5V at 1.25MHz operation the peak efficiency of the converter IC is measured to be 70%. The
power loss of the prototype should be further investigated in order to understand the unpredicted deviation between the target and measured efficiencies. A primary suspicion for the deviation is a possible relatively high leakage current that should be further examined by experimental setups.
4. Discussion

4.1. Contribution of the research

The key contributions of this work are summarized as follows:

**Optimal design procedure for a resonant-mode SCC IC** – In SCC technology, existing design tools propose symmetrical switch resistances for all switching states. In IC area-sensitive applications higher attention should be given to the desired resistance per switch to obtain optimum results. An optimal size-efficiency design procedure for IC realization of resonant switched-capacitor-type converters based on the target operating point has been proven throughout the research that it can reduce the overall volume of converter and improve the power processing efficiency.

**GRSCC IC design guidelines** – Following the optimal design procedure of a resonant-mode SCC IC realization, full analytic extraction of a GRSCC has been carried out, detailing efficiency analysis and characteristics of a GRSCC operating as a voltage regulator. The design methodology combined with the converter’s benefits present an attractive approach for better power delivery concepts for PoL applications.

**Fully monolithic constant on-time controller** – A fully monolithic internal controller based delay-line has been designed and implemented on-chip by pure digital automated synthesis process and place-and-route tools to regulate the output voltage. The controller’s design is generic and scalable with the technology, such that its overall area can be significantly reduced by implementing it to a deeper sub-micron process.

**Optimization principles and design guidelines for monolithic synchronous buck converter in TJ 0.18μm PM** – This study introduces an optimization principles and design guidelines for monolithic synchronous buck converter using TJ 0.18μm PM technology. Combined with a digital control method developed in PEMIC group, the optimized buck IC design introduces first of its kind a fully-integrated digital average current-mode control 12V-to-1.xV voltage regulator module that has been designed and fabricated by PEMIC group.
4.2. Suggestions for future research

Some suggestions for future lines of investigation that can be developed as a result of this thesis are outlined below:

**3-D power delivery of a fully monolithic GRSCC** – The GRSCC combines the topology features of switched-capacitor technology and conversion characteristics from the switched-inductor family, therefore, GRSCC is a perfect candidate for future 3-D technology integration. Comprehensive investigation of realizing this technology with the GRSCC is a key factor in yielding an ultimate PoL converter configuration with much better power density.

**Development of improved dead-time calibration and ZCD circuitry for a monolithic constant on-time controller** – The experimental results of the GRSCC IC prototype reveal extra losses resulted from mismatches of zero-current detection and dead-time calibration. Precise calibration is important in soft switching topologies for maintaining both high frequency and efficiency operation and, further improving the overall efficiency of the GRSCC.

**Leakage current of the power devices** – In modern ICs leakage current is not negligible, thus, a primary suspicion for the difference between the predicted and measured efficiencies may be the static leakage current of the devices. Further measurements and analysis can be done to completely characterize TJ 0.18μm PM LDMOS power devices.

**Including packaging and wiring optimization to assure absolute certainty of final IC design** – The experimental measurements of the IC prototypes presented in this thesis, clearly exhibit the bond wires and package limitation, in the case of the GRSCC prototype by four times than the targeted on-resistance. Future work direction can include packaging and wiring optimization to accurately estimate the package contribution to the system performance, assuring absolute certainty of final design.
Appendix – Optimization method of Lagrange multipliers for RSCC design procedure

5. Appendix – Optimization method of Lagrange multipliers for RSCC design procedure

The conduction losses of the transistors are given in Section 2.2 as

\[
P_{\text{cond},i} = \sum_{i=1}^{N} P_{Q_i} = P_{Q_1} + P_{Q_2} + \ldots + P_{Q_N}, \quad K_i = \frac{L_g}{\mu C_{ov}(V_{gs} - V_{th})}, \quad (3.26)
\]

where \( W_i \) is the gate width which determines the transistor’s resistance alongside the technology-dependent parameter \( K_i \).

The total area width \( W_{\text{total}} \) is the sum of the individual width per transistor and can be expressed as

\[
\sum_{i=1}^{N} W_i = W_1 + W_2 + \ldots + W_N = W_{\text{total}}. \quad (3.27)
\]

By utilizing the *optimization method of Lagrange multipliers* on (3.26), using (3.27) as the optimization constraint yields

\[
\begin{align*}
\text{function: } f(W_1, W_2, \ldots, W_N) &= P_{\text{cond}} = \frac{I_{\text{rms},Q_1}^2 K_1}{W_1} + \frac{I_{\text{rms},Q_2}^2 K_2}{W_2} + \ldots + \frac{I_{\text{rms},Q_N}^2 K_N}{W_N} \\
\text{constraint: } g(W_1, W_2, \ldots, W_N) &= W_{\text{total}}
\end{align*}
\]

\[
, \quad (3.28)
\]

**Lagrange Multipliers Method:**

\[
\begin{align*}
\nabla f(W_1, W_2, \ldots, W_N) &= \lambda \nabla g(W_1, W_2, \ldots, W_N) \\
g(W_1, W_2, \ldots, W_N) &= W_{\text{total}}
\end{align*}
\]

this yields

\[
\begin{align*}
1: \quad \frac{\partial f}{\partial W_1} &= \lambda \frac{\partial g}{\partial W_1} \Rightarrow \frac{I_{\text{rms},Q_1}^2 K_1}{W_1^2} = \lambda \\
2: \quad \frac{\partial f}{\partial W_2} &= \lambda \frac{\partial g}{\partial W_2} \Rightarrow \frac{I_{\text{rms},Q_2}^2 K_2}{W_2^2} = \lambda \\
3: \quad \frac{\partial f}{\partial W_3} &= \lambda \frac{\partial g}{\partial W_3} \Rightarrow \frac{I_{\text{rms},Q_3}^2 K_3}{W_3^2} = \lambda \\
& \vdots \\
N: \quad \frac{\partial f}{\partial W_N} &= \lambda \frac{\partial g}{\partial W_N} \Rightarrow \frac{I_{\text{rms},Q_N}^2 K_N}{W_N^2} = \lambda
\end{align*}
\]

which results in the following equality
Appendix – Optimization method of Lagrange multipliers for RSCC design procedure

\[
\frac{I_{rms,Q_1}^2 K_1}{W_1^2} = \frac{I_{rms,Q_2}^2 K_2}{W_2^2} = \ldots = \frac{I_{rms,Q_N}^2 K_N}{W_N^2}, \tag{3.30}
\]

the equality in (3.30) can be thus rewritten as

\[
\begin{cases}
\frac{I_{rms,Q_1}^2 K_1}{W_1^2} = \frac{I_{rms,Q_n}^2 K_n}{W_n^2} \\
\frac{I_{rms,Q_2}^2 K_2}{W_2^2} = \frac{I_{rms,Q_n}^2 K_n}{W_n^2} \\
\frac{I_{rms,Q_3}^2 K_3}{W_3^2} = \frac{I_{rms,Q_n}^2 K_n}{W_n^2} \\
\vdots \\
\frac{I_{rms,Q_{N-1}}^2 K_{N-1}}{W_{N-1}^2} = \frac{I_{rms,Q_n}^2 K_n}{W_n^2}
\end{cases} \quad \Rightarrow \quad \begin{cases}
W_1 = W_N \frac{I_{rms,Q_1} \sqrt{K_1}}{I_{rms,Q_n} \sqrt{K_n}} \\
W_2 = W_N \frac{I_{rms,Q_2} \sqrt{K_2}}{I_{rms,Q_n} \sqrt{K_n}} \\
W_3 = W_N \frac{I_{rms,Q_3} \sqrt{K_3}}{I_{rms,Q_n} \sqrt{K_n}} \\
\vdots \\
W_{N-1} = W_N \frac{I_{rms,Q_{N-1}} \sqrt{K_{N-1}}}{I_{rms,Q_n} \sqrt{K_n}} \\
W_N = W_N \frac{I_{rms,Q_N} \sqrt{K_N}}{I_{rms,Q_n} \sqrt{K_n}}
\end{cases}, \tag{3.31}
\]

or more generally

\[
W_i = W_N \frac{I_{rms,Q_i} \sqrt{K_i}}{I_{rms,Q_n} \sqrt{K_n}}, \quad i = 1, 2, \ldots, N. \tag{3.32}
\]

Substituting (3.31) into (3.27), and after some manipulations, \(W_{total}\) can thus be expressed as a function of \(W_N\), the rms currents and the technology technology-dependent parameters \(K_i\)

\[
W_{total} = W_N \left( 1 + \frac{1}{I_{rms,Q_n} \sqrt{K_n}} \left( I_{rms,Q_1} \sqrt{K_1} + I_{rms,Q_2} \sqrt{K_2} + \ldots + I_{rms,Q_{N-1}} \sqrt{K_{N-1}} \right) \right) = W_N \left( \frac{\sum_{j=1}^{N} I_{rms,Q_j} \sqrt{K_j}}{I_{rms,Q_n} \sqrt{K_n}} \right) = W_N \left( \frac{\sum_{i=1}^{N} I_{rms,Q_i} \sqrt{K_i}}{I_{rms,Q_n} \sqrt{K_n}} \right) \tag{3.33}
\]

By reversing (3.33) \(W_N\) is expressed as

\[
W_N = W_{total} \left( \frac{I_{rms,Q_n} \sqrt{K_n}}{\sum_{i=1}^{N} I_{rms,Q_i} \sqrt{K_i}} \right) \tag{3.34}
\]
Appendix – Optimization method of Lagrange multipliers for RSCC design procedure

By substituting (3.34) into (3.32), a generalized expression of the individual silicon width $W_i$ with respect to the total die-size is obtained to be

$$W_i = W_{total} \frac{I_{rms,n} \sqrt{K_N}}{\sum_{i=1}^{N} I_{rms,Q_i} \sqrt{K_i}} \frac{I_{rms,Q_i} \sqrt{K_i}}{L_{rms,Q_i} \sqrt{K_i}}, \quad i = 1, 2, ..., N. \quad (3.35)$$
6. References


References

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