Soft Switching of Switched-Capacitor Converters

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE M.Sc. DEGREE

By: Eli Hamo

Supervised by:
Dr. Mor Mordechai Peretz

January 2015
Soft Switching of Switched-Capacitor Converters

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE M.Sc. DEGREE

By: Eli Hamo

Supervised by:
Dr. Mor Mordechai Peretz

Author: Eli Hamo  Date: 05/01/15
Supervisor: Dr. Mor Mordechai Peretz  Date: 05/01/15

Chairman of graduate studies committee
Name: Dr. Ilan Shalish  Date: 05/01/15
Dedicated to my beloved mother

Shoulamit

With love and gratitude
Abstract

Switched-capacitor dc-dc power converters are a subset of dc-dc power converters that use a network of switches and capacitors to efficiently convert one voltage to another. Unlike traditional inductor-based dc-dc converters, switched capacitor converters (SCCs) do not rely on magnetic energy storage. This fact makes SCC ideal for integrated implementations. However, SCCs have traditionally been used in low power and low conversion ratio applications due to the inherent energy losses resulting from the capacitor charging and discharging processes, conduction, and switching losses.

The primary aim of this thesis is to improve the behavior and performance of SCC applications in the higher power range. The methods and the applications presented in this study are focused on high efficiency including many target voltages and soft switching. Typically, these challenges prohibit the operation of capacitor-based converters in the medium and high power ranges. This study introduces a simple and efficient isolated gate driver circuitry and active control system for applying the soft switching method. This work provides a streamlined procedure to design reliable and practical multiphase SCCs with respect to the desired efficiency and conversion ratios. The research includes a full behavioral description, analysis theorem, application examples, and experimental results. Those parts of the research have been published in the proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE) 2013 [1], and within a larger study in the IEEE Transactions on Power Electronics [2]. Relevant sections have also already been published [3].

Another objective of this thesis is to develop a modeling methodology to describe and explore the loss mechanism of a resonant SCC operating in a self-commutation zero current switching (ZCS) mode. This passive, soft switching approach simplifies the control effort and eliminates additional circuitry involved in active soft-switching controls. The model presented in this study assists in the simplification and optimization of SCC systems and their controls to achieve high efficiency up to the higher power range. The modeling methodology provides a streamlined procedure to design a reliable and low-cost soft-switched SCC. The theoretical predictions of the model were compared with simulations and laboratory experiments in various SCC topologies and operation modes. This part of the research has been published in the proceedings of the IEEE Applied Power Electronics Conference (APEC) 2014 [4] and within a larger study in the IEEE Transactions on Power Electronics [5].

This research can directly contribute to the research and development of converters, regulators, and integrated power supplies that are based on switched-capacitor technology in a wide range of power applications.

Keywords: Average static model, binary codes, conduction losses, dc-dc power converters, free-wheeling diode, modeling, resonant converter, self-commutation, soft switching, switched capacitor converter, switched-mode power supply, switching losses, zero current switching.
Acknowledgements

I would like to thank my supervisor Dr. Mor Peretz for his invaluable guidance and support for the duration of my research. Through an invaluable and rare combination of professional expertise, managerial guidance, and amiable friendship, Mor has impelled me to excellence, all the while providing me with the opportunities for enjoyment and for the self-fulfillment of achieving my goals.

I give special thanks to my supervisor Professor Shmuel (Sam) Ben-Yaakov, for all I have learned from him, for support and for his constant demand for high-quality science advances. Thanks for the open mind, boundless enthusiasm, and sense of humor and for his willingness to support and to help.

Special thanks must be recorded to the co-authors of the articles, Dr. Michael Evzelman, and Mr. Alon Cervera, for their collaboration, research work, and ideas. They are always happy to help everyone, at anytime, anywhere.

I must not forget all undergraduate and graduate students here at our research laboratory whose support and friendship meant so much: Mr. Alon Blumenfeld, Mr. Shai Dagan, Ms. Yara Halihal, Dr. Natan Krihely, Mr. Zeev Rubinshtein, Mr. Ofer Ezra, Mr. Or Kirshenboim, and anyone that I forgot to mention by name.

Of the technical staff, I would like to thank Neli Grinberg, Azrikam Yehieli, and Udovikin Larisa who are responsible for the excellent working and social conditions of the laboratory.

I give thanks to my parents for their love and support throughout my whole life, and for their steering me towards a higher education and the achievement of excellence in whatever I undertake without treading on others or using any insincere techniques. It would be hard to imagine better individuals to guide me through life, show me an example of how to live and behave, and provide for all my spiritual and material needs, never expecting anything in return but my love.
# Table of Contents

List of Tables .............................................................................................................................. xi
List of Figures .............................................................................................................................. xii
Acronyms and Abbreviations ...................................................................................................... xvii
Inline References Legend ............................................................................................................ xvii

## Chapter 1 - Introduction

1. Power supplies .......................................................................................................................... 1
   1.1 Linear regulators .................................................................................................................... 1
   1.2 Switched capacitor dc–dc converters .................................................................................. 4
1.3 Generic conduction losses model and efficiency of SCC ....................................................... 6
   1.3.1 Equivalent resistance calculation: Hard switching case .................................................. 6
   1.3.2 Equivalent resistance calculation: Soft switching case .................................................. 8
   1.3.3 Diode losses ................................................................................................................... 8
1.4 Binary and Fibonacci SCC .................................................................................................... 9
   1.4.1 Binary and Fibonacci codes .......................................................................................... 10
   1.4.2 Translating the codes into SCC topologies .................................................................... 11
1.5 Resonant converters and soft switching .............................................................................. 13
   1.5.1 High power resonant SCC ............................................................................................ 14
1.6 Current sensing ...................................................................................................................... 16
   1.6.1 Current sensors .............................................................................................................. 16
   1.6.2 Zero current detection .................................................................................................... 18
1.7 Research objectives and significance .................................................................................... 20
1.8 Thesis Overview ..................................................................................................................... 22

## Chapter 2 - Multiple Conversion Ratio Resonant Switched-Capacitor Converter

  with Active Zero Current Detection ......................................................................................... 23
2.1 Introduction ............................................................................................................................ 23
2.2 Principle operation of the resonant binary/Fibonacci SCC .................................................. 24
2.3 Practical implementation ...................................................................................................... 26
   2.3.1 Current sensing and zero crossing detection ................................................................. 27
   2.3.2 Reference voltage ......................................................................................................... 28
   2.3.3 Stabilizing the flying capacitors voltage on startup .................................................... 29
   2.3.4 Switches and isolated gate drivers .............................................................................. 30
2.4 Conclusions .......................................................................................................................... 33
List of Tables

Table 1.1  The Codes for n=1÷3 ..................................................................................................................11
Table 2.1  Solutions of the Average Capacitor Currents for Various Ratios ........................................26
Table 3.1  Solutions of the Average Capacitors Currents for All Ratios and Total Capacitance
  per Phase ..................................................................................................................................................37
Table 3.2  Normalized Form of the Equivalent Resistors of the EXB Codes ........................................38
Table 3.3  Normalized Form of the Equivalent Resistors of the SFN Codes ........................................39
Table 3.4  Normalized Form of the Equivalent Resistors of the SGF Codes ........................................40
Table 3.5  Converter Parameters ............................................................................................................47
Table 3.6  Measurements with Active ZCS for Constant ......................................................................47
Table A.1  The Switches State According to the EXB Codes .................................................................76
List of Figures

Fig. 1.1. A basic linear regulator: (a) equivalent regulator circuit (b) a simple practical implementation.................................................................2

Fig. 1.2. Basic dc-dc switching converter: (a) switching equivalent circuit (b) Output voltage........2

Fig. 1.3. (a) Buck dc-dc converter. (b) Typical waveforms voltages and currents with time in an ideal buck converter operating in continuous mode. ...........................................................3

Fig. 1.4. Dickson topology for basic voltage multiplier (charge pump). For example of double gain topology - when the CLK is at low level, D1 conduct and C1 is charging from V_in and C2 discharge to the load. CLK at high level - D2 conducted and C2 is charge from C1 ..................................................................................5

Fig. 1.5. Structure of modern SCC topologies. ........................................................................5

Fig. 1.6. SCC generic equivalent circuit....................................................................................6

Fig. 1.7. Charge/discharge instantaneous capacitor current waveforms: (a) Complete charge—CC mode. (b) Partial charge—PC mode. (c) No charge—NC mode.........................7

Fig. 1.8. Plot of the normalized equivalent resistance covering all SCC operation modes for the hard switch case. ........................................................................................................7

Fig. 1.9. The binary/Fibonacci converter with three flying capacitors (n=3): (a) step down topology, (b) typical efficiency graph showing multiple peaks for 19 conversion ratios.....9

Fig. 1.10. SCC topologies configured from the EXB codes of M=5/8. ........................................12

Fig. 1.11. Currents and voltages waveforms of the switching modes. (a) Hard switching with and without snubers. (b) Resonant switching. V_s is the voltage across the switch and I_s is the current through the switch.....................................................................14

Fig. 1.12 Typical switching loci for a hard-switched converter without switching-aid-networks, with snubbers and for a soft-switched converter operation, (V_T is the voltage across the switch and I_T is the current through it). ............................................................................................14

Fig. 1.13. High power resonant SCC topology with interleaved, V_o=V_in/5. .................................15

Fig. 1.14. Waveforms of the high power resonant SCC: (a) capacitors and load currents (b) capacitors and output voltages. Simulations set-up at: V_in=250V, P_out=12.5 kW, L1=8.2 µH, L2=2.2 µH, all flying capacitors Cj=300 µF, and f_s=1.67 kHz. ..............................15

Fig. 1.15. Conventional DCR current sensing method in a buck converter. In this method, when \( R_C \cdot C_1 = L/DCR \) from the transfer function, \( V_{c1}/I_L \) then \( V_{c1} = DCR \cdot I_L \). ..................................................17

Fig. 1.16. A typical structure of SENSEFET and sample circuit to increase the accuracy........17

Fig. 1.17. (a) Typical basic ZCD system configuration (b) Resonant pulses and the reference value........................................................................................................................................19
Fig. 2.1. Resonant SCC scheme showing the current sensors and analog comparator for zero cross detection. .................................................................24
Fig. 2.2. Resonant SCC sub-circuits configured from the EXB codes of $M=5/8$ ...............25
Fig. 2.3. Resonant binary SCC (a) Capacitors and output stage current waveforms. (b) Capacitors and output voltages waveforms. PSIM Simulations set-up at: $M=5/8$, $V_{in}=100V$, $P_{out}=100W$, $L_s=200nH$, all flying capacitors $C_j=9.4\mu F$, and $f_s=90kHz$. S5 is the normalized switch gate-source control voltages, $I_{C1}$, $I_{C2}$ and $I_{C3}$ are the currents through the flying capacitors $C_1$, $C_2$ and $C_3$. $I_{Ls}$ is the inductor current at the output stage, and $I_{out}$ is the load current. $V_{C1}$, $V_{C2}$, $V_{C3}$ are the capacitor voltages across the flying capacitors and AVG($V_{C1}$, $V_{C2}$, $V_{C3}$) are the average voltages. .................................................................................................................26
Fig. 2.4. Worst-case conditions of state current variation and the mismatch of the switching instance due to fixed reference settings. ..................................................................................29
Fig. 2.5. Conceptual operation of the soft start sequences for $M=3/8$ (resonant current): (a) high-frequency switching; (b) estimated resonant values; (c) active ZCS method .................30
Fig. 2.6. Isolated Gate Driver and four-quadrant switch using N – channel power MOSFETs ....32
Fig. 2.7. Operation modes: (a) on state - CGS charging (b) off state - CGS Discharging ..........32
Fig. 2.8. Experimental waveforms of the isolated gate driver: (a) $C_3$ voltage (5 V/div). (b) $C_2$ voltage (2 V/div). (c) $D_2$ voltage (5 V/div). (d) output voltage, $V_{Gate}$ (5 V/div). Horizontal scale (10 $\mu$s/div). .................................................................................................................32
Fig. 3.1. Worst-case plot of the normalized equivalent resistance as a function of $Q_{j,low}$, for conversion the ratios: (a) $M=1/8$, 3/8, and (b) $M=5/8$, 7/8 for $df_j$ in the range of 0.15-0.35 (0.05 step each iteration in $df_j$). The curves were extracted numerically using MATLAB ..................................................................................................................32
Fig. 3.2. Worst-case plot of the normalized equivalent resistance as a function of $Q_{j,low}$, for conversion the ratios: (a) $M=2/8$, 6/8 (b) $M=3/8$, 4/8 (c) $M=2/5$, 3/5 (d) $M=1/3$, 2/3 (e) $M=1/5$ (f) $M=4/5$ (g) $M=1/2$ (h) $M=1/7$- 6/7 for $df_j$ in the range of 0.15-0.35..............41
Fig. 3.2. (Continued). .................................................................................................................42
Fig. 3.3. $I_{out}$ and $V_{DS}(S6)$ at $V_{in}=100V$, $P_{out}=136W$, $M=5/8$ ........................................44
Fig. 3.4. $I_{out}$ and $V_{DS}(S6)$ at $V_{in}=80V$, $P_{out}=100W$, $M=5/8$ ........................................44
Fig. 3.5. $I_{out}$ and $V_{DS}(S6)$ at $V_{in}=60V$, $P_{out}=69.89W$, $M=3/8$ ........................................44
Fig. 3.6. Efficiency of step-down, resonant binary SCC, $M=5/8$ ............................................44
Fig. 3.7. Prototype of the resonant binary SCC ............................................................................47
Fig. 3.8. Experimental result of the binary converter operating in active ZCS mode for various conversion ratios. (a) \( M=1/8 \), \( V_{in}=80 \) V, \( P_{out}=31.3 \) W, \( \eta=0.85 \); Traces top to bottom: inductor current \( I_{Ls} \) (0.8 A/div), rectified sensed voltage resulting from \( I_{c3}, V_{c3} \) (10 V/div), rectified sense voltage resulting from \( I_{c2}, V_{c2} \) (10 V/div), comparator output, \( V_{cmp} \) (5 V/div). Horizontal scale (5 \( \mu \)s/div). (b) \( M=3/8 \), \( V_{in}=100 \) V, \( P_{out}=76.5 \) W, \( \eta=0.92 \); Traces top to bottom: \( I_{Ls} \) (0.8 A/div); \( V_{c3} \) (10 V/div); \( V_{cmp} \) (5 V/div); interrupt status \( V_{out} \) (5 V/div). Horizontal scale (10 \( \mu \)s/div). (c) \( M=5/8 \), \( V_{in}=80 \) V, \( P_{out}=73 \) W, \( \eta=0.95 \). Traces and horizontal scale: as in (b). (d) \( M=7/8 \), \( V_{in}=80 \) V, \( P_{out}=131.7 \) W, \( \eta=0.99 \). Traces top to bottom: \( I_{Ls} \) (0.4 A/div), \( V_{c3} \) (5 V/div); \( V_{cmp} \) (5 V/div); \( V_{int} \) (5 V/div). Horizontal scale (5 \( \mu \)s/div). .................................................................................................................................48

Fig. 3.9. (a) Slope difference between the highest and the lowest current pulses at fixed output power - 31.3 W, \( I_o=3.6 \) A. (b) and (c) Slope differences between pulses at wide output power range, \( P_o=5 \) W, \( I_o=1.7 \) A and \( P_o=31.3 \) W, \( I_o=3.6 \) A, respectively........................................48

Fig. 3.10. Measured efficiency, \( M=1/8-7/8 \), constant \( R_o, V_{in}=30-80 \) V.................................................................49

Fig. 3.11. Measured efficiency, \( M=1/8-7/8 \), constant \( V_{in}=80 \) V.................................................................49

Fig. 3.12. Experimental results of the inductor current for the soft-start method for \( M=3/8 \): (a) High switching frequency; (b) estimated resonant values; (c) active ZCS method........49

Fig. 4.1. Typical resonant current waveforms during a: Charge phase – DCP operation, Discharge phase – SCP operation ...........................................................................................................53

Fig. 4.2. Unity gain SCC with free-wheeling ZCS of the charge state.................................................................53

Fig. 4.3. Operation states of unity gain SCC (Fig. 4.2): (a) Charging sub-state \( ij = 1a \), (b) Charging sub-state \( ij = 1b \), (c) Discharging state \( i = 2 \) .................................................................54

Fig. 4.4. The basic and generic instantaneous \( RLC \) sub-circuit.................................................................54

Fig. 4.5. DCP switching phase current waveform............................................................................................55

Fig. 4.6. SCC generic average equivalent circuit that shows the contribution of the partial sub-circuits equivalent resistances \( R_{ei} \) to the total equivalent circuit resistance \( R_e \). For the unity gain SCC example of Fig. 4.2, \( R_{e1a} \) is the loss contribution of charge sub-state 1a, \( R_{e1b} \) and \( V_{d1b} \) are the resistive and diode loss contribution of the free-wheeling sub-state, respectively, \( R_{e2} \) is the loss contribution of discharging phase........................................................................56

Fig. 4.7. Variation of \( R_e \) as a function of \( \phi_i \) for different ratios of loop resistances between \( R_{1a} \) and \( R_{1b} \). In the example above \( R_{1a} = R_{2} = 10 \) m\( \Omega \). ................................................................................................................57

Fig. 4.8. Distribution of the charge through paths \( ia \) and \( ib \) as a function of the commutation angle \( \phi_i \) ........................................................................................................................................58

Fig. 4.9. Output voltage of a unity gain SCC as a function of the commutation angle, \( \phi \). Model calculation–solid trace, simulation–asterisk marks. \( V_{in}=10 \) V, \( V_{f}=1.7 \) V, \( R_{DS(on)}=100 \) m\( \Omega \), \( R_o=5 \) \( \Omega \), \( Q \approx 30, f_o \approx 5 \) kHz. ........................................................................................................................................59
Fig. 4.10. Illustration waveform of a resonant current for several values of the quality factors 
(0.55≤f7), where \(L=50\ \mu\text{H},\ C=100\ \mu\text{F}\) and 0.1 \(\Omega<r<1.4\ \Omega\) .................................60

Fig. 4.11. Illustration of DCP switching phase current waveform at low Q .........................................................61

Fig. 4.12. Distribution of the charge through paths \(ia\) and \(ib\) as a function of the commutation 
angle \(\phi_i\) for an extensive range of the quality factor \((0.58>Q>10)\), where \(L=1\ \mu\text{H},\ C=100\ \mu\text{F}\) and 0.01 \(\Omega<r_{\text{loop}}<0.18\ \Omega\), \(R_{\text{loop}1a}=R_{\text{loop}1b}\) ........................................61

Fig. 4.13. Unity gain SCC switching circuit, with charge phase operated in a DCP mode. 
(Switch \(S_{1b}\) blocks undesired conduction paths) .................................................................63

Fig. 4.14. Voltage doubler converter topology with free-wheeling diodes \(D_1, D_2\). Charge phase: 
\(S_{1a}, S_{1b}–\text{ON}, \text{discharge phase: } S_{2a}, S_{2b}–\text{ON}.\) .................................................................63

Fig. 4.15. Experimental waveforms obtained from a unity gain resonant SCC operating in DCP 
mode with \(\phi_i \approx 126^\circ\). Upper traces–charge sub-states currents, Bottom trace–discharge 
current. Scale: vertical–2 A/div, horizontal–2 ms/div .................................................................64

Fig. 4.16. Average currents at paths 1a and 1b. Model calculation–solid trace, simulation–dashed 
line, and experimental results–\((I_{1a})\) asterisk marks and \((I_{1b})\) circle marks ........................................64

Fig. 4.17. Equivalent average diode voltage drop, \(V_d\), as a function of the commutation phase, \(\phi\). 
Model calculation–solid trace, simulation–dashed line, and experimental results–asterisk marks.................................64

Fig. 4.18. Output voltage as a function of the commutation phase, \(\phi\). Model calculation–solid 
trace, simulation–dashed line, and experimental results–asterisk marks .................................................64

Fig. 4.19. Experimental waveforms obtained from a double gain resonant SCC operating in DCP 
mode with \(\phi_1\approx96^\circ, \phi_2\approx139^\circ, V_{in}=10\ \text{V}, R_{\text{loop}1a,2a}=370\ \text{m\Omega}, R_{\text{loop}1b,2b}=100\ \text{m\Omega}, V_{F1,2}=1.7\ \text{V}, P_{\text{out}}=10.6\ \text{W}, \text{Upper traces–charge sub-states currents, bottom trace–discharge sub-states currents. Scale: vertical–2 A/div, horizontal–5 ms/div}.................................66

Fig. 4.20. Experimental waveforms obtained from a double gain resonant SCC operating in DCP 
mode with \(\phi_1\approx\phi_2\approx139^\circ, V_{in}=10\ \text{V}, R_{\text{loop}1a,2a}=370\ \text{m\Omega}, R_{\text{loop}1b,2b}=100\ \text{m\Omega}, V_{F1,2}=1.7\ \text{V}, P_{\text{out}}=11.3\ \text{W}, \text{Upper traces–charge sub-states currents, bottom trace–discharge sub-states currents. Scale: vertical–2 A/div, horizontal–5 ms/div}.................................66

Fig. 4.21. Experimental waveforms obtained from a double gain resonant SCC operating in DCP 
mode with \(\phi_1\approx148^\circ, \phi_2\approx139^\circ, V_{in}=10\ \text{V}, R_{\text{loop}1a,2a}=370\ \text{m\Omega}, R_{\text{loop}1b,2b}=100\ \text{m\Omega}, V_{F1,2}=1.7\ \text{V}, P_{\text{out}}=11.3\ \text{W}, \text{Upper traces–charge sub-states currents, bottom trace–discharge sub-states currents. Scale: vertical–2 A/div, horizontal–5 ms/div}.................................66
Fig. 4.22. SCC generic average equivalent circuit that shows the contribution of the partial sub-circuits equivalent resistances $R_{ei}$ to the total equivalent circuit resistance $R_e$. (For the doubler SCC example of Fig. 4.14, $R_{e1a}$ is the loss contribution of charge sub-state 1a, $R_{e1b}$ and $V_{d1b}$ are the resistive and diode loss contribution of the free-wheeling sub-state, respectively. $R_{e2a}$ is the loss contribution of the discharge sub-state 2a, $R_{e2b}$ and $V_{d2b}$ are resistive and diode loss contribution of the free-wheeling discharge sub-state, respectively).

Fig. 4.23. Multiphase Fibonacci resonant SCC topology with free-wheeling diodes $D_{1-4}$. Phase1: $S_1$, $S_3$–ON, Phase 2: $S_2$, $S_4$, $S_6$–ON, Phase 3: $S_2$, $S_5$, $S_7$, $S_9$–ON, Phase 4: $S_2$, $S_5$, $S_8$, $S_{10}$–ON.

Fig. 4.24. Simulation waveforms obtained from a resonant Fibonacci SCC operating in DCP mode with $\phi_i \approx 144^\circ$.

Fig. 4.25. Output voltage of the DCP operation mode of a resonant Fibonacci SCC as a function of the commutation angle, $\phi$. Model calculation–solid trace, simulation–asterisk marks.

Fig. 4.26. Contribution of conduction losses of the resonant Fibonacci SCC operated in DCP mode. (a) Equivalent resistant, $R_e$, as a function of the commutation angle, $\phi$ (b) Equivalent average diode voltage drop, $V_d$, as a function of the commutation angle, $\phi$.

Fig. 4.27. Average currents at paths 1a and 1b at low $Q$ as function of $\phi$. Model calculation–$(I_{1b})$ solid trace and $(I_{1a})$ dashed line, simulation results–$(I_{1a})$ asterisk marks and $(I_{1b})$ circle marks.

Fig. A.1. Resonant binary/Fibonacci switched capacitor step-down converter, example for $n=3$.

Fig. A.2. Resonant binary/Fibonacci switched capacitor step-up converter, example for $n=3$.

Fig. A.3. Resonant SCC sub-circuits configured from the Fibonacci sequence $M=8$. 
### Acronyms and Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>BSD</td>
<td>Binary Signed-Digit</td>
</tr>
<tr>
<td>CC</td>
<td>Complete Charge</td>
</tr>
<tr>
<td>CCM</td>
<td>Continuous Conduction Mode</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DCM</td>
<td>Discontinuous Conduction Mode</td>
</tr>
<tr>
<td>DCP</td>
<td>Divided Conduction Path</td>
</tr>
<tr>
<td>DCR</td>
<td>Direct-Current Resistance</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
</tr>
<tr>
<td>EXB</td>
<td>Extended Binary</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>KCL</td>
<td>Kirchhoff’s Current Law</td>
</tr>
<tr>
<td>KVL</td>
<td>Kirchhoff’s Voltage Law</td>
</tr>
<tr>
<td>LDO</td>
<td>Low Dropout</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-Oxide-Semiconductor Field-Effect Transistor</td>
</tr>
<tr>
<td>NC</td>
<td>No Charge</td>
</tr>
<tr>
<td>PC</td>
<td>Partial Charge</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PV</td>
<td>Photo Voltaic</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>RMS</td>
<td>Root Mean Square</td>
</tr>
<tr>
<td>RSCC</td>
<td>Resonant Switched Capacitor Converter</td>
</tr>
<tr>
<td>SC</td>
<td>Switched Capacitor</td>
</tr>
<tr>
<td>SCC</td>
<td>Switched Capacitor Converter</td>
</tr>
<tr>
<td>SCP</td>
<td>Single Conduction Path</td>
</tr>
<tr>
<td>SFN</td>
<td>Signed Fibonacci Number</td>
</tr>
<tr>
<td>SGF</td>
<td>Signed Generalized Fibonacci</td>
</tr>
<tr>
<td>SIC</td>
<td>Switched Inductor Converter</td>
</tr>
<tr>
<td>SMPS</td>
<td>Switched Mode Power Supplies</td>
</tr>
<tr>
<td>ZCD</td>
<td>Zero Current Detection</td>
</tr>
<tr>
<td>ZCS</td>
<td>Zero Current Switching</td>
</tr>
<tr>
<td>ZVS</td>
<td>Zero Voltage Switching</td>
</tr>
</tbody>
</table>

### Inline References Legend

<table>
<thead>
<tr>
<th>Reference Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>X.XX</td>
<td>Section/Chapter number</td>
</tr>
<tr>
<td>(X.XX)</td>
<td>Equation</td>
</tr>
<tr>
<td>[XX]</td>
<td>Reference</td>
</tr>
<tr>
<td>Fig. X.XX</td>
<td>Figure</td>
</tr>
</tbody>
</table>
Chapter 1 - Introduction

1.1 Power supplies

Power supplies are an essential part of practically all-modern technological systems, ranging from appliances to mobile phones, renewable energy sources and just about any grid-connected system. Power supplies are used to convert the electrical energy provided by an electrical source to another form needed for proper operation of the system. Power supplies can be divided into two basic groups—linear regulators and switched mode converters.

1.1.1 Linear regulators

Linear regulators [6]-[11] have been widely used for decades in power supply systems, providing supplies for low-power applications. This kind of voltage regulator provides a low cost solution for voltage stabilization. Linear regulators are easy in design and implementation and have good precision of the output voltage value (in the steady-state). They are built around an active element (such as a transistor), which is normally connected between the electrical source and the load and operated in its linear region. In this way the active element acts as a variable resistor and together with the load forms as a voltage divider.

An example of converting a dc voltage to a lower dc voltage level is the simple circuit shown in Fig. 1.1. The output voltage is \( V_{out} = I_o R_o \), where the load current is controlled by the transistor represented by a variable resistor (see Fig. 1.1a). By adjusting the transistor base current, the output voltage may be controlled over a range of zero to \( V_{in} \). The base current can be adjusted by control circuitry to compensate for variations in the supply voltage or the load, thus regulating the output. As can be seen from Fig. 1.1a, the only current in the series element is the load current. Neglecting the power required for the circuit to control the series element, the efficiency of any regulator carrying out the process of power conversion, is defined as:

\[
\eta = \frac{P_{out}}{P_{in}} = \frac{V_{o}}{V_{in}},
\]

(1.1)

where \( P_o \) is the output power, \( P_{in} \) is the input power, and the dissipated power is defined as \( P_{in} - P_{out} \).

As can be observed, the efficiency depends on the ratio of load-to-source voltage and not on the load current. This series–pass transistor drives all the current demanded by the load. Thus, this component has to be dimensioned to dissipate an important quantity of energy, increasing the price, volume, and weight in the supply system. For large differences between the input and the output voltages the efficiency of linear regulators is fairly low, and hence its use is normally restricted to low drop out (LDO) applications, where this difference is small. While this may be a simple method of converting a dc supply voltage to a lower dc voltage level and regulating the output, the low efficiency
of this circuit is a serious drawback, especially for high-power applications. A simple practical implementation of a linear regulator is depicted in Fig.1.1b. This application uses an operational amplifier feedback network to control the series transistor.

![Diagram of linear regulator circuit](image)

Fig. 1.1. A basic linear regulator: (a) equivalent regulator circuit (b) a simple practical implementation.

1.1.2 Switched mode converters

An efficient alternative to the linear regulators is the switch mode converters [6]-[11]. These circuits employ solid-state devices that operate as electronics switches by being completely on (saturation) or completely off (cutoff).

Switch mode power supplies (SMPS) and converters aim to use high-frequency switching in order to reduce the component size. In its simplest form, a reactive element is switched in between an input and an output, charging and discharging, respectively. The reactive element can be either an inductor or a capacitor or both. Inductor-based SMPS has several basic structures, emphasizing the buck (step-down), the boost (step-up), and the buck-boost converters. The main advantage of these structures is their high efficiencies.

A simple switch mode converter can be described by Fig. 1.2a. Assuming the switch is ideal, the output is the same as the input when the switch is closed, and the output is zero when the switch is open. Periodic opening and closing of the switch results in the pulse output shown in Fig. 1.2b.

![Diagram of switch mode converter](image)

Fig. 1.2. Basic dc-dc switching converter: (a) switching equivalent circuit (b) Output voltage.

The average or dc component of the output is:

\[ V_o = \frac{1}{T_s} \int_0^{T_s} V_o(t) dt = \frac{1}{T_s} \int_0^{T_s} V_{in} dt = DV_{in} , \]  

(1.2)
where $D = t_{on}/T_S$, $t_{on}$ is the time the switch is on, and $T_S$ is the switching period. The dc component of the output is controlled by adjusting the duty ratio, $D$, and will be less than or equal to the input for this circuit.

Losses will occur in a real switch because the voltage drop across it will not be zero when it is on, and the switch must pass through the linear region when making a transition from one state to another. Furthermore, the design and implementation of this sort of converter is a more complex process than in linear regulators. This is important especially in the control loops when both line and load regulations are desired. Another drawback is that the intrinsic switched nature of the converter produces ripples in the output voltage, as well as an increment of the electromagnetic interference (EMI) due to high frequency switching.

Controlling the dc component of a pulse output of the type in Fig. 1.2b may be sufficient for some applications, but often the objective is to produce an output that is purely dc. One way of obtaining a dc output from a circuit of the type in Fig. 1.2a is to insert a low pass filter after the switch, as depicted in Fig 1.3. When the switch is closed, (diode reverse biased), the inductor is charging from the input voltage while the free-wheeling diode provides a path for the inductor discharging current to the load when the switch is opened. The diode naturally opens as the input is disconnected due to current continuity demands of the inductor. The switching frequency now depends on the hardware capabilities, e.g., the switch turn on and turn off times, driving component speed, etc.

![Diagram](image-url)

**Fig. 3.1.** (a) Buck dc-dc converter. (b) Typical waveforms voltages and currents with time in an ideal buck converter operating in continuous mode.
1.2 Switched capacitor dc-dc converters

Since the 1970s, switched-capacitor dc-dc converters [12] have been investigated due to their small size, lightweight, and good integration features for a power supply on chip (Fig. 1.4). As opposed to conventional switch mode dc-dc converters that include bulky inductors to process and store energy, switched capacitor converters (SCCs) require only capacitors and MOSFET switches (in basic form). The use of a small ceramic capacitor makes them very compact and suitable for high temperature environments. Conventional switched-capacitor dc-dc converters mainly concentrate on the low-power conversion area for portable electronic equipment applications [13]. Switched-capacitor converters are useful for applications that require small currents, usually less than 100 mA. Applications include use in RS-232 data signals that require both positive and negative voltages for logic levels; in flash memory circuits, where large voltages are needed to erase stored information; and in drivers for LEDs and LCD displays [14]-[19].

A SCC can be unidirectional or bidirectional and can have any number of inputs, outputs, or both [14]. The basic SCC cell is shown in Fig. 1.5. It has a flying (switched) capacitor and a network of switches that connect the capacitor to the ports of the SCC and/or other capacitors. The name ‘flying’ reflects the nature of the capacitor, which is connected to different ports during the SCC operation. Subsequently, its common mode to ground voltage can change during the operation.

A full SCC system can be built around a single SCC cell, or can contain a large number of cells (Fig. 1.5) where they are interconnected depending on the purpose of the converter: step-up, step-down, inverting, etc. Moreover the converter can be based on a number of sub-converters connected in series or in parallel, or a combination of the two [15]. For example, a unit gain converter can be applied with one cell, (includes C, S₁, and S₂), that connect the flying capacitor to the input stage (for charging) and to the load (for discharging). Double gain can be obtained with one cell, (C, S₁-S₄), where the flying capacitor is in series with the input voltage during its discharge cycle.

Some more advanced converters have sophisticated switch networks, which allow more than a single conversion ratio with the same SCC stage. Many variations [15]-[21] of the switched capacitor are able to provide multiple output levels by manipulating multiple flying capacitors, alternating between parallel, series, or mixed parallel-series connections. An example of a multiple conversion system is an SCC with binary and Fibonacci resolution, built around three basic SCC cells [22]-[24]. These bidirectional SCC formed 19 discrete fractional options to voltage conversion in step-up or step-down mode.

In order to increase the efficiency, reduce the switching losses, voltage spikes, and EMI, several zero current switching (ZCS) topologies have been proposed. These are realized by inserting small inductors in series with the capacitors for resonant operation [16]-[21]. An important feature of the converter is its internal resistance of each phase, $R_i$. This represents the sum of all losses due to parasitic properties of
the used components. Efforts to eliminate the internal resistance lead to the use of capacitors with low series resistance (ESR) and to the use of switching elements with uni-polar characteristics with low impedance in the switched “on” state. Parallel, or interleaved [25], structures have an advantage in reducing the ripple of the input/output port of the converter, and the disadvantage is the larger number of components and the requirement for a more advanced controller.

Fig. 3.1. Dickson topology for basic voltage multiplier (charge pump). For example of double gain topology - when the CLK is at low level, $D_1$ conduct and $C_1$ is charging from $V_{in}$ and $C_2$ discharge to the load. CLK at high level - $D_2$ conducted and $C_2$ is charge from $C_1$.

Fig. 3.1. Structure of modern SCC topologies.
1.3 Generic conduction losses model and efficiency of SCC

Any SCC operating in open loop can be represent by an equivalent circuit [26] that includes target voltage, $V_T$, connected in series with an equivalent resistant, $R_e$, that represents all the conduct losses in the converter (Fig 1.6). The model is applicable in the case where all the converter phases can be represented by $RC$ (hard switching) or $RCL$ (resonant and soft switching) networks. The target voltage refers to the no-load output voltage of the converter and can be evaluated for a given SCC by a set of algebraic equations.

![SCC generic equivalent circuit.](image)

The efficiency of SCC can be defined by the model described in Fig. 1.6 as:

$$\eta = \frac{V_o}{V_T} = \frac{R_o}{R_o + R_e}, \quad V_T = M \cdot V_{in},$$

(1.3)

where $M$ is the no-load voltage transfer ratio. The no-load conversion ratio $M$ of a charge pump is defined as the ratio of the desired output voltage, $V_T$, to the supply voltage, $V_{in}$, when the load current is zero. A step-up charge pump has $M>1$ and step-down $M<1$.

1.3.1 Equivalent resistance calculation: Hard switching case

The equivalent resistance expresses the conduction losses of the converter caused by the current that passes via all the loop resistances in the capacitors’ charge/discharge phases. In hard switched SCC, the equivalent resistance can be represented by [26], [27]:

$$R_e = \frac{1}{2f_s} \cdot \sum_{i=1}^{n} \frac{k_i^2 \coth \left( \frac{\beta_i}{2} \right)}{C_i},$$

(1.4)

where $\beta_i = t_i / R_i C_i$, $k_i$ is the proportional factor, $R_i$ and $C_i$ are the total resistance and capacitance of phase $i$, respectively. The loop resistance, $R_i$, of phase $i$, can be derived from $R_i = R_{\text{switch}} + R_{\text{inductor}} + \text{ESR}$.

The proportional factor, $k_i$, depends on the SCC topology and may vary between the charge/discharge phases. It can be calculated by applying KCL and taking into account the charge balance equation for all SCC switching capacitors. This factor connects between the average current of the flying capacitor, $I_{C_{avg}}$, to the average output current, $I_o$, as follows:
\[ I_{c_{av}} = k_i I_o, \]  

(1.5)

Analysis of the loss expressions for the hard switched case reveals that the losses of a given SCC will depend on the value of equation (1.4) for each of the sub-circuits. This value depends, in turn, on the operating mode of the SCC and in particular on the value of \( \beta_i \), which will determine whether the charging/discharging process completed within \( T_i \) will have the current waveform shown in Fig. 1.7(a) (denoted as Complete Charging (CC) mode), the charging is partially completed (“PC” mode) and has the current waveform that is presented in Fig. 1.7(b), or the current will be about constant (Fig. 1.7(c)), and the capacitor will have a practically constant voltage (denoted as No Charging (NC) mode).

Fig. 1.7. Charge/discharge instantaneous capacitor current waveforms: (a) Complete charge—CC mode. (b) Partial charge—PC mode. (c) No charge—NC mode.

The behavior of \( R_{ei} \) over the full range [27] of the charge/discharge regions (CC, PC, and NC) is given in Fig. 1.8, which presents the normalized equivalent resistance, \( R_{ei}^* \), of a single charge or discharge sub-circuit, derived from equation (1.4) and normalized by the factor \( 1/(m \cdot k_i^2 \cdot R_i) \), assuming symmetrical operation (i.e., the same switching duration for each of the \( m \) sub-circuits). Fig. 1.8 illustrates the case of unity SCC, where \( m=2 \).

Fig. 1.8. Plot of the normalized equivalent resistance covering all SCC operation modes for the hard switch case.
1.3.2 Equivalent resistance calculation: Soft switching case

In soft-switched resonant SCC, the equivalent resistance can be represented by:

\[ R_{eq} = \frac{1}{2f_s} \cdot \sum_{i=1}^{n} k_i^2 \cdot \tanh \left( \frac{\pi \cdot \xi_{di}}{2} \right), \]  \hspace{1cm} (1.6)

where \( \omega_0 = \frac{1}{\sqrt{L_i C_i}} \), \( \alpha_i = \frac{R_i}{2 \cdot L_i} \), \( \xi_{di} = \frac{a_i}{\omega_{di}} \), \( \omega_{di} = \sqrt{\omega_0^2 - \alpha_i^2} \), and \( L_i \) is the total inductance of phase \( i \).

It should be noted that equation (1.6) is valid when the quality factor \( Q_i > 1/2 \). Equation (1.6) can also be expressed in terms of the quality factor \( Q_i \), [27]:

\[ R_{eq} = \frac{1}{2f_s} \cdot \sum_{i=1}^{n} k_i^2 \cdot \frac{2\pi Q_i^2 R_i}{\text{df}_i \sqrt{4Q_i^4 - 1}} \cdot \tanh \left( \frac{\pi}{2\sqrt{4Q_i^4 - 1}} \right), \]  \hspace{1cm} (1.7)

where \( \text{df}_i \) is the ratio between the switching frequency, \( f_s \), to the damped resonant frequency, \( f_{di} \).

1.3.3 Diode losses

Diode conduction losses are modeled by adding to the generic equivalent circuit (Fig 1.6) a voltage source, \( V_D \), which is equal to the sum of the forward voltage drops, \( V_{F_i} \), of all the diodes in the converter. Diode voltage source, \( V_D \), is connected in series to the target voltage and in negative polarity. The expression of the diode is taking into account the average current through each diode by the proportional factor, \( k_i \), that is:

\[ V_D = \sum_{i=1}^{n} k_i V_{F_i}. \]  \hspace{1cm} (1.8)
1.4 Binary and Fibonacci SCC

In many applications there is a need to maintain a constant output voltage under input voltage variation or to provide different output voltages. As mentioned in Section 1.3, a generic equivalent circuit model [27] for SCC has losses that are conveniently described as a function of the load current by $R_e$. Equation (1.3) implies that a high efficiency can be reached if $M$ is controllable with high resolution. Many studies demonstrated a multiphase SCC topologies producing several conversion ratios [28]-[30]. These studies have shown that the efficiency of multiple conversion ratio SCCs can be maintained effectively over a wider input voltage range than that of a single topology converter.

An effective method to realize many target voltages is to use the binary/Fibonacci SCC that exhibits a high resolution [22]-[24]. For example, step-down SCC (Fig. 1.9) with closely spaced multiple target voltages, have been developed with extended binary (EXB), signed Fibonacci (SFN), and signed generalized Fibonacci (SGF) codes. Those codes can be translated into sequences of SCC topologies that produce fractional output to input ratios. According to this approach, flying capacitors are automatically kept charged to binary weighted voltages and, consequently, the resolution of the target voltages is binary. The resolution can be made higher by increasing the number of codes and/or flying capacitors. These previous binary/Fibonacci SCC were implemented by hard switched SCC topologies and were limited to low-power devices due to the relatively large number of switches [22]-[24].

![SCC Diagram](image)

**Fig. 1.9.** The binary/Fibonacci converter with three flying capacitors ($n=3$): (a) step down topology, (b) typical efficiency graph showing multiple peaks for 19 conversion ratios.
1.4.1 Binary and Fibonacci codes

The structures of the binary SCC depicted in Fig. 1.9a are based on algebraic expressions [22]-[24] that are described by the following definitions and observations. Any number of \( M \) in the range (0, 1) can be represented in the form:

\[
M = A_0 + \sum_{j=1}^{n} A_j 2^{-j},
\]

(1.9)

where \( A_0 \) can be either 0 or 1, \( A_j \) takes on any of three values -1, 0, 1, and \( n \) sets the resolution. For example, the code \( \{1 0 -1 -1\} \) implies:

\[
M = 1 + 0 \cdot 2^{-1} - 1 \cdot 2^{-2} - 1 \cdot 2^{-3} = 5/8.
\]

(1.10)

Expression (1.9) defines the EXB representation that is a modified version of the binary signed-digit (BSD) representation [31]-[33]. Unlike the conventional binary case, a number of different EXB codes can represent a single \( M \) value. The different codes can be generated by spawning rules [22].

The following example demonstrates how four alternative EXB codes are spawned from the binary code of \( M=\frac{5}{8} \). For example, the conventional binary code of \( \frac{5}{8} \) is \( \{0 1 0 1\} \). In the left sequence of equation (1.11) the “1” of \( A_3 \) (the LSB) is replaced by “-1” and the “1” carry is added to \( A_2 \). The resulting code is \( \{0 1 1 -1\} \). The conventional code is transformed to other equivalent codes and so on.

\[
\begin{align*}
A_0 A_1 A_2 A_3 & \quad A_0 A_1 A_2 A_3 & \quad A_0 A_1 A_2 A_3 & \quad A_0 A_1 A_2 A_3 & \quad A_0 A_1 A_2 A_3 \\
2^0 2^1 2^2 2^3 & \quad 2^0 2^1 2^2 2^3 & \quad 2^0 2^1 2^2 2^3 & \quad 2^0 2^1 2^2 2^3 & \quad 2^0 2^1 2^2 2^3 \\
0 1 0 1 & + 0 1 0 1 & + 0 1 0 1 & + 0 1 1 -1 & + 1 -1 1 -1 \\
0 0 0 \text{(1)} & + 0 0 1 0 & + 0 1 0 0 & + 0 1 0 0 & + 0 0 1 0 \\
0 1 1 0 & + 0 1 1 1 & + 1 0 0 1 & + 1 0 1 -1 & + 1 0 0 -1 \\
0 0 0 \text{(1)} & + 0 0 -1 0 & + 0 -1 0 0 & + 0 -1 0 0 & + 0 0 -1 0 \\
0 1 1 -1 & + 0 1 0 1 & + 1 -1 0 1 & + 1 -1 1 -1 & + 1 0 -1 -1
\end{align*}
\]

(1.11)

The conventional and alternatives EXB codes, thus generated and representing the same fraction of \( M=\frac{5}{8} \) are summarized as follows:

\[
\begin{align*}
\{1 0 -1 -1\} & \rightarrow 1 + 0 \cdot 2^{-1} - 1 \cdot 2^{-2} - 1 \cdot 2^{-3} = 5/8 \\
\{1 -1 1 -1\} & \rightarrow 1 - 1 \cdot 2^{-1} + 1 \cdot 2^{-2} - 1 \cdot 2^{-3} = 5/8 \\
\{0 1 1 -1\} & \rightarrow 0 + 1 \cdot 2^{-1} + 1 \cdot 2^{-2} - 1 \cdot 2^{-3} = 5/8 \\
\{1 -1 0 1\} & \rightarrow 1 - 1 \cdot 2^{-1} + 0 \cdot 2^{-2} + 1 \cdot 2^{-3} = 5/8 \\
\{0 1 0 1\} & \rightarrow 0 + 1 \cdot 2^{-1} + 0 \cdot 2^{-2} + 1 \cdot 2^{-3} = 5/8
\end{align*}
\]

(1.12)

All other codes (SFN, SGF) extract with the same method but with different math rules. The EXB, SFN, and SGF codes for all 19 fractions, \( n=1\div3 \), are summarized in Table 1.1.
Table 1.1 - The Codes for \( n=1/3 \)

<table>
<thead>
<tr>
<th>EXB Codes</th>
<th>( M=1/8 )</th>
<th>( M=2/8 )</th>
<th>( M=3/8 )</th>
<th>( M=4/8 )</th>
<th>( M=5/8 )</th>
<th>( M=6/8 )</th>
<th>( M=7/8 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( A_1 )</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>( A_2 )</td>
<td>0</td>
<td>1</td>
<td>-1</td>
<td>-1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>( A_3 )</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>-1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

1.4.2 Translating the codes into SCC topologies

Fig. 1.10 shows how EXB codes of a given \( M \) can be translated into sequences of SCC topologies that produce the fractional output to input ratio \( M \) [22]-[24]. Consider a step-down SCC including a voltage source \( V_{\text{in}} \), a set of \( n \) flying capacitors \( C_j \), and an output capacitor \( C_o \), which is paralleled to load \( R_o \).

The topological interconnection of \( V_{\text{in}} \), \( C_j \), and \( C_o \) are carried out according to the following rules: the connection of \( V_{\text{in}} \) is defined by the coefficient \( A_0 \) in each of the EXB codes for a given \( M \), where “1” indicates a connection. Irrespective of the connection of \( V_{\text{in}} \), the flying capacitors \( C_j \) are always connected serially according to the coefficients \( A_j \) in the EXB codes. The coefficient \( A_j \) represents the connection and the mode of the flying capacitor, \( C_j \), where “1” indicates a discharged and “-1” indicates a charged. A “0” constantly indicates a disconnection.

These rules are illustrated by considering the EXB codes of \( M=5/8 \). In the given example, we use three flying capacitors \( C_1\div C_3 \), \( (n=3) \). Assume that \( C_1 \) is charged to \( V_{\text{in}}/2 \), \( C_2 \) to \( V_{\text{in}}/4 \), \( C_3 \) to \( V_{\text{in}}/8 \), and \( C_o \) to \( M\cdot V_{\text{in}} \). Following the above rules, each EXB code for \( M=5/8 \) leads to a specific connection as depicted in Fig. 1.10 that maintains \( V_o = 5/8 \cdot V_{\text{in}} \).
Fig. 1.10. SCC topologies configured from the EXB codes of $M=5/8$.

Since each of the five configurations of Fig. 1.10 is a one-to-one translation of the EXB code corresponding to $5/8$, and assuming that the capacitors are charged to the binary fractions of the input voltage, the output will be kept at $5/8 \cdot V_{in}$, if the system cycles in perpetuity through these configurations. The KVL equations for the SCC of Fig. 1.10 are:

$$\begin{align*}
V_{in} + 0 &- V_{C2} - V_{C3} = V_{Co} \\
V_{in} &- V_{C1} + V_{C2} - V_{C3} = V_{Co} \\
0 + V_{C1} &+ V_{C2} - V_{C3} = V_{Co} \\
V_{in} &- V_{C1} + 0 + V_{C3} = V_{Co} \\
0 &+ V_{C1} + 0 + V_{C3} = V_{Co}
\end{align*}$$

(1.13)

The system in (1.13) comprises five equations, while the number of unknowns is equal to four. It can be solved by eliminating one of the equations, hence:

$$\begin{align*}
V_{C1} &= 1/2 \cdot V_{in} \\
V_{C2} &= 1/4 \cdot V_{in} \\
V_{C3} &= 1/8 \cdot V_{in} \\
V_{Co} &= 5/8 \cdot V_{in}
\end{align*}$$

(1.14)

Since the solutions in (1.14) are unique [22], [34], the capacitors' voltages are self-adjusting, so that there is no need for any control system to assure that the capacitors reach the nominal value and hence the output will always self-stabilize to the expected voltage. Considering the fact that the set of equations (1.13) is solvable, it should also be solvable if $V_{in}$ and $V_{Co}$ are switched as shown in (1.15). This means switching the input and output functions and converting the step-down SCC to a step-up SCC. The KVL equations for the SCC at step-up configuration are:

$$\begin{align*}
V_{Co} + 0 &- V_{C2} - V_{C3} = V_{in} \\
V_{Co} &- V_{C1} + V_{C2} - V_{C3} = V_{in} \\
V_{Co} + V_{C1} &+ V_{C2} - V_{C3} = 0 \\
V_{Co} &- V_{C1} + 0 + V_{C3} = V_{in} \\
V_{Co} + V_{C1} + 0 &+ V_{C3} = 0
\end{align*}$$

(1.15)
The solutions of equations (1.15) are:

\[
\begin{align*}
V_{C1} &= 4/3 \cdot V_{in}, \\
V_{C2} &= 2/3 \cdot V_{in}, \\
V_{C3} &= 1/3 \cdot V_{in}, \\
V_{C0} &= 8/5 \cdot V_{in}.
\end{align*}
\] (1.16)

The fraction voltages value mentioned at the solutions of equation (1.13) and equation (1.15) remain constant for all EXB codes (x/8 fractions). For the SFN codes, the flying capacitors will stabilize on the average voltages: \( V_{C1} = 3/5 V_{in} \), \( V_{C2} = 2/5 V_{in} \), and \( V_{C3} = 1/5 V_{in} \) at step-down configuration, and for step-up at the average voltages \( V_{C1} = V_{in} \), \( V_{C2} = 2/3 V_{in} \), and \( V_{C3} = 1/3 V_{in} \). For the SGF codes (x/7 fractions), the flying capacitors will stabilize on the average voltages: \( V_{C1} = 4/7 V_{in} \), \( V_{C2} = 2/7 V_{in} \), and \( V_{C3} = 1/7 V_{in} \) at step-down configuration and for step-up at the average voltages \( V_{C1} = 7/4 V_{in} \), \( V_{C2} = 7/2 V_{in} \), and \( V_{C3} = 7 V_{in} \).

### 1.5 Resonant converters and soft switching

Imperfect switching is one of the major contributors to power loss in converters [6]-[10]. Switching devices absorb power when they turn on or off, if they go through a transition when both voltage and current are nonzero (Fig. 1.11a). Another significant drawback of the switch mode operation is the EMI produced due to large \( \text{di/dt} \) and \( \text{dv/dt} \) caused by a switch mode operation. These shortcoming of switch mode converters are exacerbated if the switching frequency is increased in order to reduce the converter size and weight and hence, to increase the power density. Therefore, to realize high switching frequencies in converters, the aforementioned shortcomings are minimized if each switch in a converter changes its status (from on to off or vice versa) when the voltage across it and/or the current through it is zero at the switching instant.

In certain switch mode converter topologies, An LC resonant can be utilized primarily to shape the switch voltage and current in order to provide zero voltage and/or ZCS. In the resonant switching circuits, switching takes place when the voltage and/or current are zero, thus avoiding simultaneous transition of voltage and current and thereby eliminating switching losses, as illustrated in Fig. 1.11b. A circuit employing this technique is known as a resonant converter (or a quasi-resonant converter, if only part of the resonant sinusoid is utilized) and this type of switching is called “soft” switching. A zero current switching circuit shapes the current waveform, while a zero voltage switching (ZVS) circuit shapes the voltage waveform.

Another method for decreasing the switching losses via reducing the overlap between the current and voltage is by adding a network in series with the switches [6]-[9]. By adding switching-aid-networks (called “snubers”), the slop of the voltage and current can be reduced and thereby decrease the overlap between voltage and current by reducing \( \text{dv/dt} \) and \( \text{di/dt} \) (Fig. 1.11a).
Fig. 1.11. Currents and voltages waveforms of the switching modes. (a) Hard switching with and without snubers. (b) Resonant switching. $V_s$ is the voltage across the switch and $I_s$ is the current through the switch.

The switching trajectory in the voltage-current plane of a device is illustrated in Fig. 1.12 comparing the paths for that of a hard-switched operation, hard-switched with adding snubbers, and a soft-switched converter operation. It is indicative of the stresses and losses.

Fig. 1.12 Typical switching loci for a hard-switched converter without switching-aid-networks, with snubbers and for a soft-switched converter operation, ($V_T$ is the voltage across the switch and $I_T$ is the current through it).

One of the main challenges in ZCS method is to maintain the transitions of the switches at the zero points despite the drift of the resonant tank ($RCL$ components) and the delay in the system, i.e., the time duration from zero current detection (ZCD) to when the switching occurs. Moreover, zero crossing point detection systems can be very complicated and have low cost effectiveness.

1.5.1 High power resonant SCC

A type of high-power SCC, characterized by resonant switching transitions, was introduced in [25]. This drastically reduces switching losses and introduces the possibility of employing thyristors instead of turn-off power semiconductors. At the same time, a larger amount of energy can be transferred per switching cycle and the application of the SCC was extended into the megawatt power range. Resonant switching is achieved by placing an inductor between capacitors that are connected in parallel (see Fig. 1.13). This inductor has a much smaller inductance than that of a comparable buck converter and can be realized with an air core, thereby not adding significant weight or losses. Moreover, instead of discharging all pump capacitors simultaneously, the capacitors are discharged in interleaved manner (see Fig. 1.14). This reduces the current stress on the discharging switches and the output capacitor.
Also, the output voltage ripple is significantly reduced. For operation with higher switching frequency the thyristors were replaced by integrated gate-commutated thyristors (IGCTs), which make it possible to avoid a turn-off time in reverse-blocking mode.

The majority of the losses of this converter occur in the semiconductors due to the forward voltage drop. Due to the relatively large number of semiconductors in the resonant SCC topology, the efficiency is not very high at low voltages. Other drawbacks of the topology are the low frequency and relative large number of capacitors and switches per voltage ratio. For high frequency operation, implementation with insulated-gate bipolar transistor (IGBT) will require a complex control system to assure the ZCS because of the component drift in the system.

![Fig. 1.13. High power resonant SCC topology with interleaved, $V_o=V_{in}/5$.](image)

![Fig. 1.14. Waveforms of the high power resonant SCC: (a) capacitors and load currents (b) capacitors and output voltages. Simulations set-up at: $V_{in}=250\text{V}$, $P_{out}=12.5\text{ kW}$, $L_1=8.2\ \mu\text{H}$, $L_2=2.2\ \mu\text{H}$, all flying capacitors $C_f=300\ \mu\text{F}$, and $f_s=1.67\ \text{kHz}$.](image)
1.6 Current sensing

There are many current sensing techniques in dc-dc converters. Every method has its advantages and disadvantages regarding the impact on power losses, number of components, etc. Almost all dc-dc converters and linear regulators sense the inductor current for over-current protection and current-mode control for loop control [7]. Since instantaneous changes in the input voltage are immediately reflected in the inductor current, current-mode control provides excellent line transient response. Another common application for current sensing in dc-dc converters where is the sensed current used to determine when to switch between continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM), which results in an overall increase in the efficiency of the converter. Additional common use for current sensors is ZCD for switching transition at zero points to reduce the switching losses as detailed in Section 1.5.

1.6.1 Current sensors

The basic parameters of any current sensor are linearity, bandwidth, offset (for dc sensors) and sensitivity, and also stability of offset and sensitivity to temperature and time. Current sensors that contain ferromagnetic material also suffer from hysteresis. It is furthermore important for contactless sensors to be insensitive to the actual position of the measured conductor and in addition resistant to external currents and magnetic fields. Some of the typical current sensors will be overviewed [35].

One of the most simple and common techniques is the series sense resistor method (sometimes called current shunt resistor). It simply inserts a sense resistor in a series with the inductor. If the value of the resistor is known, the current flowing through the inductor is determined by sensing the voltage across it. This method obviously incurs a power loss; however, current-sensing resistors are a robust and cheap solution for many applications. The power loss in the resistor can be minimized by amplifying the voltage by op-amp.

Power MOSFETs act as resistors when they are “on” state and they are biased in the Ohmic region. Consequently, the switch current is determined by sensing the voltage across the drain-source of the MOSFET, provided that the $R_{DS}$ of the MOSFET is known. The main drawback of this technique is low accuracy. The $R_{DS}$ of the MOSFET is inherently nonlinear and usually has significant variation caused by temperature, the MOSFET capacitance, and the threshold voltage. In spite of low accuracy, this method is very common in commercially because of its high power efficiency.

Direct-current resistance (DCR) is one low loss and cost method for measuring current; it consists of a series $RC$ network in parallel with the inductor. The correct $RC$ time constant will produce a measurable capacitor voltage that matches the inductor current. However, DCR could run into issues at fast switching frequencies where parasitics arise or when the inductor coil heats up, which increases resistance. Both situations disarrange the tuned circuit network making the measurement less accurate. Figure 1.15 demonstrates the method in a buck converter.
The SENSEFET (sense MOSFET) method is a practical technique for current sensing in new power applications [36], [37]. Current sensing power MOSFETs allow an efficient way to detect the main power current by sampling just a portion of it. This is achieved by isolating the source contact of a selected area; the current is then split between the main power and the SENSEFET cells, which still share the drain and gate contacts with the main device, where the effective width of the sense MOSFET is significantly smaller than the power FET. A complete current sensing circuit using a SENSEFET is shown in Fig. 1.16, where $M_1$ is the power MOSFET and $M_S$ is the SENSEFET. The op amp is used to force the drain voltages of $M_1$ and $M_S$ to be equal and to eliminate the current mirror non-ideality resulting from channel-length modulation. The main drawback of this technique is low accuracy. Due to the high current ratio, even a low degree coupling between $M_1$ and $M_S$ can induce a significant error, and large spikes should be expected in the sense signal during periods of high di/dt. Therefore, proper layout schemes should be chosen to minimize the mutual inductance.

Current transformers are very popular [35] devices and are common in high-power systems. They are very simple and robust, do not require external power, have high galvanic insulation, are cheap, and have a long lifetime with invariant parameters. The idea is to sense a fraction of the high inductor current using the mutual inductor properties of a transformer. A current transformer usually has a bulk ring core made of high-permeability material. The core is wound with high permeability tape (for low-frequency devices) or is made from ferrite (for high-frequency current probes). For high currents, primary winding is usually a single conductor through the core opening. The secondary winding for
most applications is connected to a small ‘burden’ resistor or impedance. In some devices, the secondary current is measured by an active current-to-voltage converter in such a way that the burden is virtually zero. The major drawbacks are increased size and non-integrability. The transformer also cannot transfer the dc portion of current, which renders this method inappropriate for over current protection.

Rogowski coil [35] for measuring current is an air coil wound around the measured current conductor. Stationary Rogowski coils are used to measure ac or transient currents or changes in dc currents. The basic operating principle is given by the mutual inductance $M$ between the primary (single turn) and the secondary (many turns). The output voltage is proportional to the derivative of the current, $u=M \frac{dI}{dt}$. In order to obtain the ac current waveform, a Rogowski coil is used together with an integrator. The Rogowski coil contains no ferromagnetic material, and thus it has excellent linearity and an extremely large dynamic range. Printed circuit board (PCB) technology was used [35] to produce Rogowski coils with a more precise geometry and improved temperature stability.

Further detail for passive and active current sensors can be found in [35].

1.6.2 Zero current detection

A ZCD can be achieved by sensing the current on the resonant tank. A ZCS can be achieved online in real time or offline by measuring the current and comparing to a reference value. The comparing stage can be applied after converting the current to a relative voltage using a comparator. Commonly the signal is rectified and clipped for microprocessor protection. A typical basic ZCD system is described in Fig. 1.17a.

The reference voltage is required to be set according to the delay time of the system (i.e., from the detection to the switching action). In multiphase converters, the slope of the sensed current depends on the circuits’ resonant frequency and peak currents, and can vary from one sub-circuit to another. Hence, a variable reference voltage would assure accurate ZCS at every switching instance. Large differences between the pulse slopes require a wider range of the reference voltage. For a constant time delay, the reference voltage deference, $\Delta V_{ref}$, is proportional to the ratio between $I_{m1}$ to $I_{m2}$ as illustrated in Fig. 1.17b.

Real time solutions [38], [39], demand early triggering to compensate for the delay line that is derived from comparator triggering, decision making in the controller, and driver and gate rise times. Thus, the reference should have a non-zero value. The main drawback of the real time solution is the essential changes in the reference point according to the predicted pulse size. In many multiphase systems, pulse sizes might vary dramatically, posing a problem for choosing the reference point. Offline methods [40] can be done by sampling the sensed signal at time points near an expected crossing, as well as before and after. The switching between states starts by using an initial estimation
based on the known resonance frequency of the designed tank. An estimation and fix can be made as to whether there is a need to increase or decrease the 'on' time of a state and by how much. The downside of the offline calibration solution is the relatively high EMI and switching losses since the converter continues to operate while calibration is being done. Moreover, the demand resources may not always be available for high sampling points. Effective sampling requires many points in the tight time interval around the zero crossing area. Ideally, in both methods, infinite bandwidth is necessary to predict the pulse size without prior knowledge.

![Diagram](image)

**Fig. 1.17.** (a) Typical basic ZCD system configuration (b) Resonant pulses and the reference value.
1.7 Research objectives and significance

The objectives of this thesis are aimed at tackling the fundamental switched capacitor converter issues in several interrelated, major directions.

One of the main objectives of this research is to improve the behavior and performance of SCC applications in the higher power range. The study aims to provide an insight into the practical limitations of multiphase SCC and to provide a soft switching method and a set of design considerations for the selection of the power stage components, for multiple sub-circuit converters.

This was achieved by examination of a complex multiphase SCC topology that produces many target voltages and that use soft switching techniques. This work examined the behavior and performance of a resonant binary/Fibonacci converter with single air core inductor and stray inductances for the medium power range.

The study introduces an active ZCS method for resonant SCC and demonstrates it on a resonant binary/Fibonacci SCC. In order to develop an effective active control system, this study includes a real-time ZCS method, suitable isolated gate driver circuitry that features a wide switching frequency, and a duty cycle range and appropriate passive current detector. The zero detection method was capable of compensating for all the processing delays.

A set of design considerations for the selection of the power stage components for multiple sub-circuit converters has been delineated, and is followed by an implementation example of a multiphase SCC configuration. The design method of multilevel SCCs has been carried out with respect to conduction losses and efficiency and verified on a resonant binary SCC.

The resultant converter has a wide range of conversion ratios with high efficiencies that can be applied to other multi-phase SCC topologies that involve a number of sub-circuits and wide operation ranges at higher power levels.

Further objectives of this study are to introduce efficiently passive soft switching techniques that can simplify the control effort and eliminate additional circuitry involved in active soft-switching controls. A simple and efficient self-commutation concept has been presented and was examined. It consists of a transistor that conducts for the majority of the resonant cycle and a parallel diode that acts as a free-wheeling element, such that turn off occurs at zero current.

This study introduces a unified modeling methodology to describe and explore the loss mechanism of resonant SCCs operating in this ZCS mode. The modeling presented in this study consists on the generic equivalent model and extends it for the case where certain phases in the converter include several paths. The theoretical predictions of the model were compared with cycle-by-cycle simulations and laboratory experiments in various operation modes on unity, double gain, and multiphase Fibonacci resonant SCCs with free-wheeling ZCS.
The model allows the use of the method that exhibits both advantages of inherent ZCS and overcomes the deficiencies of many previous methods, such as high conduction losses and complex control hardware.

These are certainly expanding our understanding of the SCC systems and conceivably have practical uses by designers and users of switch mode converters in general and SCC technology in particular. The results provide not only more natural and straightforward analysis methods, but also highlight the operation conditions that will lead to better design and potentially improved performance of SCC systems up to the higher power ranges.
1.8 Thesis Overview

The research addresses fundamental issues of SCC towards high power density, soft switching, modeling, and analysis. The thesis can be divided into two general areas: Chapters 2 and 3 address issues of SCC applications in the medium and high power ranges. Chapter 4 addresses a modeling and analysis of a resonant SCC with a free-wheeling diode. The technical content of this thesis has been presented in a number of journal and conference articles. Chapters 2 and 3 are based on [1]-[3]. Chapter 4 is based on [5] and earlier results were given in [4].

Chapter 2 proposes a high efficiency resonant multiphase SCC methodology covering several practical issues, including the active zero detection method, current sensing, the zero crossing detection technique, soft start, and isolated gate driver with an appropriate step-by-step design guideline. The active ZCD method is analyzed and demonstrated on a resonant multiphase binary SCC that prohibits high resolution of the target voltages. The converter is simulated and the principals of operation are described.

Chapter 3 focused on the multiphase SCC design guidelines for optimal performance in terms of the desired efficiency. A full analysis and numeric plots of the resonant binary SCC are given. Following the design methodology, two types of experiments were demonstrated on the resonant binary SCC, including the active ZCD method introduced in Chapter 2. Furthermore, the binary converter and the isolated gate driver were constructed with simple means, based on the guideline detailed in Chapter 2 and 3.

Chapter 4 offers a modeling and methodology to describe and explore the loss mechanism of a resonant switched capacitor converter operating in a self-commutation ZCS mode. Throughout the study, the modeling concept will be explained on a unity gain resonant SCC, which highlights the mechanism of divided conduction path operation. The general case of divided conduction path (DCP) applies a free-wheeling mode realized by diode conduction. The model is constructed by considering a series connection of the equivalent resistances and the voltage source between the target voltage and the output port. More general extensions for the model were made and present a closed form to DCP mode for the entire range of the quality factor. The modeling approach is well detailed and demonstrates on several topologies and operation modes, including unity, double gain, and resonant Fibonacci SCC. A very good agreement was found between the values predicted by the model, the simulation, and the experimental results.

Contribution of the thesis and suggestions for future research are discussed in Chapter 5, which summarizes the work.
2.1 Introduction

Switched capacitor converters (SCC) are becoming an attractive alternative in many applications ranging from low to high power. These include voltage regulators for mobile electronic systems, voltage equalizers for batteries and capacitors, for photovoltaic (PV) modules and for automotive applications [13]-[21].

The efficiency of an SCC linearly depends on the proportionality between the output voltage and the target voltage \( \frac{V_o}{V_{\text{Target}}} \) [22]-[24], [29], where \( V_{\text{Target}}=M V_{\text{in}} \) and \( M \) is the no-load voltage transfer ratio. High efficiency can be reached if \( M \) is widely controllable with high resolution. The generic equivalent circuit model for SCC [26], [27] describes the losses by an equivalent resistance connected at the output of the SCC - \( R_{\text{eqT}} \), i.e., \( \eta=\frac{V_o}{V_{\text{Target}}}=\frac{R_o}{(R_o+R_{\text{eqT}})} \).

An effective way to realize many target voltages is the binary/Fibonacci SCC that exhibits a widely controllable conversion ratio [24]. The benefits of a resonant operation with this converter have been demonstrated in [3].

Soft switching in resonant converters can be obtained by switching the transistors at zero current. Given that the resonant frequency depends on the tank's physical parameters, \( C \), \( L \), and \( R \), the switching times can be either calibrated in advance to match the resonant frequency, or a control circuit can be implemented to identify zero crossing. For the case of conventional resonant converters, ZCS operation and its implementation have been widely demonstrated [41]-[45]. For the case of resonant SCC however, few topologies have been proposed e.g., [16]-[21]. A methodological approach to obtain ZCS for the entire dynamic range of the SCC has not been reported hitherto.

The main problem of pre-calibrating resonant SCCs for ZCS is that the physical parameters of the system are prone to drifts throughout the operation range. This is particularly crucial in resonant SCC circuits since the inductance is often implemented by the stray inductance of the circuit, which may vary by design and from one sub-circuit to another while the capacitance values drift as a function of bias voltages and temperature. Hence, an active zero current cross detection circuitry is required to compensate for all inaccuracies and uncertainties of the parameters and to assure ZCS operation.

Another challenge for sensing the current in resonant SCC is the dc component of the resonant current. In this case, the signal is not centered around zero and requires additional processing for zero detection. This can be done using rather costly active sensors or by resistive elements alongside with very high gain bandwidth op-amps [46]-[49].
The objective of this part of the study is to introduce an active ZCS method for resonant SCC and to apply it on a resonant binary/Fibonacci SCC. The resultant converter has a wide range of conversion ratios with high efficiency that can be applied in higher power applications. The diagram of Fig. 2.1 shows the system configuration of the active ZCS converter. A resonant binary/Fibonacci SCC is implemented by adding an inductance at the output of the converter. The converter is capable of either step-up or step-down conversions depending on the source-load orientation. That is, step-up conversion can be obtained by swapping the input and output. For simplicity and without losing generality, the active ZCS method is demonstrated and explained for a binary SCC case.

![Fig. 2.1. Resonant SCC scheme showing the current sensors and analog comparator for zero cross detection.](image)

### 2.2 Principle operation of the resonant binary/Fibonacci SCC

The precursor of the converter of Fig. 2.1 is the hard-switched binary/Fibonacci step-down SCC [22]-[24], which is capable of generating multiple fractional conversion ratios with binary and/or Fibonacci resolution. For a case of three flying capacitors \(n=3\), the converter is capable of producing 19 levels of conversion ratios with high efficiency [24]. To achieve a desired fractional conversion ratio, a specific switching sequence that interconnects the flying capacitors with summing or subtracting action to the source and the output is applied. For example, a conversion ratio of \(M=5/8\), requires EXB codes that are translated to five sub-circuits as illustrated in Fig. 2.2. Following the switching sequence, the average voltages across the flying capacitors and the output voltage will adjust to: 

\[
V_{C1} = (1/2)V_{in}, \quad V_{C2} = (1/4)V_{in}, \quad V_{C3} = (1/8)V_{in}, \quad V_{Co} = (5/8)V_{in}.
\]

Since the solution is unique [24], [34], control is not required to assure that the capacitors have stabilized at their nominal voltages. The voltages of the flying capacitors hold the same average value for any conversion ratio available using the EXB code.

Resonant operation with a sinusoidal current can be obtained by relying on the stray inductances that exist in the conduction path of each sub-circuit. This approach may be impractical in applications where the switching frequency is limited (by the generator or drive losses) [16]-[21]. A more practical approach that is applied in this study is to introduce a single air-core inductor, \(L_s\), in series to the output stage [3], [16]-[21]. By doing so, the same (dominant) inductance is affecting all sub-circuits (see Fig. 2.2). Transition between switching states (sub-circuits) under ZCS conditions can be carried out either
by manual timing of the switching period of each state, or by an active ZCS, that is, measuring the resonant current, detecting a zero current level, and then toggling the switches to the next sub-circuit sequence. Since the resonant characteristics, i.e., the natural frequency and quality factor, of the sub-circuits may vary significantly because of different interconnections of the capacitors, as well as stray inductances, an active method is essential to assure ZCS. This approach also compensates for any parameter variations or drifts due to changes in the operating conditions.

![Resonant SCC sub-circuits configured from the EXB codes of M=5/8.](image)

The contribution of each flying capacitor to the average output current (for \(M=5/8\)) may be derived from the equivalent \(RCL\) circuits of Fig. 2.2. Under steady-state operation, the charge balance of all capacitors is satisfied (i.e., average current equals zero). The sum of the currents for each state \(I_1-I_5\), and the sum of all currents, can be expressed as:

\[
\begin{align*}
0 - I_2 + I_3 - I_4 + I_5 &= 0 ; \quad C_1 \\
-I_1 + I_2 + I_3 + 0 + 0 &= 0 ; \quad C_2 \\
-I_1 - I_2 - I_3 + I_4 + I_5 &= 0 ; \quad C_3 \\
I_1 + I_2 + I_3 + I_4 + I_5 &= I_o ;
\end{align*}
\]

where the currents \(I_j\) are average currents of each sub-circuit (averaged over the entire switching period).

Table 2.1 summarizes the expected currents for various conversion ratios that were obtained by solving a set of equations similar to (2.1). In each case \(k_j\) is the proportional coefficient between the average current of the flying capacitor and output current for state \(j\), namely, \(I_j = k_jI_{out}\). Duality can be observed between ratios 1/8 to 7/8 and 3/8 to 5/8.

The results of Table 2.1 indicate that, for a given sub-circuit, the average currents vary considerably between the switching state and in some cases, a negative current may exist in one of the states. This implies, however, that for some conversion ratios, one of the states discharges the output capacitor. The extra circulating current will increase the losses. The variability of the average currents between the states adds extra burden to the zero detection circuitry. Obviously, parallel connection of two flying capacitors must be avoided when transitioning between two sub-circuits. This is done to eliminate a large current spike that may damage the system.
Table 2.1 - Solutions of the Average Capacitor Currents for Various Ratios

<table>
<thead>
<tr>
<th>Proportional Coefficient</th>
<th>$M$</th>
<th>$k_1$</th>
<th>$k_2$</th>
<th>$k_3$</th>
<th>$k_4$</th>
<th>$k_5$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1/8</td>
<td>1/8</td>
<td>1/8</td>
<td>1/4</td>
<td>1/2</td>
<td>--</td>
</tr>
<tr>
<td></td>
<td>3/8</td>
<td>-1/8</td>
<td>3/8</td>
<td>1/2</td>
<td>0</td>
<td>1/4</td>
</tr>
<tr>
<td></td>
<td>5/8</td>
<td>1/4</td>
<td>3/8</td>
<td>-1/8</td>
<td>0</td>
<td>1/2</td>
</tr>
<tr>
<td></td>
<td>7/8</td>
<td>1/2</td>
<td>1/4</td>
<td>1/8</td>
<td>1/8</td>
<td>--</td>
</tr>
</tbody>
</table>

To illustrate the operation of the resonant SCC, typical currents and voltages waveforms are depicted in Fig. 2.3 for the case of $M=5/8$. It can be observed that the average currents of the flying capacitors are zero, their voltages are stabilized, and that the dc output current is built up by the contribution of all sub-circuits that, in turn, are connected to the load for half a resonant period. The portion of negative current is also observed.

![Waveforms](image)

Fig. 2.3. Resonant binary SCC (a) Capacitors and output stage current waveforms. (b) Capacitors and output voltages waveforms. PSIM Simulations set-up at: $M=5/8$, $V_{in}=100$ V, $P_{out}=100$ W, $L_s=200$ nH, all flying capacitors $C_f=9.4$ µF, and $f_s=90$ kHz. S5 is the normalized switch gate-source control voltages, $I_{C1}$, 2, 3 are the currents through the flying capacitors $C_1$, $C_2$ and $C_3$, $I_{Ls}$ is the inductor current at the output stage, and $I_{out}$ is the load current. $V_{C1}$, 2, 3 are the capacitor voltages across the flying capacitors and $AVG(V_{C1}$, 2, 3) are the average voltages.

### 2.3 Practical implementation

To realize cost-effective resonant operation for the SCC of Fig. 2.1, that is, to obtain soft switching of all switches for all transitions between sub-circuits, the following challenges need to be addressed:

- The seemingly natural current sensing point, the series inductance to the output, contains a dc component.
The resonant characteristics (natural frequency and quality factor) are considerably different from one sub-circuit to another. This is due to different interconnections of the flying capacitors according to the EXB code (e.g., Fig. 2.2).

Uncertainties and variations of the parameters (inductance and capacitance) may be very large. Especially for different operating conditions (conversion ratio and power levels).

The average and the peak current are not constant for each sub-circuit and for a given state at different power ratings.

Zero current detection at the crossing point is impractical due to a poor signal-to-noise (SNR) ratio and the time delay from detection to commutation of the switches. Selection of the reference depends on the above arguments.

Gate drive circuitry to assure the operation of a large number of floating switches.

Considerations for components selection based on the expected losses of the system (further discussed in Chapter 3).

To overcome these challenges, a ZCD and control circuitry was developed in this study and is schematically described in Fig. 2.1. It includes a current sensor for each of the flying capacitors, a comparator module, microcontroller, and decoders. The transition between switching states of the EXB code is governed by comparing the resonant currents to specified references. These are discussed in this section, which also addresses issues of limiting the inrush current, stabilizing the capacitors’ voltages after startup, and the realization of simple and efficient floating gate drivers of the power switches.

### 2.3.1 Current sensing and zero crossing detection

To eliminate the need for a rather costly, active current sensing circuitry that accommodates dc current, passive magnetic current transformers are placed on all three flying capacitors.

Since the aim of the current sensing is the detection of the zero crossing point rather than regulation, the dc component of the current is not of interest. The reason for the apparent redundancy in the current measurements is that there is no single capacitor that participates in all the states for all voltage ratio configurations. In the example shown in Fig. 2.2 of 5/8, \( C_3 \) participates in all the states, but for other ratios, such as 2/8, it is omitted. By having three sensors, current can be read from any active capacitor.

A conventional passive magnetic sensor has been utilized for zero detection. This exemplary practice may seem against the original concept for using SCC technology to avoid magnetic components. Fortunately, since current sensing is aimed purely for detection of the current zero crossing point, only the shape of the current signal in the vicinity of zero is of interest. This implies that weakly coupled, i.e., coreless, sensors may be employed [50].
A comparator module that is integrated in a microcontroller was utilized in this work for current detection. Since the comparator is a part of the integrated circuit (IC) and prohibits negative voltages, the sensed current was first rectified and then converted to a proportional voltage using a resistor $R_{\text{sense}}$. To protect the I/O ports of the digital controller and since only the information in the vicinity of zero current is of interest, the rectified signal is clamped to the voltage rails by diodes. The series resistor is used to limit the current to the controller. By taking these measures of precaution, the resistor $R_{\text{sense}}$ can be selected to the worst-case for the state of the lowest current.

At steady-state, the switching command is initiated by the analog comparator module. The comparator output triggers an auxiliary interrupt upon zero detection in which the switching state of the next sub-circuit is applied on the transistors, and if required, changes the path selector of the MUX for next state.

### 2.3.2 Reference voltage

As mentioned above, the comparator reference voltage cannot be zero since finite response time, $t_d$, exists in the control system – i.e., delay time from detection to actual switching action. The reference voltage is set to compensate for $t_d$ and for the slope of the sensed current [38]. Figure 2.4 shows the typical difference between two state pulses being sensed. Assuming a high quality factor ($Q>3$), the reference voltage, as a function of the resonant peak and time duration can be expressed as:

$$V_{\text{ref },j} = \frac{I_{mj}}{n} \sin \left( 2\pi \left[ \frac{1}{2} - \frac{t_d}{t_{oj}} \right] \right) R_{\text{sense}},$$

where $n$ is the current transformer-winding ratio, $I_{mj}$ is the flying capacitors currents, $t_{oj}$ is the resonant period, and $j \in \{1,2,3,4\}$ is state indicator. The peak value of the sensed signal is translated into voltage by $V_{mj} = (I_{mj}/n) R_{\text{sense}}$.

The slope of the sensed current depends on the circuits’ resonant frequency and peak currents and varies from one sub-circuit to another. A variable reference voltage would assure accurate ZCS at every switching instance. However, this requires an extremely fast control loop to obtain the information of the state current on-the-fly [39]. To avoid this complexity, a compromise is made based on the expected variations in the currents due to the operation in different sub-circuits and parameters variations. It allows setting of a constant reference voltage with the penalty of mismatch in the switching with respect to the zero crossing point. Considering an extreme worst-case slope variation as depicted in Fig. 2.4 of a 400% increase in peak current and a 200% increase in the resonant period, and that $t_d$ is approximately $0.1t_{oj}$, the ratio between the worst-case reference ($V_{\text{ref1}}$) and the nominal reference voltage ($V_{\text{ref2}}$) can be obtained using equation (2.2), that is:
\[
\begin{align*}
V_{\text{ref1}} &= \frac{4I_{m_1}}{n} \sin \left( 2\pi \left( \frac{1}{2} - \frac{0.1t_{o1}}{2t_{o1}} \right) \right) R_{\text{sense}} \\
V_{\text{ref2}} &= \frac{I_{m_2}}{n} \sin \left( 2\pi \left( \frac{1}{2} - \frac{0.1t_{o1}}{t_{o1}} \right) \right) R_{\text{sense}} = 2.1,
\end{align*}
\] (2.3)

which translates into an absolute maximum mismatch in the switching time of 0.1\(t_{o1}\). Provided that the operation of each sub-circuit is in the range of microseconds, the result of equation (2.3) implies a small deviation from the true zero crossing point, allowing the use of a fixed reference voltage.

![Diagram](image)

Fig. 2.4. Worst-case conditions of state current variation and the mismatch of the switching instance due to fixed reference settings.

In this work, the reference voltage and the sensing gain are selected such that the true ZCS is obtained at higher power levels (higher states’ currents), and the small mismatches in the ZCS will be at lower power levels. To allow operation in a wide range of power levels and input voltage variations and still work in the vicinity of ZCS, a coarse tuner to switch between operation ranges is realized. The scaling of the sensing gain is implemented by voltage dividers branching out to the MUX (Fig. 2.1).

Another consideration when setting a low reference value is the need to avoid the ground noise caused by imperfect switching at nonzero, common-mode, etc. that may result in erroneous triggering of the comparator. This is overcome by a blanking period of the comparator after the switching action, as done in many commercial current sensing oriented applications.

### 2.3.3 Stabilizing the flying capacitors voltage on startup

The design of the active ZCS method and circuitry assumes that the voltages of all capacitors have stabilized to their nominal values (binary fractions). Applying the above zero detection method (demonstrated in detail in the next section), assures that at steady-state ZCS is realized for all conversion ratios and over a wide operation range of input voltage and power levels. In a practical turn-on situation, the capacitors’ voltages are zero. This results in high inrush currents if the converter is allowed to operate in the vicinity of the steady-state resonant frequency. Moreover, relying on the
comparator to trigger commutation is impractical since the inrush current profile may not be of a resonant nature. To remedy this, a voltage-stabilizing and current-limiting sequence is required to limit the flying capacitors currents to a safe value and to bring the flying capacitors voltages to their steady-state value.

In this study, as shown in Fig. 2.5, a voltage-stabilizing and current-limiting method that is based on the operation of the binary converter is applied. The concept is to rely on the EXB codes to assure stabilization of the capacitors’ voltages to the correct values and to limit the inrush current by controlling the switching frequency; this is done as follows: at startup the switching times are made significantly shorter than the resonant period such that the peak current does not exceed a set maximum value. This is done for few cycles until the voltage across the capacitors has stabilized. Then, a second switching sequence that is adjusted to the estimated resonant values is applied for few cycles to ease the transition to active current sensing. At the end of this phase, the ZCS circuitry is activated and transition between sub-circuits is governed by the comparator output.

![Diagram](image.png)

Fig. 2.5. Conceptual operation of the soft start sequences for $M=3/8$ (resonant current): (a) high-frequency switching; (b) estimated resonant values; (c) active ZCS method.

### 2.3.4 Switches and isolated gate drivers

To facilitate all the interconnections of the flying capacitors as prescribed in the EXB codes [22]-[24] for all conversion ratios, the converter includes twelve four-quadrant switches (see Fig. 2.1). Each switch is realized by two N-channel power MOSFETs with the gate and sources interconnected as depicted in Fig. 2.6.

Isolated gate drivers are required to allow high input voltage operation. As depicted in Fig. 2.6, the gate driver structure used in this study consists of a 1:1 pulse transformer for isolation, a dc blocking capacitor $C_1$ to prevent the dc content of the gate drive from passing through the pulse transformer, $C_2$ and $D_2$ to restore the dc level at the secondary side, capacitor $C_3$ that acts as independent floating supply, and NPN and PNP transistors connected in a push-pull configuration.

Assuming that the voltages across $C_2$ and $C_3$ are stable, the operation of the gate driver may be described as follows: at turn on (see Fig. 2.7a) $V_p$ is positive which turns on $Q_1$, partially discharging $C_3$ upon $C_{GS}$, to turn on the MOSFET. Once $D_1$ starts conducting, $C_3$ recharges through $C_2$ and $D_1$. The independent supplier $C_3$ provides a quick charging of $C_{GS}$ and therefore, the rise time is relatively fast. At turn off (see Fig. 2.7b) $V_p$ is negative, $D_2$ is forward biased, and $C_2$ now charges in the opposite
direction through $D_2$. In addition, $C_{GS}$ discharges through $Q_2$ that is saturated, turning off the MOSFET. $R_2$ damps potential overshoots that may occur due to stray inductances.

For construction and component selection of the isolated gate driver of Fig. 2.6, the following procedure is suggested:

- Given a power transistor with specified gate charge requirements ($Q_{gate}$) and provided the turn on/off transition time $t_r$, the required peak current of the low-side driver can be estimated as:

$$ I_{pk} = \frac{Q_{gate}}{t_r}, \quad (2.4) $$

- The effective magnetic area, $A_e$, for the isolation transformer is calculated based on the maximum flux density that is allowed, $B_{max}$, resulting from the maximum on time $t_{on}$, that is defined by the resonant period of the system. To comply with the specification sheets of commercial compact pulse transformers, the voltage-time product has been defined as the target parameter as:

$$ nA_eB_{max} = V_{GS} t_{on}, \quad (2.5) $$

where $V_{GS}$ is the applied gate voltage and $n$ is the number of turns at the secondary winding.

- Resistors $R_1$ and $R_2$ (optional) are selected to damp oscillations and avoid high peak currents that may appear due to the stray inductances and the total gate capacitance. These are typically applied using manual trim.

- The dc blocking and restoring capacitors $C_1$ and $C_2$ are selected to sustain the average drive voltage per switching cycle.

- Capacitance $C_3$ is required to be sufficiently high to allow charging of $C_{GS}$ while sustaining the required gate voltage, that is:

$$ C = \frac{I_{av}}{\Delta V \cdot f_s}, \quad (2.6) $$

where $I_{av}$ is the average capacitor current, and $\Delta V$ is the voltage ripple of the capacitor.

- Transistors $Q_1$ and $Q_2$ are selected to sustain the gate peak current with the repetitive rate of switching frequency.

The components values (see Table 3.1) used in the experimental prototype are: $C_1=C_2=C_3=1 \ \mu F$, $R_1=3.3 \ \Omega$, $R_2=33 \ \Omega$. The operation of the experimental floating drivers has been verified at switching frequency in the range of 30-350 kHz, wide duty cycle range of 0.1-0.9, and rise and fall times of approximately 200 ns. Figure 2.8 demonstrated the driver output signal, $V_{Gate}$, voltages of capacitors $C_2, C_3$, and the voltage across diode $D_2$.  

31
Fig. 2.6. Isolated Gate Driver and four-quadrant switch using N-channel power MOSFETs.

Fig. 2.7. Operation modes: (a) on state - CGS charging (b) off state - CGS Discharging.

Fig. 2.8. Experimental waveforms of the isolated gate driver: (a) $C_3$ voltage (5 V/div). (b) $C_2$ voltage (2 V/div). (c) $D_2$ voltage (5 V/div). (d) output voltage, $V_{\text{Gate}}$ (5 V/div). Horizontal scale (10 µs/div).
2.4 Conclusions

A resonant binary and Fibonacci step-up/down converter was introduced. The soft switching method is based on inserting one air core inductor or the use of parasitic inductance and with an active zero detection method. The major challenge in the design of a resonant binary SCC is the significant variation in switching times that is required for soft-switching operation. This variation is present when switching between one sub-circuit to another that may involve a different number of capacitors in a series, which therefore, changes the resonant period. Another source for different resonant periods is that the capacitance and inductance values are strongly dependent on the operating conditions. This means that the time period of a given sub-circuit is not constant for variations in the power level or the input voltage, and this rules out any non-instantaneous ZCS or pre-calibrated resonant operation. The method can be implemented with most of the switch capacitor topologies for reducing conduction losses and EMI noises. Furthermore, the converter reduces the power losses by increasing the number of target voltages. The proposed converter is a viable approach for medium and high step-up/down power systems, despite of the large number of switches.
Chapter 3 - Design of the Multiphase Resonant Switched-Capacitor Converters

3.1 Introduction

The objective of this part of the study is to set the design guideline considerations and rules for the selection of the power stage components, for multiple sub-circuit converters. The proposal methodology is based on the generic equivalent model of the soft switching case [27]. The design method of multilevel SCCs with respect to conduction losses and efficiency was demonstrated on the resonant binary SCC. This topology was analyzed and two types of experiments were constructed to examine the design methodologies.

3.2 Equivalent resistance – considerations for components selection

The primary contributor of losses for the ZCS resonant binary/Fibonacci SCC under study is the conduction losses in each sub-circuit. When combined together, the total equivalent resistance is a good tool to predict the system efficiency based on the system parameters. Examination of the losses based on the generic equivalent modeling approach of [26], [27] adds practical insight to determine the size of the power transistors (on resistance) and the required characteristic impedance (capacitance-inductance ratio). There, the equivalent resistance is represented as a function of the resonant characteristics of the system. In this study, the methodology presented in [26], [27] for a simplistic case of a unity converter has been adapted to estimate the equivalent resistance of the resonant binary/Fibonacci SCC that includes multiple sub-circuits per operation cycle.

Given that each stage for all EXB/SFN/SGF codes consists of four dual switches in the conduction path, without loss of generality, the total parasitic loop resistance for every sub-circuit \( R_{\text{loop},j} \), is approximated to \( 8R_{\text{DS(on)}} \) (neglecting the ESR and other stray resistances). The total equivalent resistance \( R_{eqT} \) in its generic form can be expressed as a function of the sub-circuits’ quality factors \( Q_j \) [27] by summation of the equivalent resistances in all sub circuits, that is:

\[
R_{eqT} = \sum_{j=1}^{n} k_j \frac{2\pi \cdot Q_j^2 \cdot R_{\text{loop},j}}{\text{df}_j \sqrt{4Q_j^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_j^2 - 1}} \right),
\]

where \( \text{df}_j = f_s / f_d \), is the ratio between the switching frequency, \( f_s \), to the damped resonant frequency, \( f_d \), for each sub-circuit, and \( j \) is the sub-circuit index.

Since the case under study involves multiple sub-circuits with different numbers of serially connected capacitors, which results in different values of \( Q_j \) (as can be observed from the sub-circuits of Fig. 2.2), a direct calculation of expression (3.1) based on the system specific values has several degrees of freedom and is therefore quite complex. To achieve a more convenient representation of
expression (3.1), the following manipulations are applied: 1) $R_{eqT}$ is normalized to $R_{loopj}$ (which is assumed to be identical for all sub-circuits); 2) $Q_j$ is represented as a function of the lowest possible quality factor of all sub-circuits (defined as $Q_{j,low}$). The value of $Q_{j,low}$ is obtained from the sub-circuit with the smallest number of serially connected capacitors; 3) $df_j$ is represented by the $df$ of the sub-circuit from which $Q_{j,low}$ is obtained (defined as $df_{j,low}$). These mathematical relationships significantly reduce the complexity of expression (3.1) to two degrees of freedom ($Q_{j,low}$ and $df_{j,low}$) and can be used to represent the worst-case design conditions from which the maximum losses can be estimated, per conversion ratio.

To exemplify the normalization procedure and plot the resultant $R_{eqT}$, consider the case of $M=5/8$ in which $C_{t1}=C_{t4}=C/2$, $C_{t2}=C_{t3}=C/3$, and $L_{ej}=L_e$. This leads to $Q_{j,low} = Q_1$, $Q_2 = \sqrt{3/2} \cdot Q_1$, $df_{j,low} = df_1$, $df_2 = \sqrt{2/3} \cdot df_1$, and the expression (3.1) can be rewritten in the normalized form as:

$$
\frac{R_{eqT}}{R_{loopj}} = k_1^2 \frac{2\pi \cdot Q_1^2}{df_1 \cdot \sqrt{4Q_1^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_1^2 - 1}} \right) + k_2^2 \frac{3\pi \cdot Q_1^2}{\sqrt{2/3} \cdot df_1 \cdot \sqrt{6Q_1^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{6Q_1^2 - 1}} \right) +
$$

$$
+ k_3^2 \frac{3\pi \cdot Q_1^2}{\sqrt{2/3} \cdot df_1 \cdot \sqrt{6Q_1^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{6Q_1^2 - 1}} \right) + k_4^2 \frac{2\pi \cdot Q_1^2}{df_1 \cdot \sqrt{4Q_1^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_1^2 - 1}} \right) .
$$

(3.2)

Following the same procedure, the worst-case total equivalent resistances for several conversion ratios ($M=1/8$, 3/8, 5/8, and 7/8) have been obtained and were numerically plotted as a function of $Q_{j,low}$ for several values of $df_{j,low}$ and are shown in Fig. 3.1. It can be observed that the normalized $R_{eqT}$ asymptotically reaches a constant value for $Q_{j,low}$ values higher than 3. This implies that the lowest possible losses can be obtained, even with fairly small inductances, thus allowing the use of stray inductance or a coreless element. It can also be observed that a quality factor lower than unity increases $R_{eqT}$. This can be explained by the fact that when $Q<1$, the operation is no longer resonant and the rms value of the circulating current significantly increases. Another observation from Fig. 3.1 is that a higher value of $df_j$ (less damped circuit) is preferable in order to obtain lower conduction losses.

Based on the above-mentioned observations and mathematical extraction, the following design procedure is proposed and demonstrated on a case of three flying capacitors:

- For the highest expected conversion ratio (smallest fraction), a worst-case $Q_{j,low}$ and $df_{j,low}$ is selected for the sub-circuit with the smallest number of serially connected capacitors.
- From Fig. 3.1, $R_{eqT}$ is extracted. Alternatively, equation (3.1) and the above-mentioned order reduction procedure can be used.
- Given a desired target efficiency, the upper boundary for $R_{DS(on)}$ is extracted according to the efficiency expression, that is:
\begin{equation}
\eta = \frac{R_e}{R_0 + R_{eqT}} \rightarrow \frac{R_e}{R_{DS(on)}} = \frac{1}{\eta} \left( 1 - \alpha \right), \quad \alpha \approx \frac{R_{eqT}}{8R_{DS(on)}}.
\end{equation}

For a reduced volume design, an sufficiently small inductance value is chosen that can be realized by the parasitics or realized without a magnetic core.

The required capacitance is calculated to satisfy the worst-case \(Q_{j,\text{low}}\).

In the case of the resultant resonant frequency (equal to the switching frequency due to the active ZCS) exceeding a practical value either due to drive losses or driver realization, \(L\) and \(C\) are recalculated by iterating the two previous steps.

Once the power transistors have been selected, the gate drive losses can be estimated as:

\begin{equation}
P_{\text{gate,loss}} = V_{GS} Q_{\text{gate}} f_s.
\end{equation}

where \(V_{GS}\) is the gate driver voltage, \(f_s\) is the switching frequency, and \(Q_{\text{gate}}\) is the total gate charge of the selected MOSFET.

Fig. 3.1. Worst-case plot of the normalized equivalent resistance as a function of \(Q_{j,\text{low}}\), for conversion the ratios: (a) \(M=1/8, 3/8\), and (b) \(M=5/8, 7/8\) for \(df\), in the range of 0.15-0.35 (0.05 step each iteration in \(df\)). The curves were extracted numerically using MATLAB.
3.3 Analysis and numerical plots

This section provides more details for all conversion ratios and sub-states of the resonant binary SCC. Solutions of the average currents of the capacitors and the total capacitance per state are summarized in Table 3.1.

<table>
<thead>
<tr>
<th>EXB Codes</th>
<th>Proportional Coefficient</th>
<th>C_Total</th>
<th>EXB Codes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/8</td>
<td>1/8</td>
<td>1/8</td>
<td>2/8</td>
</tr>
<tr>
<td>2/8</td>
<td>1/4</td>
<td>C/2</td>
<td>C/2</td>
</tr>
<tr>
<td>3/8</td>
<td>-1/8</td>
<td>C/3</td>
<td>C/3</td>
</tr>
<tr>
<td>4/8</td>
<td>1/2</td>
<td>C/3</td>
<td>C/2</td>
</tr>
<tr>
<td>5/8</td>
<td>1/4</td>
<td>C/3</td>
<td>C/3</td>
</tr>
<tr>
<td>6/8</td>
<td>1/4</td>
<td>C/2</td>
<td>C/2</td>
</tr>
<tr>
<td>7/8</td>
<td>1/2</td>
<td>C/3</td>
<td>C/3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SFN Codes</th>
<th>Proportional Coefficient</th>
<th>SFN Codes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/5</td>
<td>1/5</td>
<td>1/5</td>
</tr>
<tr>
<td>1/3</td>
<td>1/3</td>
<td>C/2</td>
</tr>
<tr>
<td>2/5</td>
<td>1/5</td>
<td>C/3</td>
</tr>
<tr>
<td>1/2</td>
<td>1/2</td>
<td>--</td>
</tr>
<tr>
<td>3/5</td>
<td>1/3</td>
<td>C/2</td>
</tr>
<tr>
<td>2/3</td>
<td>1/3</td>
<td>C/3</td>
</tr>
<tr>
<td>4/5</td>
<td>1/5</td>
<td>C/2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SGF Codes</th>
<th>Proportional Coefficient</th>
<th>SGF Codes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/7</td>
<td>3/7</td>
<td>1/7</td>
</tr>
<tr>
<td>2/7</td>
<td>3/7</td>
<td>C/2</td>
</tr>
<tr>
<td>3/7</td>
<td>1/7</td>
<td>C/2</td>
</tr>
<tr>
<td>4/7</td>
<td>3/7</td>
<td>C/2</td>
</tr>
<tr>
<td>5/7</td>
<td>1/7</td>
<td>C/2</td>
</tr>
<tr>
<td>6/7</td>
<td>1/7</td>
<td>C/2</td>
</tr>
</tbody>
</table>

Table 3.1 - Solutions of the Average Capacitors Currents for All Ratios and Total Capacitance per Phase

Tables 3.2-3.4 summarize the normalized forms of the equivalent resistors of all conversion ratios. The dominant part of any equivalent resistor contains the worst-case \(Q_{j,\text{low}}\) and \(df_{j,\text{low}}\) and furthermore this part is multiple with the highest value of the proportional factor, \(k_j\). The highest \(k_j\) factor is related to the lowest \(Q_j\) since this phase includes the highest equivalent capacitance value (sub-circuit with the smallest number of serially connected capacitors where \(R_{\text{loop}}\) and \(L_o\) are constant).
### Table 3.2 - Normalized Form of the Equivalent Resistors of the EXB Codes

<table>
<thead>
<tr>
<th>M</th>
<th>( \frac{R_{eq}}{R_{loop}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/8</td>
<td>( k_1^2 \left( \frac{6\pi Q_i^2}{\sqrt{1/3} \cdot df_i \sqrt[4]{Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{12Q_i^3} - 1} \right) + k_2^2 \left( \frac{6\pi Q_i^2}{\sqrt{1/3} \cdot df_i \sqrt[4]{Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{12Q_i^3} - 1} \right) + k_3^2 \left( \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df_i \sqrt[4]{Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{8Q_i^3} - 1} \right) + k_4^2 \left( \frac{2\pi Q_i^2}{df_i \sqrt[4]{Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{4Q_i^3} - 1} \right) )</td>
</tr>
<tr>
<td>2/8</td>
<td>( k_1^2 \left( \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df_i \sqrt[4]{Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{8Q_i^3} - 1} \right) + k_2^2 \left( \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df_i \sqrt[4]{Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{8Q_i^3} - 1} \right) + k_3^2 \left( \frac{2\pi Q_i^2}{df_i \sqrt[4]{Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{4Q_i^3} - 1} \right) )</td>
</tr>
<tr>
<td>3/8</td>
<td>( k_1^2 \left( \frac{3\pi Q_i^2}{\sqrt{2/3} \cdot df_i \sqrt[4]{6Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{6Q_i^3} - 1} \right) + k_2^2 \left( \frac{3\pi Q_i^2}{\sqrt{2/3} \cdot df_i \sqrt[4]{6Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{6Q_i^3} - 1} \right) + k_3^2 \left( \frac{2\pi Q_i^2}{df_i \sqrt[4]{4Q_i^3 - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{4Q_i^3} - 1} \right) + k_4^2 \left( \frac{2\pi Q_i^2}{df_i \sqrt[4]{4Q_i^3 - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{4Q_i^3} - 1} \right) )</td>
</tr>
<tr>
<td>4/8</td>
<td>( k_1^2 \left( \frac{2\pi Q_i^2}{df_i \sqrt[4]{Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{4Q_i^3} - 1} \right) + k_2^2 \left( \frac{2\pi Q_i^2}{df_i \sqrt[4]{Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{4Q_i^3} - 1} \right) )</td>
</tr>
<tr>
<td>5/8</td>
<td>( k_1^2 \left( \frac{2\pi Q_i^2}{df_i \sqrt[4]{Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{4Q_i^3} - 1} \right) + k_2^2 \left( \frac{3\pi Q_i^2}{\sqrt{2/3} \cdot df_i \sqrt[4]{6Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{6Q_i^3} - 1} \right) + k_3^2 \left( \frac{3\pi Q_i^2}{\sqrt{2/3} \cdot df_i \sqrt[4]{6Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{6Q_i^3} - 1} \right) + k_4^2 \left( \frac{2\pi Q_i^2}{df_i \sqrt[4]{4Q_i^3 - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{4Q_i^3} - 1} \right) )</td>
</tr>
<tr>
<td>6/8</td>
<td>( k_1^2 \left( \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df_i \sqrt[4]{8Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{8Q_i^3} - 1} \right) + k_2^2 \left( \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df_i \sqrt[4]{8Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{8Q_i^3} - 1} \right) + k_3^2 \left( \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df_i \sqrt[4]{8Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{8Q_i^3} - 1} \right) )</td>
</tr>
<tr>
<td>7/8</td>
<td>( k_1^2 \left( \frac{2\pi Q_i^2}{df_i \sqrt[4]{Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{4Q_i^3} - 1} \right) + k_2^2 \left( \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df_i \sqrt[4]{8Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{8Q_i^3} - 1} \right) + k_3^2 \left( \frac{6\pi Q_i^2}{\sqrt{1/3} \cdot df_i \sqrt[4]{12Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{12Q_i^3} - 1} \right) + k_4^2 \left( \frac{6\pi Q_i^2}{\sqrt{1/3} \cdot df_i \sqrt[4]{12Q^3_i - 1}} \right) \tanh \left( \frac{\pi}{2\sqrt{12Q_i^3} - 1} \right) )</td>
</tr>
<tr>
<td>M</td>
<td>( \frac{R_{eq}}{R_{loop}} )</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>1/5</td>
<td>( k_i^2 \frac{2\pi Q_i^2}{df, \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df, \sqrt{8Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df, \sqrt{8Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + k_i^2 \frac{6\pi Q_i^2}{\sqrt{1/3} \cdot df, \sqrt{12Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{12Q_i^2 - 1}} \right) )</td>
</tr>
<tr>
<td>1/3</td>
<td>( k_i^2 \frac{2\pi Q_i^2}{df, \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df, \sqrt{8Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + k_i^2 \frac{2\pi Q_i^2}{df, \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) )</td>
</tr>
<tr>
<td>2/5</td>
<td>( k_i^2 \frac{2\pi Q_i^2}{df, \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df, \sqrt{8Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + k_i^2 \frac{6\pi Q_i^2}{\sqrt{1/3} \cdot df, \sqrt{12Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{12Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df, \sqrt{8Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) )</td>
</tr>
<tr>
<td>1/2</td>
<td>( (k_i^2 + k_i^2) \frac{2\pi Q_i^2}{df, \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) )</td>
</tr>
<tr>
<td>3/5</td>
<td>( k_i^2 \frac{2\pi Q_i^2}{df, \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df, \sqrt{8Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + k_i^2 \frac{6\pi Q_i^2}{\sqrt{1/3} \cdot df, \sqrt{12Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{12Q_i^2 - 1}} \right) )</td>
</tr>
<tr>
<td>2/3</td>
<td>( k_i^2 \frac{2\pi Q_i^2}{df, \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df, \sqrt{8Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + k_i^2 \frac{2\pi Q_i^2}{df, \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) )</td>
</tr>
<tr>
<td>4/5</td>
<td>( k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df, \sqrt{8Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df, \sqrt{8Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2} \cdot df, \sqrt{8Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + k_i^2 \frac{2\pi Q_i^2}{df, \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) )</td>
</tr>
</tbody>
</table>
### Table 3.4 - Normalized Form of the Equivalent Resistors of the SGF Codes

<table>
<thead>
<tr>
<th>M</th>
<th>( R_{eq}/R_{loop} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/7</td>
<td>[ k_i^2 \frac{2\pi Q_i^2}{\text{df} \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi^2}{\text{df} \sqrt{8Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) ] + [ k_i^2 \frac{6\pi Q_i^2}{\sqrt{1/3 \cdot \text{df} \sqrt{12Q_i^2 - 1}}} \tanh \left( \frac{\pi}{2\sqrt{12Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2 \cdot \text{df} \sqrt{8Q_i^2 - 1}}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) ]</td>
</tr>
<tr>
<td>2/7</td>
<td>[ k_i^2 \frac{2\pi Q_i^2}{\text{df} \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi^2}{\text{df} \sqrt{8Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + ] + [ k_i^2 \frac{6\pi Q_i^2}{\sqrt{1/3 \cdot \text{df} \sqrt{12Q_i^2 - 1}}} \tanh \left( \frac{\pi}{2\sqrt{12Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2 \cdot \text{df} \sqrt{8Q_i^2 - 1}}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) ]</td>
</tr>
<tr>
<td>3/7</td>
<td>[ k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2 \cdot \text{df} \sqrt{8Q_i^2 - 1}}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + k_i^2 \frac{6\pi Q_i^2}{\sqrt{1/3 \cdot \text{df} \sqrt{12Q_i^2 - 1}}} \tanh \left( \frac{\pi}{2\sqrt{12Q_i^2 - 1}} \right) + ] + [ k_i^2 \frac{2\pi Q_i^2}{\text{df} \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2 \cdot \text{df} \sqrt{8Q_i^2 - 1}}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) ]</td>
</tr>
<tr>
<td>4/7</td>
<td>[ k_i^2 \frac{2\pi Q_i^2}{\text{df} \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi^2}{\text{df} \sqrt{8Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + ] + [ k_i^2 \frac{6\pi Q_i^2}{\sqrt{1/3 \cdot \text{df} \sqrt{12Q_i^2 - 1}}} \tanh \left( \frac{\pi}{2\sqrt{12Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2 \cdot \text{df} \sqrt{8Q_i^2 - 1}}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) ]</td>
</tr>
<tr>
<td>5/7</td>
<td>[ k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2 \cdot \text{df} \sqrt{8Q_i^2 - 1}}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + k_i^2 \frac{4\pi^2}{\text{df} \sqrt{8Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + ] + [ k_i^2 \frac{2\pi Q_i^2}{\text{df} \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) + k_i^2 \frac{6\pi Q_i^2}{\sqrt{1/3 \cdot \text{df} \sqrt{12Q_i^2 - 1}}} \tanh \left( \frac{\pi}{2\sqrt{12Q_i^2 - 1}} \right) ]</td>
</tr>
<tr>
<td>6/7</td>
<td>[ k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2 \cdot \text{df} \sqrt{8Q_i^2 - 1}}} \tanh \left( \frac{\pi}{2\sqrt{8Q_i^2 - 1}} \right) + k_i^2 \frac{6\pi Q_i^2}{\sqrt{1/3 \cdot \text{df} \sqrt{12Q_i^2 - 1}}} \tanh \left( \frac{\pi}{2\sqrt{12Q_i^2 - 1}} \right) + ] + [ k_i^2 \frac{4\pi Q_i^2}{\sqrt{1/2 \cdot \text{df} \sqrt{8Q_i^2 - 1}}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) + k_i^2 \frac{2\pi Q_i^2}{\text{df} \sqrt{4Q_i^2 - 1}} \tanh \left( \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) ]</td>
</tr>
</tbody>
</table>

Figures 3.2a–h show the worst-case plot of the normalized equivalent resistance as a function of \( Q_{low} \) and \( \text{df} \) covering the entire conversion ratios. Figures 3.2a and b demonstrate EXB codes (x/8 fractions), Figures 3.2c–g demonstrate SFN codes, and Figure 3.2h demonstrates SGF codes (x/7 fractions). The curves were extracted numerically using MATLAB. Duality can be observed between ratios 2/8 to 6/8, 2/5 to 3/5, 1/3 to 2/3, and between each of the x/7 fractions. Duality can be also observed between the ratios 1/2 and 4/8, although these are extracted from different types of codes. Similarity can be observed between ratios 3/8 to 4/8 and 3/5 to 4/5.
Fig. 3.2. Worst-case plot of the normalized equivalent resistance as a function of $Q_{j,\text{low}}$, for conversion the ratios: (a) $M=2/8, 6/8$ (b) $M=3/8, 4/8$ (c) $M=2/5, 3/5$ (d) $M=1/3, 2/3$ (e) $M=1/5$ (f) $M=4/5$ (g) $M=1/2$ (h) $M=1/7$- 6/7 for $df_j$ in the range of 0.15-0.35.
Fig. 3.2. (Continued).
3.4 Experimental results of the resonant binary/Fibonacci SCC

To validate the proposed design methodology, two experiments were tested at the medium power range. The first experiment, demonstrated the binary SCC using the stray inductance and with pre-calibration of the switching timing. The second experiment demonstrated the converter with the active ZCD system. The design of the active zero detection system and component selection of the power stage were done according to the guidelines and practical implementation described in Chapters 2 and 3, respectively.

3.4.1 Resonant binary SCC with pre-calibration of the switching timing

The 100 W resonant binary SCC Prototype was realized using the stray inductance in the circuit alone without adding an additional inductor. The switching frequency was adjusted correspondingly to the equivalent RCL circuit in every stage [3].

The test parameters of the prototype were $V_{in}=100$ V and $f_S\approx 53$ kHz. The resonant capacitors are two 4.7 µF, 100 V MLCC capacitors C5750X7R2A475K (TDK) connected in parallel. Output capacitors were ten 4.7 µF, 100 V capacitors connected in parallel with nominal $R_o=39$ Ω. The bidirectional switching devices are two 100 V power MOSFETs with ‘on’ resistance around 45 mΩ each. Microcontroller DsPic33J12GP202 was used for timing the frequency and the duty cycles, respectively.

The calculated stray inductance were approximately $L_1=680$ nH, $L_2=358$ nH, $L_3=866$ nH, $L_4=484$ nH. Taking into account the capacitance change due to the change of the average voltages and that the total parasitic loop resistance in every state is about 360 mΩ, the quality factors were calculated to be $Q_1=1.08$, $Q_2=1.12$, $Q_3=1.68$, and $Q_4=1.05$. Furthermore, the frequency ratio $df_1=0.58$, $df_2=0.32$, $df_3=0.48$ and $df_4=0.42$.

Figures 3.3 through 3.5 show the experimental waveforms of the resonant binary SCC prototype with the components mentioned above. Figures 3.3 and 3.4 show the current at the output stage for $V_{in}=80$ V and $V_{in}=100$ V at $M=5/8$, respectively, and Figure 3.5 shows for $V_{in}=60$ V at $M=3/8$.

Figure 3.6 shows the efficiency of various input voltages and loads. It is clear from the generic equivalent circuit model described in Fig. 1.6 that for higher target voltages, the rms current values will be smaller for a constant $P_o$ and the power loss on $R_{eqT}$ will decrease. The calculated values of $R_{eqT}$ according to equation (3.1) for the 5/8 case were 1.2 Ω while the experimentally evaluated values were about 1.3 Ω.
Fig. 3.3. $I_{\text{out}}$ and $V_{DS}(S6)$ at $V_{in}=100V$, $P_{out}=136W$, $M=5/8$.

Fig. 3.4. $I_{\text{out}}$ and $V_{DS}(S6)$ at $V_{in}=80V$, $P_{out}=100W$, $M=5/8$.

Fig. 3.5. $I_{\text{out}}$ and $V_{DS}(S6)$ at $V_{in}=60V$, $P_{out}=69.89W$, $M=3/8$.

Fig. 3.6. Efficiency of step-down, resonant binary SCC, $M=5/8$. 
3.4.2 Resonant binary SCC with active zero current detection

To demonstrate the performance of the resonant binary SCC and the operation of the active ZCS, a 100 W prototype has been built and tested experimentally. A summary of the system components can be found in Table 3.5. The generation of the EXB codes has been realized on a dsPIC33F series microcontroller. Due to the large number of I/O ports required for the power switches, an auxiliary decoder is used. The microcontroller selected includes an analog comparator module and a multiplexer to allow selection of the input feed. The comparator module features high-speed operation with a typical delay of 20 ns and a typical offset voltage of ±5 mV. However, a typical delay of the zero detection system, from comparator detection until the time that an interrupt is triggered was measured at 500 ns. The total processing time (from comparator to switches commutation) was found to be approximately 1 µs. Following the design guidelines above, the worst-case resonant frequency (highest value) per state is set to 180 kHz to allow sufficient processing time. The reference voltage to the comparator is set to 1.65 V to compensate for the processing time delay and improve the SNR of the detection. Performance of the system and the ZCS method developed is demonstrated on operation with the conversion ratios of 1/8, 3/8, 5/8, and 7/8 to cover the entire operation range. For each of the conversion ratios, the capability of the method to lock the switching frequency to the resonant frequency is verified for a wide range of line (30-80 V) and load variations (20-130 W). For the conversion ratios of 3/8 and 5/8, the current has been sensed from \( C_3 \) that is active at all sub-circuits and the peak currents from one state to another are of the same order. For the case of 1/8, the current levels significantly vary between sub-circuits; therefore, the feed to the comparator has been switched between \( C_3 \) and \( C_2 \). A larger \( R_{\text{sense}} \) is chosen for \( C_2 \) to successfully detect the zero crossing point at lower currents. For 7/8, to cover the full power range of 130 W, the current is sensed from the top of the resistive ladder (390 Ω) of \( C_3 \) for lower power range (up to 70 W), and is then switched manually to the voltage division point (220 Ω) to measure higher power levels up to 130 W. The measurement circuitry (sensors, dividers, etc.) is detailed in Fig. 2.1. The gate drive losses were measured in the range of 1 to 2 W for all conversion ratios. A photograph of the vector-board-based experimental prototype is given in Fig. 3.7.

Figure 3.8 shows exemplary snapshots of the system operating at steady-state with active ZCS for four conversion ratios tested. As described in the practical implementation section and can be observed from Fig. 3.8, large differences exist between the sub-circuits in the peak currents, quality factors, and the signals’ slopes at the vicinity of zero current. Minor glitches in the current shapes are the result of small deviations between the estimated reference voltage and the experimental signal.

To verify the operation of the active ZCS method, two sets of experiments have been carried out. In the first experiment, the load resistance is kept constant while the input voltage varied from 30 V to 80 V. Active ZCS is obtained for the entire operation range and all conversion ratios. Figure 3.10 shows the efficiency curves of the converter as a function of the output power for each of the conversion
ratios. It can be observed that, as expected from the theory of SCC, the efficiency is virtually constant for a given load resistance.

The strength of the active ZCS is highlighted in Table 3.6, which summarizes the average values of equivalent resistance and efficiency, and the deviation (in percentage) of the duration of each sub-circuit. As described earlier and observed in Fig. 3.8, the conduction time of the sub-circuit varies from one to another; this is primarily due changes in the overall capacitance. Moreover, Table 3.6 indicates that the duration of a specific sub-circuit may also vary considerably due to changes in components’ values for different operating conditions, strongly promoting the necessity of an active method for zero detection. The largest variations in components’ values are expected in wider conversion ratios, such as 1/8. There, larger rms currents are needed per unit of transferred power, which affects the capacitance and inductance within a sub-circuit. The larger rms currents are also the reason for the somewhat lower efficiency, in spite of the lower equivalent resistance obtained for this ratio.

The variable resonant period and the variations in the sensed signal slope are experimentally demonstrated in Figs. 3.9a–c for the case of $M=1/8$. It can be observed in Fig. 3.9a that while the resonant period significantly varies between $k=1/2$ and $k=1/8$ (due to the different number of serially connected capacitors in each state), the slope in the vicinity of zero is virtually fixed. The minor glitches in the current shapes are due to the minor differences of the slopes, as explained in Section 2.3.2. Figures 3.9b and c, depict the variations due to different power levels. The extended period at higher power levels are due to component variations that reduce the effective quality factor of the sub-circuits. Fortunately, since the initial $Q$ is designed to be of a moderate value (based on Section 3.2), the reduction in $Q$ extends the resonant period sufficiently such that the variation of the slopes of the resonant currents near zero are negligibly small.

In the second experiment, the input voltage is kept constant at 80 V while varying the load. Active ZCS is obtained for the entire operation range and all conversion ratios. Figure 3.11 shows the efficiency curves of the converter as a function of the output power for each of the conversion ratios. Similarly to the previous experiment, the efficiency is nearly constant for a wide operation range. It should be noted, however, that in the case of 1/8, a narrower power range is examined due to practical constraints on the stress of the components. The power range for each conversion ratio that is covered in this experiment has been intentionally limited due to practical restrictions. That is, the experiment is conducted such that the maximum current stress on the flying capacitors does not exceed 4 Arms.

The startup sequence that was described earlier is also demonstrated on the experimental setup. Figure 3.12 demonstrates the three operation modes used to limit the inrush currents and stabilize the capacitors’ voltages, that is, operation with EXB code at: (a) high frequency; (b) estimated times; (c) activating the active ZCS mode and locking the switching frequency to the resonant frequency.

The loss estimation method was found to be in very good agreement with the experimental measurements. Given an estimated $R_{loop}$ value 170 mΩ (based on measured conduction path), the
calculated $R_{eqT}$, according to equation (3.1) were 0.94 Ω (df ≈ 0.23, $R_{eqT}/R_{loop} \approx 5.5$) and 0.46 Ω (df ≈ 0.35, $R_{eqT}/R_{loop} \approx 2.7$) for 3/8 and 1/8, while the measured $R_{eqT}$ were 1 Ω and 0.37 Ω, respectively. It should be noted that the discrepancies are due to the asymmetrical layout of the sub-circuits.

Table 3.5 - Converter Parameters

<table>
<thead>
<tr>
<th>Component</th>
<th>Power Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Part No.</td>
</tr>
<tr>
<td>Input capacitor</td>
<td>C5750X7R2A475K</td>
</tr>
<tr>
<td>Output capacitor</td>
<td>C5750X7R2A475K</td>
</tr>
<tr>
<td>Flying capacitor</td>
<td>C5750X7R2A475K</td>
</tr>
<tr>
<td>MOSFETs (R_{on})</td>
<td>IPA030N10N3</td>
</tr>
<tr>
<td>Air Inductor</td>
<td>Air core</td>
</tr>
<tr>
<td>Microcontroller</td>
<td>dsPIC33FJ16GS502</td>
</tr>
<tr>
<td>Current Transformer</td>
<td>FXC-7TN169/36.3 (Ferrite toroid)</td>
</tr>
<tr>
<td>Digital Section</td>
<td>Microcontroller</td>
</tr>
<tr>
<td></td>
<td>Decoder</td>
</tr>
</tbody>
</table>

Table 3.6 - Measurements with Active ZCS for Constant

<table>
<thead>
<tr>
<th>M</th>
<th>$R_{in}$ [Ω]</th>
<th>$R_{out}$ [Ω]</th>
<th>$\Delta V_{in}$ [V]</th>
<th>$\Delta I_{in}$ [A]</th>
<th>$\eta_{eqT}$ [%]</th>
<th>$\eta_{eqT}$ [%]</th>
<th>$\eta_{eqT}$ [%]</th>
<th>$\eta_{eqT}$ [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/8</td>
<td>2.5</td>
<td>0.37</td>
<td>0.847</td>
<td>36.8</td>
<td>2.37</td>
<td>28.6</td>
<td>25</td>
<td>23.2</td>
</tr>
<tr>
<td>3/8</td>
<td>16</td>
<td>1.05</td>
<td>0.925</td>
<td>38.6</td>
<td>1.27</td>
<td>25</td>
<td>2.5</td>
<td>2.4</td>
</tr>
<tr>
<td>5/8</td>
<td>29.3</td>
<td>1.01</td>
<td>0.958</td>
<td>36.5</td>
<td>0.74</td>
<td>1.4</td>
<td>30</td>
<td>10</td>
</tr>
<tr>
<td>7/8</td>
<td>36.5</td>
<td>0.42</td>
<td>0.979</td>
<td>24.1</td>
<td>0.57</td>
<td>7.7</td>
<td>25</td>
<td>3.2</td>
</tr>
</tbody>
</table>

$\Delta x$ – Indicates the amount of variation in a measured variable $x$ value throughout the experiment.

---

Fig. 3.7. Prototype of the resonant binary SCC.
Fig. 3.8. Experimental result of the binary converter operating in active ZCS mode for various conversion ratios. (a) $M=1/8$, $V_{in}=80$ V, $P_{out}=31.3$ W, $\eta=0.85$; Traces top to bottom: inductor current $I_{Ls}$ (0.8 A/div), rectified sensed voltage resulting from $Ic_3$, $V_{Ic3}$ (10 V/div), rectified sense voltage resulting from $Ic_2$, $V_{Ic2}$ (10 V/div), comparator output, $V_{cmp}$ (5 V/div). Horizontal scale (5 $\mu$s/div). (b) $M=3/8$, $V_{in}=100$ V, $P_{out}=76.5$ W, $\eta=0.92$; Traces top to bottom: $I_{Ls}$ (0.8 A/div); $V_{Ic3}$ (10 V/div); $V_{cmp}$ (5 V/div); interrupt status $V_{int}$ (5 V/div). Horizontal scale (10 $\mu$s/div). (c) $M=5/8$, $V_{in}=80$ V, $P_{out}=73$ W, $\eta=0.95$. Traces and horizontal scale: as in (b). (d) $M=7/8$, $V_{in}=80$ V, $P_{out}=131.7$ W, $\eta=0.99$. Traces top to bottom: $I_{Ls}$ (0.4 A/div), $V_{Ic3}$ (5 V/div); $V_{cmp}$ (5 V/div); $V_{int}$ (5 V/div). Horizontal scale (5 $\mu$s/div).

Fig. 3.9. (a) Slope difference between the highest and the lowest current pulses at fixed output power - 31.3 W, $I_o=3.6$ A. (b) and (c) Slope differences between pulses at wide output power range, $P_o=5$ W, $I_o=1.7$ A and $P_o=31.3$ W, $I_o=3.6$ A, respectively.
Fig. 3.10. Measured efficiency, $M=1/8-7/8$, constant $R_o$, $V_{in}=30-80$ V.

Fig. 3.11. Measured efficiency, $M=1/8-7/8$, constant $V_{in}=80$ V.

Fig. 3.12. Experimental results of the inductor current for the soft-start method for $M=3/8$: (a) High switching frequency; (b) estimated resonant values; (c) active ZCS method.
3.5 Discussion and conclusions

An active ZCS method that allows resonant operation of binary and Fibonacci step-up/down SCC was developed and tested experimentally. For high-frequency resonant operation, the stray inductances of the circuit can be used. To lower the frequency of operation, a single air-core inductor in series to the output stage was added. Consequently, the workload requirements from the digital processor are eased, and a realization with a simple, low-cost controller is feasible.

The active zero current cross detection was found to accurately adjust the switching times for four different RCL sub-circuits dictated by the EXB/SFN/SGF codes. The current sensing mechanism was implemented using three current transformers strategically mounted after the capacitors to avoid measurement of the output current that includes a dc component.

The experimental validation confirmed that conjecture and highlighted the advantages of an active method. It revealed that the changes in the resonant period within a sub-circuit are significant and may vary up to 30% for the operation range tested. It has also been established that although the resonant periods vary considerably, the slope of the sensed current in the vicinity of the zero crossing point is less prone to variations. Therefore, for the case of the binary SCC, the method can be further simplified by fixed reference voltage settings. This eliminates the need for an additional fast compensation loop to vary the reference voltage.

The experimental results also support the need for a dynamic wide-range reference voltage in order to compensate for processing delays and different current levels of each sub-circuit. Since a reasonable SNR is required, the reference to the comparator was kept constant (well above zero) and the reference was changed by the effective sensing gain. This was done by resistor dividers of the sensed signal and may be useful for implementation in other resonant switch capacitor topologies.

Study on the efficiency was carried out. It was found that although the calculated equivalent resistance is the lowest at the ratio of 1/8, that ratio provides the poorest efficiency. Moreover, the efficiency increases for smaller conversion ratios (larger fractions). This behavior is intuitively explained by the fact that higher ratios (such as 1/8, 3/8) have higher rms current for a given transferred power and hence the power losses will be higher. This can be illustrated by rewriting the well-known RSCC efficiency expression as a function of the output current, i.e., \( \eta = \frac{V_o}{V_{in}} = \frac{(V_o/I_o)}{(V_o/I_o+R_{eqT})}. \) This implies that for a given power level, the load resistance of larger ratios (smaller fractions), such as 1/8, is significantly smaller; the efficiency is expected to drop per unit of transferred power. Another observation on the efficiency and the expected equivalent resistance is made by the current waveforms and from the solution for the average currents for each sub-circuit. It shows that for some conversion ratios, there might be a sub-circuit in which the current is negative. This phenomenon can be explained from a charge-balance perspective and is given in Section 2.2. However, from an efficiency and \( R_{eqT} \) point of view, that means that for this particular sub-circuit,
current flows from the output into the system, which may affect the estimations of $R_{eqT}$ and the expected efficiency. A detailed analysis of this topic is beyond the scope of this study.

The method presented in this study has been verified to successfully operate resonant binary SCC and to accommodate a wide and dynamic operation range, and therefore can be applied to other multi-phase SCC topologies that involve a number of sub-circuits and a wide operation range.
Chapter 4 - Modeling and Analysis of Resonant Switched-Capacitor Converters with Free-Wheeling ZCS

4.1 Introduction

In resonant switched capacitor converters (RSCC), zero current switching (ZCS) is mandatory to achieve high power conversion efficiency and reliability. A ZCS can be achieved by employing an active monitoring and control of the resonant current [2], [39]. This requires a complex control scheme and circuitry. Alternatively, ZCS can be obtained by unidirectional switches, e.g., inserting a diode in series to the active switch. In this case, ZCS is assured by simple means at the cost of increased conduction losses. To overcome the deficiencies of these methods, a simple and efficient self-commutation concept as illustrated in Fig. 4.1 has been presented in [41], [51], and [52]. It consists of a transistor that conducts for the majority of the resonant cycle, and a parallel diode that acts as a free-wheeling element such that turn off occurs at zero current. This method exhibits both advantages of inherent ZCS and overcomes the deficiencies of previous methods, such as high conduction losses and complex control hardware. However, due to a divided conduction path (DCP) of the resonant current (Fig. 4.1), the conventional equivalent resistance method for loss evaluation [26], [27], [53], [54], cannot be applied directly in this case.

The objective of this part of study is to describe and explore the loss mechanism of resonant SCC operating in a self-commutation ZCS mode. The new modeling methodology extends the modeling concept employed in [26], [27], and [53]-[63] to take into account the DCP of a single charge/discharge state.

The deliverables of this modeling approach are on both theoretical and practical realms; it provides a streamlined procedure to design a reliable and low-cost soft-switched SCC, as well as an insight into the dominant contributors of losses in DCP operation mode.

The rest of this part of the work is organized as follows: Section 4.2 details the terminology and basic definitions to the approach of this study; the modeling methodology is delineated in Section 4.3; Section 4.4 derives the loss contributors; Section 4.5 provides a rigorous validation of the modeling concept; and finally, the chapter is concluded in Section 4.6.

4.2 Basic terminology and definitions

Throughout the study, the modeling concept will be explained on a unity gain resonant SCC (Fig. 4.2). Even though the exemplary circuit is not the best candidate to showcase the strength of ZCS, it highlights the mechanism of the DCP operation and was therefore selected.
Resonant SCC that operates in an open-loop can be represented by an equivalent circuit, [62]-[73], which consists of a target voltage source, \( V_T \), that represents the no-load output voltage of the converter and a series equivalent resistance, \( R_e \), that stands for the conduction losses caused by the current flow in the series resistances of the capacitor’s charge/discharge path.

Self-commutated unity gain SCC (see Fig. 4.2) operates in two phases. The charging phase is split into two sub-states, as marked in the timing diagram (see Fig. 4.1). First, the switch \( S_1 \) is turned on, and the capacitor \( C_f \) is charged resonantly. Next, approaching the end of the half resonant cycle, \( S_1 \) is turned off, and the free-wheeling diode conducts until the current reaches zero. The second phase starts by turning \( S_2 \) on, and \( C_f \) resonantly discharges onto the output.

![Fig. 4.1. Typical resonant current waveforms during a: Charge phase – DCP operation, Discharge phase – SCP operation.](image1)

![Fig. 4.2. Unity gain SCC with free-wheeling ZCS of the charge state.](image2)

To facilitate systematic analysis, the following definitions and terminology are used: phase—relates to a time period of a half resonant cycle, e.g., charging phase, or discharging phase (see Fig. 4.1), denoted by a numerical index \( i = 1, 2 \ldots \); sub-state—a portion of a phase, denoted by an alphabetical index \( j = a, b \ldots \); single conduction path (SCP)—a phase that includes one sub-state only; divided conduction path (DCP)—a phase that includes more than one sub-state. For example, sub-state ‘a’ at phase 1 (red lines marked with a dashed-dot in Figs. 4.1 and 4.2), will be denoted as \( ij = 1a \).
4.3 Modeling approach

The generic approach to extract the equivalent model of resonant SCC operating in the particular case of SCP has been presented in [26], [27], [53] and [54]. Generalization of the model to include DCP operation requires the following steps: first, based on the switching sequence applied to the SCC, each phase is described by one or more sub-states according to the operation mode (SCP or DCP). Given the example on hand, the operation of SCC in Fig. 4.2 is represented by three sub-circuits, that is, a charging sub-state by the transistor conduction (see Fig. 4.3a), a charging sub-state by the free-wheeling diode (see Fig. 4.3b), and a discharge phase (see Fig. 4.3c).

Second, each of the sub-circuits is simplified to a lumped RLC circuit as shown in Fig. 4.4. This circuit is used to describe the operation of each sub-circuit in its relevant conduction time, where \( \Delta V_i \) is the initial voltage difference between the charging/discharging source and the resonant tank voltage, \( R_{ij} \) is the total loop resistance (switch resistance \( R_{Si} \), inductor resistance \( R_{Li} \), and capacitor ESR), \( C_i \) and \( L_i \) are the total capacitance and inductance of the loop, respectively.

The next step applies the calculation of the power loss, \( P_{ij} \), due to the series resistances \( R_{ij} \) of each sub-state, and expressing it as a function of the average capacitor current \( I_{avg} \). The average capacitor current of each phase is linearly proportional to the average output current [27], [68], [69]. By doing so, the power dissipated in each phase is referenced to the output current, using the proportionality factor \( k_i \). The equivalent resistances of each sub-state, \( R_{eij} \), are then extracted from the dissipated power, \( P_{ij} \). It should be noted that by addressing the model calculation from the average current domain, the calculation of \( \Delta V_i \) which primarily depends on the capacitors value and the operating frequency, is eliminated [26], [27], [53].

The general case of DCP applies a free-wheeling mode realized by diode conduction. Since the dominant loss contributor of the diode is the average current, an additional proportionality factor is
required to relate the average sub-state current to the total average current of the phase in which it exists (see Fig. 4.5). In this study, this factor is referred as \( \rho_{ij} \), and the relationship between the average currents can now be expressed as:

\[
I_{av1} = \rho_{1a} \cdot I_{av1}; \quad I_{av1b} = \rho_{1b} \cdot I_{av1},
\]

where \( I_{av1} \) is the phase current, which equals to the sum of the average capacitor currents during each sub-state \( I_{av1a} \) plus \( I_{av1b} \). The relationship between the average currents to the output current is obtained by substituting \( I_{av1} = k_1 I_{out} \) in equation (4.1), that is:

\[
I_{av1a} = \rho_{1a} k_1 \cdot I_{out}; \quad I_{av1b} = \rho_{1b} k_1 \cdot I_{out},
\]

where \( k_1 \) is the proportionality factor of the charge phase.

It should be noted that the averaging method applied here considers the contribution of the sub-state average current on the entire switching period, that is:

\[
I_{av1} = q_i / T_s; \quad I_{av1a} = q_{ia} / T_s,
\]

where \( q_i \) is the total charge of the \( i^{th} \) phase, and \( q_{ia} \) is the charge of the sub-state ‘a’ while commutated at the angle \( \phi_i = \pi T_{ia} / T_i \) (see Fig. 4.5). Therefore, the diode loss contribution can be represented as a function of the phase current, i.e., by a voltage source, \( V_{dij} \), that takes into account the partial average current in the sub-state as follows:

\[
V_{dij} = k_i \cdot \rho_{ij} \cdot V_{Fi},
\]

where \( V_{Fi} \) is the average voltage drop across the diode due to current through it at sub-state, \( j \), in phase, \( i \).

Finally, the model is constructed by considering a series connection of the equivalent resistances, \( R_{ei} \) and the voltage source, \( V_{dij} \), between the target voltage and the output port. As a result, the SCC in Fig. 4.2 that operates in DCP mode is represented by the average equivalent model circuit depicted in Fig. 4.6.
Fig. 4.6. SCC generic average equivalent circuit that shows the contribution of the partial sub-circuits equivalent resistances $R_e$ to the total equivalent circuit resistance $R_c$. For the unity gain SCC example of Fig. 4.2, $R_{el_a}$ is the loss contribution of charge sub-state 1a, $R_{el_b}$ and $V_{dib}$ are the resistive and diode loss contribution of the free-wheeling sub-state, respectively, $R_{el_2}$ is the loss contribution of discharging phase.

### 4.4 Extraction of equivalent resistances and equivalent average voltage drop

Following the modeling methodology described earlier, the equivalent resistance value is extracted in this section. It is assumed that each RLC sub-state (Fig. 4.4) operates under ZCS conditions, and the quality factor, $Q_{ij}$, is sufficiently high ($Q_{ij} > 5$).

The peak currents, $I_{pki}$ of the sub-states are considered equal to the charge phase peak current $I_{pki}$. For the case of the circuit in Fig. 4.2, this applies the following:

$$I_{pki} = I_{pka} = I_{pkb},$$  \hspace{1cm} (4.5)

where $I_{pki}$, $I_{pka}$, and $I_{pkb}$, are the potential peak currents that are or could be developed given the conditions of the switching phase $i$, or the sub-state $j$, $ia$ and $ib$, respectively.

#### 4.4.1 Equivalent resistance calculation

The energy, $E_{ia}$, dissipated in the sub-circuit due to the loop resistance, $R_{ia}$ (Fig. 4.4) and the current during the time interval $T_{ia}$ (Fig. 4.5) is derived by integrating the instantaneous power $p(t) = i_C^2(t) \cdot R_{ia}$ ($i_C(t)$ is the capacitor current) over the sub-state time interval, $T_{ia}$:

$$E_{ia} = R_{ia} \cdot \left(I_{pki}\right)^2 \cdot \int_0^{\phi_{0ia}} \left[\sin(\omega_{0ia} t)\right]^2 dt = R_{ia} \cdot \left(I_{pki}\right)^2 \cdot \frac{\left(\phi_i - \cos(\phi_i)\sin(\phi_i)\right)}{2\omega_{0ia}},$$  \hspace{1cm} (4.6)

where $\omega_{0ia} = 2\pi f_{0ia}$ is the natural resonance frequency of the phase $i$, sub-state ‘a’. The relationship between the peak current and the average current of phase, $i$, can be expressed as:

$$\left(\frac{2}{\pi}\right) \cdot I_{pki} = I_{avo} \cdot (2 \cdot df_i),$$  \hspace{1cm} (4.7)

where $df_i = f_i / f_0$ is the ratio between the switching frequency and the natural frequency of the resonant network [27].

Substituting expressions (4.2) and (4.7) into expression (4.6), and after some manipulations, the power loss of the sub-state can be expressed as a function of the average output current, $I_o$ by:
\[ P_{ea} = (I_o)^2 \cdot k_i^2 \cdot \frac{\pi \cdot R_{ma}}{4 \cdot df_i} \cdot (\varphi_i - \cos(\varphi_i) \sin(\varphi_i)) \].  

(4.8)

To comply with the equivalent model (Fig. 4.6), the equivalent resistance of the sub-state, \( i_a \), is extracted from equation (4.8) to be:

\[ R_{ea} = k_i^2 \cdot \frac{\pi \cdot R_{ma} \cdot \varphi_i}{4 \cdot df_i} \cdot (1 - \sin(c \cdot 2\varphi_i)) \].

(4.9)

Figure 4.7 shows various curves of equation (4.9) for different ratios of loop resistances between sub-states 1a and 1b, demonstrating the change of \( R_e \) as a function of charge phase commutation angle \( \varphi_1 \). The losses per a DCP phase (either charging or discharging) are inversely proportional to the commutation angle, i.e., decreases with the reduction of the free-wheeling sub-state. From an efficiency point of view, this provides an insight to the practical commutation angles that may be used to assure ZCS without a significant increase in the conduction losses. As can be conjectured from Fig. 4.7, a good practical commutation angle would be in the range of 0.85\( \pi \), which is satisfactory for a wide range of loop resistances. The results of Fig. 4.7 may also assist in the selection of the transistors, given the target efficiency of the practical converter.

In a similar manner, all the equivalent sub-state resistances can be extracted using the steps described above. Alternatively, for the case of a complementary free-wheeling action, the equivalent resistance can be derived by substituting the commutation angle \( \varphi_i \), by the complementary one (\( \pi - \varphi_i \)). Naturally, for the particular case of SCP (discharging phase, \( i = 2 \)), calculations are carried out with \( \varphi_i = \pi \), that is:

\[ R_i = k_i^2 \cdot \frac{\pi^2}{4 \cdot df_i} \cdot R_{ma} \].

(4.10)

As can be observed, expression (4.10), derived using the generalized approach of this study, is in agreement with the SCP modeling methodology previously reported in [26], [27], [53], and [54].

![Fig. 4.7. Variation of \( R_e \) as a function of \( \varphi_1 \) for different ratios of loop resistances between \( R_{1a} \) and \( R_{1b} \). In the example above \( R_{1a} = R_2 = 10 \) m\( \Omega \).](image)
4.4.2 Equivalent average diode voltage source calculation

Following Fig. 4.5, the proportionality factor, $\rho_{ia}$, that represents the ratio between the charge transferred via sub-state $i_a$, and the total charge via phase $i$, can be derived as follows:

$$
\rho_{ia} = \frac{q_{ia}}{q_i} = \frac{\int_{0}^{\phi_i/\pi_0} I_p k_i \sin(\omega_0 t) dt}{\int_{0}^{\pi/\pi_0} I_p k_i \sin(\omega_0 t) dt} = \sin^2\left(\frac{\phi_i}{2}\right).
$$

(4.11)

The complementary proportionality factor in the case of two sub-states in one phase is $\rho_{ib} = 1 - \rho_{ia}$. As can be seen from Fig. 4.8, symmetry exists in the charge distribution through paths $i_a$ and $i_b$ below and above the point of $\phi_i = \pi/2$.

![Fig. 4.8. Distribution of the charge through paths $i_a$ and $i_b$ as a function of the commutation angle $\phi_i$.](image)

In the general case of multiple phases with free-wheeling diodes, the effective average equivalent voltage drop, $V_d$, can be obtained by summation of equation (4.4) for all the contributing sub-states, and expressed as:

$$
V_d = \sum_{i,j,a} k_{ij} \cdot \rho_{ij} \cdot V_{ij},
$$

(4.12)

where $m$ is the total number of switching phases, and $n$ is the total number of sub-states per phase $i$.

Another potential contributor to losses in resonant SCC is the time-delay between consecutive phases, i.e., the time duration between the current zero crossing of the free-wheeling diode and the initiation of the next phase. Ideally, the next commutation phase is to start immediately when the current is zero, otherwise, a zero current period exists, that influences the total efficiency of the system [2]. The model presented in this study is well-suited for quantifying this effect by employing the ratio factor $df$, which represents the ratio between the switching frequency and the natural frequency of the resonant network [27]. This implies that the losses due to the time delay are inversely proportional with $df$. An application example of this factor in the model is presented in Fig. 4.9, which illustrates the curves of the expected output voltage as a function of the commutation angle $\varphi_i$ for several time
delay settings. As expected, the output voltage is lower with the increase of the zero current period added between the phases.

\[ df = 0.1 \]
\[ df = 0.3 \]
\[ df = 0.5 \]
\[ df = 0.7 \]
\[ df = 0.9 \]

Fig. 4.9. Output voltage of a unity gain SCC as a function of the commutation angle, \( \varphi \). Model calculation–solid trace, simulation–asterisk marks. \( V_{in} = 10 \) V, \( V_f = 1.7 \) V, \( R_{DS(on)} = 100 \) m\( \Omega \), \( R_o = 5 \) \( \Omega \), \( Q = 30 \), \( f_0 = 5 \) kHz.

### 4.4.3 Equivalent resistance calculation at low \( Q \)

The energy interpretation of the quality factor, \( Q \), of a resonant circuit can be expressed as [11]:

\[
Q = \frac{\text{energy stored}}{\text{average power dissipated in the resistor}}.
\]

So, theoretically we would prefer to design the converter tank component for working with sufficient high quality factor values. From the SCC average model point of view, low quality factor, \( Q < 1 \), can lead to significant extremely high values of the series equivalent resistance, \( R_e \), as well as low efficiency. On the other hand, the equivalent resistance asymptotically reaches a constant value at \( Q \) higher than 3, as detailed in [1], [2], and [27], and in Chapter 3. Hence, a losses model for the DCP mode that covers lower quality factor values is essential. This subsection introduces the expanding expressions to (4.9) and (4.11), and presents a closed form to DCP mode. The extended expressions produce the charge distributions and equivalent resistance formulas for the entire range of the quality factor (i.e., \( Q > 1/2 \)).

Equation (4.13) also holds for the series \( RCL \) circuit at resonant and the resonant frequency can be calculated taking into account the damp factor, \( a = R_i / 2L_i \), of certain sub-state \( i \). Figure 4.10 illustrates the shape of a resonant current for several values of the quality factor ranging from low to high. As can be seen from Fig. 4.10, at high values of \( Q \), the zero crossing point of the current occurs at \( 2\pi/\omega_0 \). At very low quality factors (\( Q \to 0.5 \)), zero crossing occurs at significantly larger time intervals.
Fig. 4.10. Illustration waveform of a resonant current for several values of the quality factors (0.55÷7), where $L=50\ \mu\text{H}$, $C=100\ \mu\text{F}$ and $0.1\ \Omega<R<1.4\ \Omega$.

Figure 4.11 illustrates the current waveform in DCP mode at low values of $Q$. Following Fig. 4.11, the proportionality factor, $\rho_{ia}$, that represents the ratio between the charge transferred via sub-state $ia$, and the total charge via phase $i$, can be derived by taking into account the current envelope, $e^{-at}$:

$$
\rho_{ia_{-\text{ext.}}} = \frac{q_{ia}}{q_i} = \frac{I_{pki} \int_0^\phi \sin(\omega_d t) e^{-at} dt}{I_{pk} \int_0^{\phi/\omega_d} \sin(\omega_d t) e^{-at} dt} = \frac{\omega_d - e^{-\omega_d \phi/\omega_d} (\omega_d \cos \phi + a \sin \phi)}{\omega_d (1 + e^{-a \pi/\omega_d})}, \quad (4.14)
$$

The complementary proportionality factor in the case of two sub-states in one phase can be derived as follows:

$$
\rho_{ib_{-\text{ext.}}} = \frac{q_{ib}}{q_i} = \frac{I_{pki} \int_0^{\pi/\omega_d} \sin(\omega_d t) e^{-at} dt}{I_{pk} \int_0^{\pi/\omega_d} \sin(\omega_d t) e^{-at} dt} = \frac{\omega_d e^{-\omega_d \pi/\omega_d} + e^{-\omega_d \phi/\omega_d} (\omega_d \cos \phi + a \sin \phi)}{\omega_d (1 + e^{-a \pi/\omega_d})}, \quad (4.15)
$$

Figure 4.12 illustrates the distribution of the charge through paths $ia$ and $ib$ as a function of the commutation angle $\phi_i$. As can be seen from Fig. 4.12, symmetry exists in the charge distributions through paths $ia$ and $ib$ at point of $\phi_i=\pi/2$, at high quality factors. At low quality factors, crossing points between $\rho_{ia}$ to $\rho_{ib}$ occurs at smaller angles of $\phi_i$. This means that at low values of the quality factor, most of the charge transfers at low phase angles, (smaller than $\pi/2$). This also can be explained from Fig. 4.11, where most of the pulse area is at the left side. It should be noted that in Figs. 4.8 and 4.12 the values of the expression of $\rho_{ij}$ converge at high quality factors ($Q \geq 5$).
Fig. 4.11. Illustration of DCP switching phase current waveform at low $Q$. 

The expressions of the equivalent resistances can be derived in the same method as detailed in subsection 4.4.2. In the case of low values of $Q$, it is assumed that the loop resistances and the resonant tanks of each sub-state are equal ($Q_{1a}=Q_{1b}$). As a result, the potential peak currents $I_{pkia}$, $I_{pkib}$, are considered equal.

Another approach to produce the equivalent resistances at low values of $Q$, can be describe as follows: The sinusoidal current formula of a series $RCL$ circuit for underdamped case is, [26], [27]:

$$i(t) = \frac{\Delta V}{\omega_i L} e^{-\alpha t} \sin (\omega_d t).$$  \hspace{1cm} (4.16)

The charge $q_{ia}$ transferred during time interval $T_{ia}$ to/from a capacitor $C_i$ is calculated to be:
\[ q_{ia} = \int_{0}^{\phi/\omega_d} i \cdot dt = \frac{\Delta V}{\omega_d L} \int_{0}^{\phi/\omega_d} e^{-at} \sin(\omega_d t) dt = \frac{\Delta V}{\omega_d \omega_a^2 L} \left[ \omega_d - e^{-a\omega_a t} \left( \omega_d \cos(\varphi) + a \sin(\varphi) \right) \right]. \quad (4.17) \]

Hence from equation (4.17), we obtain:

\[ \Delta V = \frac{\omega_d \cdot I_{(av)}ia}{f_i C \left[ \omega_d - e^{-a\omega_a t} \left( \omega_d \cos(\varphi) + a \sin(\varphi) \right) \right]}, \quad (4.18) \]

where the average capacitor current, \( I_{(av)}ia \), is obtain from:

\[ q_{ia} = I_{(av)}ia / f_i. \quad (4.19) \]

The energy loss, \( E_{ia} \), dissipated in the sub-state ‘a’ at DCP mode calculated to be:

\[ E_{ia} = \int_{0}^{\phi/\omega_d} i^2 R dt = \int_{0}^{\phi/\omega_d} \left( \frac{\Delta V}{\omega_d L} e^{-at} \sin(\omega_d t) \right)^2 R \cdot dt = \left( \Delta V^2 R e^{-a\omega_a t} \left( -a^2 + \omega_a^2 \left( e^{2a\omega_a t} - 1 \right) + a^2 \cos(2\varphi) - a \omega_d \sin(2\varphi) \right) \right) = \frac{4aL \omega_d^2 \omega_a^2}{2} \left( e^{-a\omega_a t} \left( -a^2 + \left( e^{2a\omega_a t} - 1 \right) \omega_a^2 + a^2 \cos(2\varphi) - a \omega_d \sin(2\varphi) \right) \right). \quad (4.20) \]

Substituting (4.18) into (4.20) yields:

\[ E_{ia} = I_{(av)}ia^2 \left( \frac{e^{-a\omega_a t} \left( -a^2 + \left( e^{2a\omega_a t} - 1 \right) \omega_a^2 + a^2 \cos(2\varphi) - a \omega_d \sin(2\varphi) \right)} {2f_i^2 C \left[ \omega_d - e^{-a\omega_a t} \left( \omega_d \cos(\varphi) + a \sin(\varphi) \right) \right]^2} \right). \quad (4.21) \]

The power loss, \( P_{ia} \), dissipated in the sub-state ‘a’ can be calculated from the energy loss by multiplying it by \( f_i \). Once the power loss, \( P_{ia} \), is obtained, it can be directly used to express the equivalent resistance, \( R_{ia} \), taking into account the relative proportionality factor (i.e., \( I_{av} = k_i \cdot \rho_{ia} \cdot I_{out} \)). Hence, the equivalent resistance of the sub-state \( ia \), can be express as:

\[ R_{ia\_ext} = \frac{k_i^2}{2f_i C} \left( \frac{e^{-a\omega_a t} \left( -a^2 + \left( e^{2a\omega_a t} - 1 \right) \omega_a^2 + a \left( a \cos(2\varphi) - a \omega_d \sin(2\varphi) \right) - a^2 \right)} {\left( \omega_d \left( 1 + e^{-a\omega_a t} \right) \right)^2} \right). \quad (4.22) \]

Similarly, the equivalent resistance of the sub-state 'b', can be derived by solving the charge and energy loss integrals, \( (q_{ib}, E_{ib}) \), in the interval of \( \phi/\omega_d \) to \( \pi/\omega_d \). So, the equivalent resistance of the sub-state \( ib \), can be expressed as:

\[ R_{ib\_ext} = \frac{k_i^2}{2f_i C} \left( \frac{e^{-a\omega_a t} \left( a^2 + \omega_d^2 - a^2 \cos(2\varphi) + a \omega_d \sin(2\varphi) \right) - a^2 \cdot e^{-2a\omega_a t}} {\left( \omega_d \left( 1 + e^{-a\omega_a t} \right) \right)^2} \right). \quad (4.23) \]
4.5 Simulation & Experimental (Model Validation)

To validate the proposed model, two experimental prototypes were constructed. In the first prototype, a unity gain RSCC depicted in Fig. 4.13 was evaluated to confirm the analytical derivation. The second experiment demonstrated the strength of the modeling methodology by considering a voltage doubler RSCC configuration, as shown in Fig. 4.14. For both configurations, the proportionality factors were \( k_{1,2} = 1 \), and the frequency ratio was \( df_{1,2} = 1 \).

![Fig. 4.13. Unity gain SCC switching circuit, with charge phase operated in a DCP mode. (Switch \( S_{1b} \) blocks undesired conduction paths).](image)

![Fig. 4.14. Voltage doubler converter topology with free-wheeling diodes \( D_1, D_2 \). Charge phase: \( S_{1a}, S_{1b} \) – ON, discharge phase: \( S_{2a}, S_{2b} \) – ON.](image)

4.5.1 Unity converter

The experimental setup and simulation test bench parameters were: quality factor of the resonant tank was maintained above 20, output power range was between 3 and 30 W. Figure 4.15 shows typical waveforms of the sub-state currents demonstrating DCP operation. As can be observed, the phase current is commutated between two sub-states.

Three sets of experiments were carried out. In the first experiment, extraction of the equivalent resistance following the procedure detailed by expression (4.9) is verified. In this experiment the free-wheeling diode, \( D_{1b} \), was omitted, and replaced by an additional resistive conduction path using the transistor, \( S_{1b} \), (the ratio of \( R_{1b}/R_{1a} \) was approximately 10) (see Fig. 4.13). Figure 4.16 shows the
experimental results of the average currents at paths 1a and 1b as a function of the commutation phase \( \phi \), and the agreement to the theoretical calculations and the simulation derived results.

In the second experiment, the capability of the model to include diode losses was evaluated by implementing \( D_{1b} \) (see Fig. 4.13) using two diodes connected in series. The total average forward voltage drop, \( V_F \), of the two diodes at nominal current was estimated to be 1.7 V. Furthermore, to emphasize the voltage drop effect, all other loss contributors were made negligibly small. Figure 4.17 shows the results of the average equivalent diode voltage drop, \( V_d \), as a function of the commutation angle, \( \phi \), obtained from model calculations, simulations, and experimental measurements.

The third experiment summarizes the validity of the modeling methodology by considering both diode as well as resistive losses. This is done by changing the free-wheeling loop to include two diodes, as well as loop resistance \( R_{1b} \) (\( R_{1b}/R_{1a} \) was approximately 10) such that both elements contributed approximately equal amounts of losses. Figure 4.18 shows the values of the output voltage predicted by the model, simulation results, and experimental measurements.

![Fig. 4.15. Experimental waveforms obtained from a unity gain resonant SCC operating in DCP mode with \( \phi_i = 126^\circ \). Upper traces–charge sub-states currents, Bottom trace–discharge current. Scale: vertical–2 A/div, horizontal–2 \( \mu \)s/div.](image1)

![Fig. 4.16. Average currents at paths 1a and 1b. Model calculation–solid trace, simulation–dashed line, and experimental results–(I_{1a}) asterisk marks and (I_{1b}) circle marks.](image2)

![Fig. 4.17. Equivalent average diode voltage drop, \( V_d \), as a function of the commutation phase, \( \phi \). Model calculation–solid trace, simulation–dashed line, and experimental results–asterisk marks.](image3)
4.5.2 Voltage doubler SCC

The experimental and simulation results were obtained for several values of quality factors, commutation angles, $\phi_i$, on both the charge phase ($i=1$) and the discharge phase ($i=2$), average voltage drop, $V_F$, and loops resistances. Also included in this experiment is a case of a voltage doubler with self-commutation (DCP mode) in both the charging and discharging phases. Figures 4.19 – 4.21 show an example of the charge and discharge sub-states current waveforms, demonstrating the DCP operation of the converter. The output voltage ripple remained constant throughout the experiments and was measured to be around 200 mV. The experimental parameters and comparison of the results to the one obtained from the modeling methodology are summarized in Table 4.1, where charge/discharge sub-states that include diodes are marked by the index ‘b’. The model used to predict the output voltage value for this experiment is depicted in Fig. 4.22. A very good agreement was found between the values predicted by the model and the experimental results (deviation of less than 1%). It should be noted that the reason for the relatively high inductance value that has been used for the experiments is to allow model validation by the insertion of non-negligible series resistances to the loop while maintaining a sufficiently high quality factor as required by the assumptions of the modeling approach. For practical application with lower on-resistance switches, the values of the passive components will comply with the commonly used values.

Table 4.1 - Voltage doubler converter–Summary of experimental results at $V_{in}=10$ V, $C_i=440$ nF,

$L_i=46$ µH, $C_o=100$ µF, and $f_s=35$ kHz

<table>
<thead>
<tr>
<th>Parameters</th>
<th>$\phi_i$ [degrees]</th>
<th>$\phi_i=103$</th>
<th>$\phi_i=149$</th>
<th>$\phi_i=90$</th>
<th>$\phi_i=123$</th>
<th>$\phi_i=150$</th>
<th>$\phi_i=90$</th>
<th>$\phi_i=139$</th>
<th>$\phi_i=139$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{loop1a}$, $R_{loop2a}$ [mΩ]</td>
<td>100 100 370 370 370 370 700 700</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{loop1b}$, $R_{loop2b}$ [mΩ]</td>
<td>100 100 100 100 100 100 100 100</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{loop2a}$ (worst case)</td>
<td>102 102 27 27 27 27 14.6 14.6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_F(D_1, D_2)$ [V]</td>
<td>1.7 0.85 1.7 1.7 1.7 1.7 1.7 1.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_o$ [Ω], $P_o$ [W]</td>
<td>30.11.4 50.7.7 30.10 30.10.6 30.10.9 30.11.3 30.9.5 30.10.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Efficiency</td>
<td>0.91 0.96 0.86 0.88 0.89 0.91 0.85 0.86</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_o$ (DC) Simulation [V]</td>
<td>18.83 19.63 17.61 18 18.31 18.54 17.14 17.65</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_o$ (DC) Experimental [V]</td>
<td>18.7 19.76 17.5 18 18.24 18.5 17 17.63</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_o$ (DC) Model [V]</td>
<td>18.79 19.65 17.62 18.18 18.36 18.46 17.12 17.67</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Fig. 4.19. Experimental waveforms obtained from a double gain resonant SCC operating in DCP mode with $\phi_1=96^\circ$, $\phi_2=139^\circ$, $V_{in}=10$ V, $R_{loop1a,2a}=370$ m$\Omega$, $R_{loop1b,2b}=100$ m$\Omega$, $V_{F1,2}=1.7$ V, $P_{out}=10.6$ W. Upper traces–charge sub-states currents, bottom trace–discharge sub-states currents. Scale: vertical–2 A/div, horizontal–5 $\mu$s/div.

Fig. 4.20. Experimental waveforms obtained from a double gain resonant SCC operating in DCP mode with $\phi_1=\phi_2=139^\circ$, $V_{in}=10$ V, $R_{loop1a,2a}=370$ m$\Omega$, $R_{loop1b,2b}=100$ m$\Omega$, $V_{F1,2}=1.7$ V, $P_{out}=11.13$ W. Upper traces–charge sub-states currents, bottom trace–discharge sub-states currents. Scale: vertical–2 A/div, horizontal–5 $\mu$s/div.

Fig. 4.21. Experimental waveforms obtained from a double gain resonant SCC operating in DCP mode with $\phi_1=148^\circ$, $\phi_2=139^\circ$, $V_{in}=10$ V, $R_{loop1a,2a}=370$ m$\Omega$, $R_{loop1b,2b}=100$ m$\Omega$, $V_{F1,2}=1.7$ V, $P_{out}=11.3$ W. Upper traces–charge sub-states currents, bottom trace–discharge sub-states currents. Scale: vertical–2 A/div, horizontal–5 $\mu$s/div.

Fig. 4.22. SCC generic average equivalent circuit that shows the contribution of the partial sub-circuits equivalent resistances $R_{ei}$ to the total equivalent circuit resistance $R_e$. (For the doubler SCC example of Fig. 4.14, $R_{e1a}$ is the loss contribution of charge sub-state 1a, $R_{e1b}$ and $V_{d1b}$ are the resistive and diode loss contribution of the free-wheeling sub-state, respectively. $R_{e2a}$ is the loss contribution of the discharge sub-state 2a, $R_{e2b}$ and $V_{d2b}$ are resistive and diode loss contribution of the free-wheeling discharge sub-state, respectively).
4.5.3 Multiphase Fibonacci resonant SCC

To further demonstrate the strength of the modeling methodology to predict the origin of the conduction losses, a multiphase Fibonacci-type resonant SCC [68] has been examined by simulation and compared to the results of the presented model. The converter in Fig. 4.23 includes four conduction phases to build the output voltage up by eight times the input voltage. To obtain a free-wheeling ZCS operation, each commutation phase includes a DCP mode as can be observed from the current waveforms in Fig. 4.24.

The transistors have been assigned with identical on-resistances, yielding the following per-phase resistances: \( R_{\text{loop1}} = 2R_{\text{DSon}} \), \( R_{\text{loop2}} = 3R_{\text{DSon}} \), \( R_{\text{loop3}} = 4R_{\text{DSon}} \), and \( R_{\text{loop4}} = 4R_{\text{DSon}} \). The proportionality factors are \( k_1 = 4 \), \( k_2 = 2 \), and \( k_3 = k_4 = 1 \), and the frequency ratio \( df_{1-4} \) is 1.

Validation of the model is carried out by simulation considering both the diode as well as resistive losses. Figure 4.25 shows the values of the output voltage predicted by the model compared with the results of a cycle-by-cycle simulation. The target parameters of the multiphase Fibonacci SCC simulations are: \( V_{\text{in}} = 5 \) V, \( V_{\text{F1-4}} = 1.7 \) V, \( R_{\text{DSon}} = 10 \) mΩ, \( R_o = 50 \) Ω, \( L_s = 2.1 \) µH, \( C_i = 10 \) µF, and \( f_s \approx 24 \) kHz. Very good agreement has been found between the values predicted by the model and the simulation results (maximum deviation of 1.5%). The results in Figs. 4.26a and b show the contribution of losses, separated into resistive and voltage drop parts.

![Multiphase Fibonacci resonant SCC topology with free-wheeling diodes D1-D4](image)

Fig. 4.23. Multiphase Fibonacci resonant SCC topology with free-wheeling diodes D1-D4. Phase 1: S1, S3–ON, Phase 2: S2, S4, S6–ON, Phase 3: S3, S5, S7, S9–ON, Phase 4: S2, S5, S8, S10–ON.

![Simulation waveforms obtained from a resonant Fibonacci SCC operating in DCP mode with \( \phi_i \approx 144^\circ \)](image)

Fig. 4.24. Simulation waveforms obtained from a resonant Fibonacci SCC operating in DCP mode with \( \phi_i \approx 144^\circ \).
Fig. 4.25. Output voltage of the DCP operation mode of a resonant Fibonacci SCC as a function of the commutation angle, $\phi$. Model calculation–solid trace, simulation–asterisk marks.

Fig. 4.26. Contribution of conduction losses of the resonant Fibonacci SCC operated in DCP mode. (a) Equivalent resistant, $R_e$, as a function of the commutation angle, $\phi$ (b) Equivalent average diode voltage drop, $V_d$, as a function of the commutation angle, $\phi$. 

68
4.5.4 Model validation for low $Q$

To validate the formulas of the extended equivalent resistances, $R_{1a,ext}$ and $R_{1b,ext}$, unit gain (Fig. 4.13) with charge phase operated in a DCP mode was simulated and compared to the results of the presented model. Simulations were set-up at: $V_{in}=10\ \text{V}$, $C_i=100\ \mu\text{F}$, $L_i=1\ \mu\text{H}$, $Q_{1a}=Q_{1b}=0.55$, $Q_2=1$, ($R_{\text{loop1a}}=R_{\text{loop1b}}=0.18\ \Omega$, $R_{\text{loop2}}=100\ \text{m\Omega}$), $R_o=5\ \Omega$, and $f_s=9.23\ \text{kHz}$. The proportionality factors were $k_{1,2}=1$, and the frequency ratio was $df_{1,2}=1$. Figure 4.27 shows the simulation results of the average currents at paths 1a and 1b as a function of the commutation phase $\phi$, and the agreement to the theoretical calculations. Very good agreement was found between the values predict by model and simulation results.

![Graph showing average currents at paths 1a and 1b at low $Q$ as function of $\phi$. Model calculation—($I_{1b}$) solid trace and ($I_{1a}$) dashed line, simulation results—($I_{1a}$) asterisk marks and ($I_{1b}$) circle marks.](image-url)

Fig. 4.27. Average currents at paths 1a and 1b at low $Q$ as function of $\phi$. Model calculation—($I_{1b}$) solid trace and ($I_{1a}$) dashed line, simulation results—($I_{1a}$) asterisk marks and ($I_{1b}$) circle marks.
4.6 Discussion and conclusions

This thesis presented a modeling approach of resonant SCC that is applicable to both the conventional resonant operation as well as to converters that operate in a more general case of a divided conduction path ZCS. The modeling concept applies representation of the resistive losses by partial equivalent resistance and losses originated from P-N junction devices, all with respect to the output current of the converter. Although rigorously demonstrated on a relatively simple case of two conduction paths, the modeling methodology is well-qualified to extract the behavior of a resonant SCC with any number of split current loops, such as a resonant Fibonacci converter, exemplified in Section 4.5.3. The resultant model is limited, however, within the assumptions specified, to resonant networks with relatively high quality factors, i.e., sinusoidal resonant current.

The experimental study confirmed the validity of the modeling method to distinguish between losses types (resistive and voltage drop) with excellent agreement between the analytical derivations, simulations, and experimental results. It was found that while the partial equivalent resistances are extracted as a function of the rms currents and the related commutation phase, the equivalent average diode voltage source depends primarily on the ratio between the sub-states charges (proportionality factor, $\rho$).

The overall efficiency in circuits operated in a DCP mode is highly dependent on the loss amount in each of the conduction paths. It is assumed throughout this work that switches with a resistive behavior, i.e., MOSFETs have lower conduction losses than devices based on a P-N junction, which is the case in modern power components for low and intermediate voltage conversion applications. Hence, there exists a tradeoff between the target efficiency and the component tolerances. Wider component variance from their nominal values results in higher uncertainty of the zero crossing point and longer duration of diode conduction path, which translates into higher losses. It should also be noted that from an efficiency point of view, the lossy diode-based conduction path is to be activated in the vicinity of zero current, so it’s contribution to the losses is minimized.

A self-commutation approach may not be compatible with all converter configurations, for example, converters where the voltage difference between input and output is higher than the forward voltage drop of the free-wheeling diode. Under these conditions undesirable current paths may appear. It should be noted that the presented modeling methodology focuses on the dominant part of the contributing losses in resonant SCC and omits the discussion on other issues such as EMI effects, gate drive losses, etc.

The DCP operation mode can significantly simplify the control effort and eliminate the additional circuitry that is required to achieve ZCS in resonant converters and in particular for resonant SCC that require active ZCD to improve the power conversion efficiency.
Chapter 5 - Contribution of Thesis and Suggestions for Future Research

5.1 Contribution of thesis

The key contributions of this work are summarized as follows:

**Generalized method of active ZCD for multiphase resonant SCCs.** This research presents an active method for ZCS for resonant SCC with a wide dynamic range. The method is demonstrated on a resonant binary and Fibonacci SCC that feature a wide range of conversion ratios. This approach reduces the power losses by reducing the switching losses together with increasing the number of target voltages. Due to the resultant high efficiency of the converter operating under soft-switching conditions, it is applicable for higher power levels up to the medium power range. A zero detection method was developed that was capable of compensating for both the processing delays (from detection to switching action) and for the large variations of the resonant characteristics (due to transition between sub-circuits), and for any other component variations.

**A Unique isolated gate driver** with an extremely wide range of duty cycle and frequency was developed. This work discusses the construction and component selection of the floating driver. The isolated driver can be suitable with many other applications.

**Design guideline of multiphase resonant SCC.** For proper construction of a high power multiphase SCC application with desired target efficiency, a set of design considerations for the selection of the power stage components, for a multiple sub-circuits converter has been delineated. The design method of multilevel SCCs with respect to conduction losses and efficiency was demonstrated and verified to successfully operate resonant binary SCC and to accommodate a wide and dynamic operation range and can be applied to other complex multi-phase SCC topologies that involve a number of sub-circuits and wide operation ranges at high power levels.

**Unified modeling methodology of self-commutation ZCS.** This study introduces a unified modeling methodology to describe and explore the loss mechanism of resonant SCC operating in a self-commutation ZCS mode. The new modeling concept is compatible to describe the losses resulting from resistive elements as well as P-N junction devices. The model can help in the simplification and optimization of SCC systems and their control to achieve high efficiency up to the high power range.

5.2 Suggestions for future research

Some suggestions for future lines of investigation that can be developed as a result of this thesis are outlined below:
Examination of the SCC design method with additional topologies. The multiphase SCC design method developed can be adapted for traditional inductor-based dc-dc converters and can be examined with more practical SCC topology ranging from low to high power.

Equivalent average diode voltage drop for low $Q$. The study that was carried out on the loss mechanism of resonant SCCs operating in a self-commutation ZCS mode can be expended to a closed-form solution. The model can be expanded to include the loss resulting from P-N junction devices at low quality factors.

Equivalent resistance model for higher-order networks. The equivalent resistance model is valid for cases where the sub-circuits of the converter can be described or approximated by a first and second order ($RC$ and $RCL$, respectively) networks. The method that was used to describe the loss in a self-commutation ZCS mode can be used to explore the modeling for the cases where there are several $RC$ times constants and for higher order networks.
References


Appendix

Appendix I - Further analysis of the resonant binary/Fibonacci SCC

Figure A.1 shows the proposed topology for a step-down resonant binary/Fibonacci SCC. In this study, ZCS is obtained by the stray inductor and with a single air core inductor, $L_s$. Step-up conversion can also be achieved by swapping the input and output stages as depicted in Fig A.2.

![Resonant binary/Fibonacci switched capacitor step-down converter, example for $n=3$.](image1)

Fig. A.1. Resonant binary/Fibonacci switched capacitor step-down converter, example for $n=3$.

![Resonant binary/Fibonacci switched capacitor step-up converter, example for $n=3$.](image2)

Fig. A.2. Resonant binary/Fibonacci switched capacitor step-up converter, example for $n=3$.

The analysis is performed on a step-down resonant SCC as shown in Fig. A.1. The connection of $V_{in}$ is defined by the coefficient $A_0$ in each of the EXB/SFN codes for a given conversion ratio, $M_n$. All flying capacitors are always connected serially according to the coefficient $A_j$. We can summarize the rules of the topological interconnections of $V_{in}$, $C_j$, and $C_o$ as follows:

1. If $A_0 = 1$, then $V_{in}$ is connected.
2. If $A_0 = 0$, then $V_{in}$ is not connected.
3. If $A_j = -1$, then $C_j$ is charged.
4. If $A_j = 0$, then $C_j$ is not connected.
5. If $A_j = 1$, then $C_j$ is discharged.

For example, in the case of $M=5/8$, this will result in the EXB codes as presented in Table 1.1, that is translated to the corresponding resonant SCC topologies of Table A.1. Thus, each EXB code leads to a specific series of high-order $RCL$ circuits in every state. The specific topologies are depicted in Fig. 2.2.

<table>
<thead>
<tr>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$S_3$</th>
<th>$S_4$</th>
<th>$S_5$</th>
<th>$S_6$</th>
<th>$S_7$</th>
<th>$S_8$</th>
<th>$S_9$</th>
<th>$S_{10}$</th>
<th>$S_{11}$</th>
<th>$S_{12}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Table A.1 - The switches state according to the EXB codes
For a simplification of the mathematical analysis on the topologies depicted in Fig. A.1, a steady-state operation and very light output load are assumed. The KVL can be obtained for each topology for the average voltages. Furthermore, at steady-state, $\dot{V}_{ls} = 0$ for each of the sub circuits. This leads to system of five linear equations and four unknowns.

\[
\begin{align*}
V_{in} + 0 - V_{c2} - V_{c3} &= V_{co} \\
V_{in} - V_{c1} + V_{c2} - V_{c3} &= V_{co} \\
0 + V_{c1} + V_{c2} - V_{c3} &= V_{co} \\
V_{in} - V_{c1} + 0 + V_{c3} &= V_{co} \\
0 + V_{c1} + 0 + V_{c3} &= V_{co}
\end{align*}
\]  

(A.1)

Grouping the unknowns in (A.1) at the left hand side and normalizing it to $V_{in}$ yields (A.2).

\[
\begin{bmatrix}
0 & -1 & -1 \\
-1 & 1 & -1 \\
1 & 1 & -1 \\
-1 & 0 & 1 \\
1 & 0 & 1
\end{bmatrix}
\begin{bmatrix}
V_{c1}/V_{in} \\
V_{c2}/V_{in} \\
V_{c3}/V_{in} \\
V_{co}/V_{in}
\end{bmatrix}
= 
\begin{bmatrix}
-1 \\
-1 \\
0 \\
-1 \\
0
\end{bmatrix}
\]  

(A.2)

Solving the system of (A.2) we obtain the voltages across the flying capacitor and the output stage: $V_{c1}=(1/2)V_{in}$, $V_{c2}=(1/4)V_{in}$, $V_{c3}=(1/8)V_{in}$, and $V_{co}=(5/8)V_{in}$. Since this is the unique solution [22] there is no need for any control system to assure that the capacitors have stabilized at their corresponding nominal voltages.
Appendix II - Analysis of the Fibonacci SCC

Figure 4.23 shows a resonant multiphase converter with the ideal step-up conversion ratio $M=8$. The flying capacitors’ voltages follow the Fibonacci sequence [68]. Following the switching sequence, the average voltages across the flying capacitors and the output voltage will adjust to: $V_{C1}=V_{in}$, $V_{C2}=2V_{in}$, $V_{C3}=4V_{in}$, and $V_{C4}=8V_{in}$.

The contribution of each flying capacitor to the average output current may be derived from the equivalent $RCL$ circuits of Fig. A.3. Under steady-state operation, charge balance of all capacitors is satisfied (i.e., average current equals zero). The sum of the currents for each state $I_1$-$I_4$, and the sum of all currents, can be expressed as:

$$
\begin{align*}
I_1 - I_2 - I_3 - I_4 &= 0 : C_1 \\
0 + I_2 - I_3 - I_4 &= 0 : C_2 \\
0 + 0 + I_3 - I_4 &= 0 : C_3 \\
0 + 0 + 0 + I_4 &= I_o
\end{align*}
$$

where the currents $I_j$ are the average currents of each sub-circuit (averaged over the entire switching period).

The solution of the system obtains the proportional coefficient between the average current of the flying capacitor and output current for state $j$, so, $k_1=4$, $k_2=2$, and $k_3=k_4=1$.

Fig. A.3. Resonant SCC sub-circuits configured from the Fibonacci sequence $M=8$. 

![Diagram of Resonant SCC sub-circuits configured from the Fibonacci sequence M=8.](image-url)
Magnetic coupling currents are a subset of the family of power electronics converters, which are integrated into the power electronics system. In contrast to traditional magnetic coupling converters, whose operation is based on magnetic components for energy storage, magnetic coupling converters, which are not dependent on magnetic components, are ideal for integration into power electronics systems. These converters are commonly used in power supplies and low-ratio applications due to the internal energy losses resulting from the charging and discharging of the cables, the energy losses of the converter, and the energy losses of the transformation.

The main objective of the thesis is to improve the behavior and performance of various systems based on magnetic coupling converters in the high-power field. The applications and methods presented in this work focus on high efficiency and cover a wide range of target voltages and soft switching. Typically, these challenges limit the implementation of magnetic coupling converters in the mid-range and high-power field. This research presents a simple and effective driver for the implementation of soft switching. In addition to applications, this work presents an effective and reliable design process for magnetic coupling converters, multi-phase, in terms of efficiency and desired ratio. This research includes a detailed analysis, theoretical analysis, a practical application, and experimental results. These parts of the research were published in the IEEE Energy Conversion Congress and Exposition (ECCE) 2013 [1], IEEE Transactions on Power Electronics [2], IEEE Applied Power Electronics Conference (APEC) 2014 [3], and additional work was published in the journal IEEE Electrical Engineering and Technology [4].

The purpose of this research is to directly influence researchers and developers of converters, controllers, and power supplies in a wide range of systems.

Keywords: power losses, soft switching, static model, model, zero current, direct current to direct current power converters, magnetic coupling converters, magnetic coupling converters, soft switching, soft switching, double transition, binary codes.
מיתוג רך בצמידי קבלים מחותמים

הبحر והממקים חול מתחדשים לקבלת תואר ראשון בהנדסה

מאת: אליל חמו

בenburgית:

דוקטור מור מרדכי פרץ

05/01/15

תאריך: אליל חמו

מנחה: ד"ר מור מרדכי פרץ

05/01/15

תאריך: ד"ר מור מרדכי פרץ

05/01/15

תאריך: ארנון ר"ז noreferrer תואר שני
ミיתוג רך במעניין קבלים ממוחדים

חיבור זה מתווה חלקי מחדרישות לפקולטה למדעי הנדסה וbrate מחקר ונדס במנחה

נאת: אליה חמות

בנagine:

דוקטור מרדכי פרץ