EFFICIENT ENERGY PROCESSING AND VOLUME REDUCTION OF SWITCHED-MODE CONVERTERS

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE MSc. DEGREE

By: Or Kirshenboim

Supervised by:
Dr. Mor Mordechai Peretz

October 2015
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October 2015
שיפור יעילות עבודה הספק ה.clientHeight הקטנת מימדים של מקרירים ממתגין

ה微商 הזMahon החלק ממאוריית לקבלת תואר מנהר במנהלת

מהנה: אור קירשנבוים

マンה: ד“ר מרדכי פרץ

October 2015
שיפור יעילות עיבוד הספק והקמת מידיות של ממירים מומחים

CallCheckת ההנדסה

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תאריך: ........................
Dedicated to my wife, Michal, who encouraged me to aspire heights and ignore any limitations that got in the way, since all limitations are simply waiting there for someone to break them.

∞

October 2015
токיציר

העבודה מציגה אתגרים בהתקדמות של ממירים הספק ממותגים לכיוון של צפיפות הספק גבוהה וזמני תגובה קצרים. העבודה מתמקדת בעיקר בבעיית תופעת המעבר בעומס של ממירים ממותגים, בעיה אשר מגבילה את מזעור המערכות הללו. המטרה העיקרית של עבודה זו היא להקטין את המימדים של ממירים ממותגים ולהפוך את יעילות עיבוד האנרגיה של ממירים אלו. לצורך כך נחקרו שתי גישות:

1. שינוי מבני של הממיר כך שיהיה ייעודי לדרישות של אפליקציה מסויימת,
2. שימוש בשיטות בקרה לא לינאריות מתקדמות המבוססות על מרחב המצב. בהקשר של שיטות בקרה לא לינאריות, פותחה שיטת ניתוח יציבות של ממירים בעלי מבנה של העברה אנרגיה לא ישירה.


мяור המחקר של ניתוח היציבות הניחו את היסודות לפיתוח של שיטות בקרה חדשות לממירים בעל מבנה של העברה אנרגיה לא ישירה. בעבודה זו מוצגת שיטה חדשה לתיאור הקשר בין זמן ההתכנסות לתנועה על המרחב המצב. בעזרת שיטה זו פותח בקר לא לינארי חדש מבוסס על מרחב המצב אשר מפיק תגובה סופר מהירה לתופעת מעבר בעומס תוך כדי שהוא מגבל את שינוי מתח המוצא. על ידי כך, הבקר החדש מקטין את הדרישות המימדית של הרכיבים הריאקטיביים, מה שמאפשר פתרון פשוט וזול. המחקר כולל ניתוח תיאורטי מלא, שיטת בקרה מפורטת, השלכות מעשיות ותוצאות מעשיות. חלק זה של המחקר פורסם כמאמר בכנס IEEE Workshop on Control and Modeling for Power Electronics [3].
Abstract

This thesis addresses the present-day challenges in the advancement of switched-mode converters towards high power density and fast response times. The work mainly covers the load transient problem of switched-mode power supplies, a problem that limits the miniaturization of these systems. The primary aim of this thesis is to reduce the overall volume of switched-mode converters and to improve the energy processing of these systems. Two methods are studied for this purpose: 1) modification of a converter structure so that it will be more application oriented, 2) advanced state-space based nonlinear control methods. Within the context of nonlinear control methods, a new stability analysis has been developed for indirect energy transfer (IET) converters.

One objective of this thesis is to improve the load transient response of voltage regulator modules (VRMs). The size of the reactive components of VRMs is determined by the load transient response, Therefore, by improving this response, i.e. reducing the output voltage deviation and transient time, a significant reduction of the reactive components’ size and volume can be achieved. To reach this goal, this work presents a new hybrid-VRM to improve loading and unloading transient response using a load-side auxiliary gyrator circuit. This VRM solution hybrids a buck converter with a resonant switched-capacitor auxiliary circuit that is connected at the load side. By incorporating two converters, one that excels in steady-state operation to maintain high efficiency and one that can produce a current step response, an increased capacitance at the output of the converter is mimicked. Moreover, by incorporating a new control method, the hybrid-VRM requires indication from the output voltage alone, without additional current sensors, making this solution simple and cost-effective. The research includes full behavioral description, power processing analysis, detailed control method and experimental results. This part of the research has been published in the proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC) 2015 [1], and within a larger study that has been submitted to the IEEE Transactions on Power Electronics.

Another objective of this thesis is to study new control methods to improve the load transient response of IET converters. Within the context of this objective, a new stability analysis of control methods for IET converters has been developed. It explores the existence of stability for converters that are controlled by either boundary or hybrid controllers and introduces a new simplified procedure for examination of large-signal stability using a graphical-analytical approach. The outcome of stability analysis leads to the definition of the large-signal region-of-convergence that is described on the state-plane. The research includes full stability analysis for variety of converters and load types, detailed stability examination procedure, examination of
stability of modern control methods and experimental results. This part of the research has been published in the IEEE Transactions on Power Electronics [2].

The results of the stability analysis lay the foundations for the development of new control methods for IET converters. In this work a new method to describe the relationship between the time of convergence and the movement on the state-plane is presented. Using this method, a new nonlinear state-space based controller that can produce extremely fast load transient response while constraining the output voltage deviation has been developed. By doing so, the new controller significantly reduces the reactive components’ stress while maintaining simple implementation. The research includes full theoretic analysis, detailed control method, practical considerations and experimental results. This part of the research has been published in the proceedings of the IEEE Workshop on Control and Modeling for Power Electronics [3] and received the best paper award.
Thesis Overview

The thesis covers issues of voltage regulator modules and control of IET converters. The voltage regulator modules part deals with the aspects of topology modification specially tailored for low-voltage high-current applications that deal with large load transients. The control of IET converters part is divided into two topics: 1) Stability analysis of controllers for IET converters and new simplified stability examination procedure, 2) A new control method for IET converters that minimizes both load transient response time and components’ stress.

The thesis is organized as follows: Chapter 1 introduces the field of power electronics and provides a comprehensive review of design, modeling and control of present-day switched-mode converters. The core chapters of this thesis (2-4) are divided into three subjects: Chapter 2 presents a new hybrid voltage regulator module to improve the loading and unloading transient response of voltage regulator modules. A new stability analysis for IET converters is presented in Chapter 3. The stability analysis of Chapter 3 lays the foundations for the development and examination of new control methods for IET converters. A new one control method for IET converters is presented in Chapter 4. The core chapters have been published as papers in conferences and journals: Chapter 2 is published in [1], Chapter 3 is published in [2] and Chapter 4 is published in [3].
Acknowledgments

I would like to thank my supervisor Dr. Mor Mordechai Peretz, with whom I worked for three intensive years. Dr. Peretz has been a supportive tutor and a friend. I thank him for teaching me how to think outside of the box, to be persistent and to bring any achievement to perfection. I also thank him for improving my learning and writing skills and for giving me splendid ideas throughout the way.

I want to thank Mr. Alon Cervera, for being a great colleague and friend. I thank him for his collaboration, research work, and ideas. Alon is always happy to help everyone, at anytime, anywhere.

I must not forget all the students here at the Center for Power Electronics and Mixed-Signal IC whose support and friendship meant so much: Mr. Ofer Ezra, Mr. Eli Abramov, Mr. Timur Vekslender, Mr. Yevgeny Bezdenezhnykh, Mr. Bar Halivli, Mr. Alon Blumenfeld, Ms. Yara Halihal, Mr. Eli Hemo, Mr. Idan Ozana and anyone that I have forgotten to mention by name.

Of the technical staff, I would like to thank Azrikam Yehieli and Neli Grinberg, who are responsible for the excellent working and social conditions of the laboratory.

With great appreciation I thank my dear wife Michal, for her tremendous loving support, patience and care. I want to thank my parents and brothers for their support and care, and for their contribution, each in his area of expertise.
# Table of Contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Table of Contents</td>
<td>i</td>
</tr>
<tr>
<td>Abstract</td>
<td>ii</td>
</tr>
<tr>
<td>Thesis Overview</td>
<td>iv</td>
</tr>
<tr>
<td>Acknowledgments</td>
<td>v</td>
</tr>
<tr>
<td>Table of Contents</td>
<td>vi</td>
</tr>
<tr>
<td>Figures List</td>
<td>ix</td>
</tr>
<tr>
<td>Tables List</td>
<td>xii</td>
</tr>
<tr>
<td>Acronyms and Abbreviations</td>
<td>xiii</td>
</tr>
<tr>
<td><strong>1. Introduction</strong></td>
<td>1</td>
</tr>
<tr>
<td>1.1. Overview of power converters</td>
<td>1</td>
</tr>
<tr>
<td>1.1.1. Linear regulators</td>
<td></td>
</tr>
<tr>
<td>1.1.2. Switched-mode converters</td>
<td>2</td>
</tr>
<tr>
<td>1.1.3. Direct energy transfer topologies</td>
<td>4</td>
</tr>
<tr>
<td>1.1.4. Indirect energy transfer topologies</td>
<td>5</td>
</tr>
<tr>
<td>1.1.5. Switched-capacitor converters</td>
<td>5</td>
</tr>
<tr>
<td>1.1.6. Resonant switched-capacitor converters</td>
<td>6</td>
</tr>
<tr>
<td>1.1.7.1. Principle of operation</td>
<td>8</td>
</tr>
<tr>
<td>1.1.8. DC-DC converter components design</td>
<td>10</td>
</tr>
<tr>
<td>1.2. State-space representation of switched-mode converters</td>
<td>12</td>
</tr>
<tr>
<td>1.2.1. State variables</td>
<td>14</td>
</tr>
<tr>
<td>1.2.2. State equations of switched-mode converters</td>
<td>14</td>
</tr>
<tr>
<td>1.2.3. State trajectories construction</td>
<td>15</td>
</tr>
<tr>
<td>1.3. Control of switched-mode converters</td>
<td>16</td>
</tr>
<tr>
<td>1.3.1. Linear control methods</td>
<td>16</td>
</tr>
<tr>
<td>1.3.1.1. Voltage-mode control</td>
<td>16</td>
</tr>
<tr>
<td>1.3.1.2. Current-mode control</td>
<td>18</td>
</tr>
<tr>
<td>1.3.1.3. Peak current-mode control</td>
<td>19</td>
</tr>
<tr>
<td>1.3.2. Digital control of switched-mode converters</td>
<td>20</td>
</tr>
<tr>
<td>1.3.3. Nonlinear control methods</td>
<td>20</td>
</tr>
<tr>
<td>1.3.3.1. Sliding-mode control</td>
<td>21</td>
</tr>
<tr>
<td>1.3.3.2. Boundary control</td>
<td>22</td>
</tr>
<tr>
<td>1.3.4. Load transient oriented control methods</td>
<td>23</td>
</tr>
<tr>
<td>1.3.4.1. Hybrid control</td>
<td>24</td>
</tr>
<tr>
<td>1.3.4.2. Time-optimal control</td>
<td>25</td>
</tr>
<tr>
<td>1.3.4.3. Minimum-deviation control</td>
<td>25</td>
</tr>
<tr>
<td>1.3.4.4. Programmable-deviation control</td>
<td>26</td>
</tr>
</tbody>
</table>

October 2015
2. Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit ................................................................. 33

2.1. Overview ........................................................................................................... 33
2.2. Transient recovery by a load-side auxiliary circuit .......................................... 34
2.3. Power processing efficiency ............................................................................ 36
2.4. Gyrator resonant switched-capacitor converter auxiliary circuit ...................... 38
2.5. Hybrid-VRM controller .................................................................................... 40
  2.5.1. Principle of operation ................................................................................. 40
  2.5.2. Comparators threshold settings ................................................................. 41
  2.5.3. Auxiliary circuit halt time – Tpreset .......................................................... 42
  2.5.4. Auxiliary capacitor voltage reset ................................................................. 44
2.6. Experimental verification .................................................................................. 45
2.7. Conclusion ........................................................................................................ 48

3. Stability Analysis of Boundary and Hybrid Controllers for Indirect Energy Transfer Converters .................................................................................................. 50

3.1. Overview .......................................................................................................... 50
3.2. Review: the load-line ....................................................................................... 52
3.3. Stability analysis .............................................................................................. 53
  3.3.1. Resistive load stability analysis ................................................................. 54
  3.3.2. Constant current load stability analysis .................................................... 57
  3.3.3. Physical interpretation of the stability conditions ...................................... 59
  3.3.4. Stability examination procedure ............................................................... 60
  3.3.5. Expansion of the Stability Analysis to Other Second-Order Indirect Energy Transfer Converters ...62
3.4. Experimental verification .................................................................................. 64
3.5. Conclusion ........................................................................................................ 67

4. Minimum-Time within a Deviation-Constrained Hybrid Controller for Boost Converters .................................................................................................. 68

4.1. Overview .......................................................................................................... 68
4.2. State-plane and time representation .................................................................. 69
4.3. Minimum-time within a deviation-constrained hybrid controller ...................... 70
  4.3.2. Principle of operation ................................................................................. 71
4.4. Minimum expected voltage drop ...................................................................... 72
4.5. Experimental verification .................................................................................. 75
4.6. Conclusion ........................................................................................................ 75
5. Discussion ............................................................................................................................................. 77

5.1. Contribution of the research ........................................................................................................... 77
5.2. Suggestions for future research ...................................................................................................... 78

6. Appendix – Derivation of the state trajectories for buck and boost converters .................. 79

7. References ........................................................................................................................................... 81
Figures List

Fig. 1.1  A basic linear regulator: (a) Equivalent circuit model, (b) a simple practise implementation. ..................2
Fig. 1.2  Basic dc-dc switching converter: (a) Equivalent switching circuit (b) Output voltage ...............................2
Fig. 1.3  (a) Buck dc-dc converter, (b) Typical current and voltage waveforms of an ideal converter. ....................3
Fig. 1.4  (a) Boost converter, (b) Buck-boost converter ...................................................................................4
Fig. 1.5  Direct energy transfer converters: (a) buck, (b) forward. .................................................................4
Fig. 1.6  Indirect energy transfer converters: (a) Boost, (b) Buck-boost, (c) Noninverting buck-boost, (d) Flyback. .................................................................5
Fig. 1.7  Basic 1st order switched-capacitor converter ....................................................................................6
Fig. 1.8  A basic resonant (2nd order) switched-capacitor converter.............................................................6
Fig. 1.9  Typical waveforms of the flying capacitor in the resonant SCC described in Fig. 1.8: dotted line - Ic, solid line - Vc, flat step - average Ic, corresponding to each switching cycle. .........................................................7
Fig. 1.10  The gyrorator resonant switched-capacitor converter configuration and operation principle: (a) charge, (b) discharge, (c) balance states. .................................................................9
Fig. 1.11  Typical waveforms of the flying capacitor voltage and current. Circuit parameters are: Vref=20V, Vc=31V, R=0.15Ω, L=5.2μH, C=0.25μF. .........................................................9
Fig. 1.12  A GRSCC realized in a bridge configuration, with optimized efficiency at voltage gain of A=2 (or A=0.5, depend on the power flow direction). ..............................................................10
Fig. 1.13  Buck converter circuit for (a) on state (b) off state. .................................................................14
Fig. 1.14  Typical structure of voltage-mode controlled power stage. ...........................................................17
Fig. 1.15  Buck converter controlled by a voltage-mode controller with a PI compensation network. ............17
Fig. 1.16  Current-mode control schematic of a synchronous buck converter. ..............................................18
Fig. 1.17  Peak current-mode control of a synchronous buck converter. ........................................................19
Fig. 1.18  Typical waveforms of peak current-mode controlled converter ....................................................19
Fig. 1.19  Digitally controlled SMPS. ........................................................................................................20
Fig. 1.20  Sliding-mode controller operation and the resultant controlled trajectories on the state-plane. .........22
Fig. 1.21  Trajectories behavior at different boundary crossing points: (a) reflective point, (b) refractive point, (c) rejective point. ........................................................................................................23
Fig. 1.22  Buck converter controlled by TOC response for a loading followed by an unloading transient. (a) Time response waveforms for inductor current and output voltage, (b) state-plane trajectories. ..................25
Fig. 1.23  Buck converter loading transient response with minimum-deviation controller. ..........................26
Fig. 1.24  Programmable-deviation controller regulating operation of a boost converter. ..................................26
Fig. 1.25  Operation of the programmable-deviation controller in a boost converter for loading transient (maximum switching frequency is limited). Inductor and load current (top), output voltage (middle), and state-plane representation of the voltage and current (bottom) ..................................................27
Fig. 1.26  Programmable-deviation controller switching boundaries for (a) on state (b) off state. ......................28
Fig. 1.27  Time-optimal response of boost converter controlled by a programmable-deviation controller during a loading transient: inductor and load current (top), output voltage (middle), and state-plane representation of the voltage and current (bottom)................................................28
Fig. 1.28  Energy transfer to the load: a main converter (a) steady-state operation, (b) during loading transient operation; a main converter with AEP (c) during steady-state operation, (d) during loading transient operation. Taken from [58] ...........................................................................................................29
Fig. 1.29  Input-side auxiliary circuit as an AEP. ................................................................................................31
Fig. 1.30  Load-side auxiliary circuit as an AEP. ................................................................................................31
Fig. 2.1  Hybrid-VRM with load-side GRSCC auxiliary circuit. The area within the bottom box is implemented within an FPGA. ...........................................................................33
Fig. 2.2  Simplified circuit with the auxiliary circuit modelled as a controlled current source, demonstrating the current relationships towards the load. .................................................................34

Fig. 2.3  Schematic response waveforms of the hybrid-VRM to an unloading step of \( \Delta I_{\text{out}} \) for different auxiliary behaviour. (a) \( I_{\text{aux}} = I_{\text{load}} - I_{\text{buck}} \), (b) \( I_{\text{aux}} = \Delta I_{\text{out}}/2 \), (c) \( I_{\text{aux}} > \Delta I_{\text{out}}/2 \), segmented to match the overall charge \( Q \). .................................................................34

Fig. 2.4  Power processing efficiency of a buck converter connected to a constant load, versus a 50kHz dynamic load with the same average current, 50% load duty-cycle (see Fig. 2.5). Series resistance is 10mΩ. ........................................................................................................36

Fig. 2.5  Inductor current waveforms for TOC (top), hybrid-VRM (middle) and ideal inductor behavior (bottom). ........................................................................................................37

Fig. 2.6  VRM efficiency as a function of load transient rate for two load-step magnitudes. \( R_{\text{load}}=10\text{mΩ} \), switching losses are not considered. .................................................................................................38

Fig. 2.7  Distribution of the auxiliary current between three interleaved GRSCCs operating at maximum frequency with half-resonance phase delay. .................................................................39

Fig. 2.8  Simulation results for the response of the hybrid-VRM to an unloading event. .................................40

Fig. 2.9  Flowchart of the end-of-transient algorithm. .........................................................................................41

Fig. 2.10  Possible range of the buck inductor current around the \( T_{\text{reset}} \) instance. ........................................43

Fig. 2.11  Simulated unloading transient followed by a reset of \( v_{\text{aux}} \) back to \( 2V_{\text{out}} \). .................................45

Fig. 2.12  Experimental results showing a 7A load transient response of the hybrid-VRM [(a),(c)] versus TOC [(b),(d)]. Signals from top to bottom: \( v_{\text{out}} \) (100mV/div, ac coupled), \( i_{\text{buck}} \) (5A/div), and load-step signal. Time scale is 5μs/div. (a),(b) 4.5A-11.5A loading event. (c),(d) 11.5-4.5A unloading event. .................................................................46

Fig. 2.13  Experimental results showing a 10A load transient response of the hybrid-VRM [(a), (c)] versus TOC [(b),(d)]. Signals from top to bottom: \( v_{\text{out}} \) [(a), (b) 100mV/div, (c), (d) 200mV/div, ac coupled], \( i_{\text{buck}} \) (5A/div), and load-step signal. Time scale is 5μs/div. (a), (b) 1.5A-11.5A loading event. (c), (d) 11.5-1.5A unloading event. .................................................................47

Fig. 2.14  Screenshot demonstrating the hybrid-VRM’s response to a repetitive 1KHz loading-unloading transients from 4.5A to 11.5A. Output capacitor voltage 100mV/div, inductor current 5A/div, time scale 500μs/div. .................................................................48

Fig. 2.15  Experimental results showing the auxiliary capacitor voltage reset procedure that follows an unloading transient. Signals from top to bottom: \( v_{\text{aux}} \) (500mV/div), \( v_{\text{out}} \) (100mV/div, ac coupled) \( i_{\text{buck}} \) (5A/div), and load-step signal. Time scale is 50μs/div. ........................................................................................................49

Fig. 2.16  Experimental efficiency measurement of the hybrid-VRM for consecutive loading-unloading transients from 4.5A to 11.5A (see Fig. 2.14 for waveforms) with different load transients frequencies. ..........51

Fig. 3.1  On and off trajectories and the load-line of a boost converter loaded by a CCL. ..............................................52

Fig. 3.2  On and off trajectories and load-line (black) of a boost converter loaded by a RL and the CCL load-line from Fig. 3.1 (green). ........................................................................................................53

Fig. 3.3  Illustration of typical region-of-convergence for boost converter loaded by a (a) resistive load, (b) constant current load. ........................................................................................................54

Fig. 3.4  The ROC for a boost converter loaded by an unknown load type. Green – CCL stability boundaries, black – RL stability boundaries. ........................................................................................................56

Fig. 3.5  Input and output power on the boost converter loaded by a RL state-plane. ..................................................59

Fig. 3.6  Simulated boost converter loaded by a RL loading transient from \( I_{\text{out,new}} = 0.55 \text{A} \) to \( I_{\text{out,new}} = 4 \text{A} \). (a) \( \lambda_{RL} = 0.5\lambda_{RL,max} < \lambda_{RL,max} \), switching surface is above the load-line (bottom – green) and under the stability bound (bottom – magenta), i.e. within the ROC, and the state variables converge to the new steady-state operating point \( (V_{\text{ref}},I_{\text{ref}}) \). (b) \( \lambda_{RL} = 1.07\lambda_{RL,max} > \lambda_{RL,max} \), switching surface is outside the ROC, and the state variables diverge from the new steady-state operating point \( (V_{\text{ref}},I_{\text{ref}}) \). (c) programmable-deviation control: The controller keeps the state variables within the ROC and they converge to the new steady-state operating point \( (V_{\text{ref}},I_{\text{ref}}) \). Top – inductor current, middle – output voltage, bottom – state-plane of inductor current and capacitor voltage. .................................................................61

Fig. 3.7  Illustration of the time response dependency on the geometric location of the controller on the state-plane. ........................................................................................................62

October 2015
Fig. 3.8  Second order IET converters: (a) Non-inverting buck-boost converter. (b) Buck-boost converter. (c) Flyback converter. .......................................................................................................................... 63

Fig. 3.9  Boost converter represented with transformed parameters and state variables of other indirect energy transfer converters. .......................................................................................................................... 63

Fig. 3.10 System’s response to a 0.5A to 2.4A loading transient: (a) using a programmable-deviation controller with boundaries maintaining the converter’s states within the ROC. (b) using a programmable-deviation controller with boundaries maintaining the converter’s states within the stability region, followed by steady-state PCMC controller to achieve zero-error state. (c) using a controller settings below the load-line that cannot maintain the converter’s states within the ROC. (d) using a programmable-deviation controller operating as time-optimal controller with boundary maintaining the converter’s states within the ROC. Time scale 20 µs/div. Inductor current (red) 2A/div [for (d) 2.5A/div], output voltage (blue) 0.5V/div AC coupled, and state-plane representation of inductor current and output voltage (bottom). 66

Fig. 4.1  MTDC hybrid controller regulating operation of a boost converter. .......................................................................................................................... 69

Fig. 4.2  Power representation on the state-plane of a boost converter loaded by a RL .......................................................................................................................... 70

Fig. 4.3  Desired movement of the state variables on the state-plane for a loading transient. .......................................................................................................................... 71

Fig. 4.4  Simulated response of the MTDC hybrid controller to a loading transient of a boost converter loaded by a RL. Output voltage (top - blue), inductor current (middle - red), and state-plane representation of the voltage and current (bottom). .......................................................................................................................... 71

Fig. 4.5  First on state trajectories and the load-lines intersections for CCL case (dotted) and RL case (solid)... 74

Fig. 4.6  Boost converter’s response to a 0.5A to 2.4A loading transient using the MTDC and time-optimal controllers: (a) MTDC controller with $V_{th} \approx V_{min}$ (b) MTDC controller with $V_{th} < V_{min}$ (c) time-optimal controller. Time scale 20µs/div, output voltage (0.5V/div, AC coupled, top - blue), inductor current [(a) 2A/div, (b) 2A/div, (c) 2.5A/div, middle - red], and state-plane representation of output voltage and inductor current. .......................................................................................................................... 75

Fig. 6.1  State-plane state trajectories of a buck converter. On state trajectories are in red, off state trajectories are in blue. .......................................................................................................................... 79

Fig. 6.2  State-plane state trajectories of a boost converter. On state trajectories are in red, off state trajectories are in blue. .......................................................................................................................... 80
Tables List

TABLE I. Experimental Prototype Values ................................................................. 45
TABLE II. Transformations of the System’s Parameters of Second Order Indirect Energy Transfer Converters .64
Acronyms and Abbreviations

ACMC – Average current-mode control
ADC – Analog-to-digital converter
AEP – Additional energy path
CCL – Constant current load
CMC – Current-mode control
DPWM – Digital pulse width modulation
EMI – Electromagnetic interference
ESR – Equivalent series resistance
FPGA – Field programmable gate array
GRSCC – Gyrator resonant switched-capacitor converter
HDL – Hardware description language
IC – Integrated circuit
IET – Indirect energy transfer
LDO – Low drop out
MOSFET – Metal oxide semiconductor field effect transistor
MTDC – Minimum-time within a deviation-constrained
PCMC – Peak current-mode control
PDM – Pulse density modulation
PI – Proportional-integral
PID – Proportional-integral-derivative
PWM – Pulse width modulation
RL – Resistive load
ROC – Region of convergence
SIC – Switched inductor converter
SCC – Switched-capacitor converter
SMC – Sliding-mode control
SMPS – Switched-mode power supply
TOC – Time-optimal control
VRM – Voltage regulator module
ZCS – Zero current switching

Inline References Legend

X.XX – Chapter / Section number
(X.XX) – Equation
[XX] – Reference
Fig. X.XX – Figure
1. Introduction

1.1. Overview of power converters

Power supplies and power converters are an essential part of practically every modern technological system, ranging from appliances to mobile phones, renewable energy sources and just about any grid-connected system. Power supplies are used to convert the electrical energy provided by an electrical source to another form of energy that is needed for proper operation of the system. Power supplies can be divided into two basic groups – linear regulators and switched-mode converters. Switched-mode converters are much more popular for processing power of more than few watts, and this chapter will mainly focus on them. The different converters’ topologies will be addressed, and a special emphasis will be given to the control methods of switched-mode converters.

1.1.1. Linear regulators

Linear regulators [4]-[9] have been widely used for decades in power supply systems, providing supplies for low-power applications. This kind of voltage regulator provides a simple low cost solution for voltage stabilization. Linear regulators are easy in design and implementation and have good precision of the output voltage value (in steady-state). They are built around an active element (such as a transistor), that acts as a variable resistor that together with the load forms a voltage divider.

An example of converting a DC voltage to a lower DC voltage level is the simple circuit shown in Fig. 1.1. The output voltage is $V_{out} = I_{load}R_{load}$, where the load current is controlled by the transistor represented by a variable resistor (see Fig. 1.1(a)). By adjusting the transistor’s base current, the output voltage is controlled to be over a range of 0 to $V_{in}$. The base current can be adjusted by control circuitry to compensate for variations in the supply voltage or the load, thus regulating the output. As can be seen from Fig. 1.1(a), the only current in the series element is the load current. Neglecting the power required for the circuit to control the series element, the efficiency of any regulator carrying out the process of power conversion, is defined as:

$$ \eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}}{V_{in}}, $$

(1.1)

where $P_{out}$ is the output power, $P_{in}$ is the input power, and the dissipated power $P_{loss}$ is defined as $P_{loss} = P_{in} - P_{out}$.
Introduction

As can be observed in (1.1), the efficiency depends on the output-to-input voltages ratio and not on the load current. This series transistor drives all the current demanded by the load and has to be designed to dissipate a significant amount of power, increasing the price, volume, and weight of the system. While this may be a simple method of converting a dc supply voltage to a lower dc voltage level and regulating the output, the low efficiency of this circuit is a serious drawback, especially for high-power applications. To overcome this issue, switched-mode converters are used.

1.1.2. Switched-mode converters

An efficient alternative to linear regulators are switched-mode converters [4]-[8]. These circuits employ solid-state devices that operate as electronics switches by being completely on (saturation) or completely off (cutoff).

The core concept of using a switch to create a dc voltage is described by Fig. 1.2(a). Assuming the switch is ideal, the output is the same as the input when the switch is on, and the output is zero when the switch is off. Periodic opening and closing of the switch results in the pulse output shown in Fig. 1.2(b).

![Fig. 1.2](image)

**Fig. 1.2** Basic dc-dc switching converter: (a) Equivalent switching circuit (b) Output voltage.

The average (dc) component of the output voltage is:

\[
V_{out} = \frac{1}{T_s} \int_{0}^{T_s} V_{out}(t) dt = \frac{1}{T_s} \int_{0}^{T_s} V_{in} dt = \frac{t_{on}}{T_s} V_{in} = DV_{in}
\]  

(1.2)
where \( D = \frac{t_{on}}{T_s} \), \( t_{on} \) is the time the switch is on, and \( T_s \) is the switching period. The dc component of the output voltage is controlled by adjusting the duty ratio, \( D \), and will be less than or equal to the input voltage for this circuit.

Switched-mode converters aim to use high-frequency switching in order to reduce the component size. In its simplest form, a reactive element is switched in between the input and the output, charging and discharging it with energy. The reactive element can be either an inductor, capacitor or both. The fundamental topologies from which variety of converters are derived are buck (step-down), boost (step-up), and buck-boost (step-up or down). These topologies can be classified into two groups - direct energy transfer converters and IET converters, and further details regarding these groups will be given in the following subsections.

Controlling the dc component of a pulse output of the type in Fig. 1.2(b) may be sufficient for some applications, but typically the objective of switched-mode converters is to produce an output that is a pure dc. One way of obtaining a dc output from a circuit of the type in Fig. 1.2(a) is using a buck converter, which inserts a low pass filter, built of an inductor and capacitor, after the transistor, as depicted in Fig. 1.3. When the transistor is on, the diode is reverse biased, the inductor is charging from the input voltage while the free-wheeling diode provides a path for the inductor discharging current to the load when the transistor is off. The diode naturally conducts as the input is disconnected due to the current continuity demand of the inductor.

![Fig. 1.3](image)

(a) Buck dc-dc converter, (b) Typical current and voltage waveforms of an ideal converter.
Introduction

DC-DC converters can also create an output voltage that is higher than the input voltage, as in the case of boost converter (see Fig. 1.4(a)), and can also create an output voltage that is either higher or lower and with different polarity, as in the case of buck-boost converter (see Fig. 1.4(b)).

\[ V_{in} \quad L \quad M_1 \quad D_1 \quad v_C \quad C \quad i_{out} \quad v_{out} \quad \text{Load} \]

(a)

\[ V_{in} \quad L \quad M_1 \quad D_1 \quad v_C \quad C \quad i_{out} \quad v_{out} \quad \text{Load} \]

(b)

Fig. 1.4 (a) Boost converter, (b) Buck-boost converter.

1.1.3. Direct energy transfer topologies

As mentioned in the previous subsection, switched-mode converters can be classified into direct energy transfer converters and IET converters. The direct conversion is achieved when the conversion is accomplished without an energy storage stage, i.e. there is a direct energy path from the input to the output of the converter [10].

Two commonly used direct energy transfer converters are the buck and forward topologies, shown in Fig. 1.5. The forward converter is a derivation of the buck converter by an addition of isolation using a transformer, and therefore has another degree of freedom for setting the desired output voltage, as the turns ratio of the transformer is dictating the conversion ratio. In a buck converter, during the on time, the input provides energy to the output and there is a direct energy path from the input to the output with an inductor between them [4], [11]. This feature of direct energy transfer provides the ability to rapidly overcome load current perturbations without compromising the output capacitor, as will be discussed in the following subsections.

\[ V_{in} \quad M_1 \quad L \quad v_{out} \quad \text{Load} \]

(a)

\[ V_{in} \quad \Sigma D_1 \quad L \quad v_{out} \quad \text{Load} \]

(b)

Fig. 1.5 Direct energy transfer converters: (a) buck, (b) forward.
1.1.4. Indirect energy transfer topologies

In contrast to direct energy transfer converters, in IET converters there is no direct energy path from the input to the output. The energy transfer is carried out by using one or more stages to temporarily store energy and then release this energy to the output. Commonly used IET topologies are boost, buck-boost, noninverting buck-boost and flyback, and are depicted in Fig. 1.6.

![Indirect energy transfer converters: (a) Boost, (b) Buck-boost, (c) Noninverting buck-boost, (d) Flyback.](image)

For example, in the buck-boost topology, during the on time, the inductor is charged from the input and since the output is disconnected from the input, the load current is supplied only from the output capacitor. Only during the off time the inductor is disconnected from the input and connected to the output, releasing its stored energy to the output.

When deriving the small-signal transfer functions of IET converters, it is found that they have a right half plane (RHP) zero [4]. This RHP zero is responsible for two major drawbacks of these converters: 1) the control loop bandwidth is limited, 2) there is a trade-off between output voltage deviation and total transient time when handling a load transient.

A special emphasis in this thesis is given to IET converters due their poor load transient response which significantly increases the volume of these converters. As will be detailed in the following sections, advanced control methods can significantly reduce the overall volume of these converters.

1.1.5. Switched-capacitor converters

A switched-capacitor converter (SCC) uses the principle of voltage potential leveling to create a desired dc voltage. In its most simplistic version, shown in Fig. 1.7, a flying
Introduction

capacitor \( (C_1) \) is alternated in between the input and the output and transfers charge from the higher to the lower potential, aiming to level the potentials.

\[
\begin{align*}
M_1 & \quad V_{in} \quad \text{Load} \\
C_1 & \quad v_{in} \quad i_{out} \\
M_2 & \quad v_{c+} \quad C_{out} \\
\downarrow & \quad v_{c-} \quad \text{Load}
\end{align*}
\]

Fig. 1.7 Basic 1st order switched-capacitor converter.

Many variations of the SCC exist that are able to provide multiple output levels by manipulating multiple flying capacitors, alternating between parallel, series, or mixed parallel-series connections. All of these variations have optimal efficiency at their natural discrete conversion ratios (1:1, 2:1, etc.). When the conversion ratio is not one of the topology dictated discrete values, losses must be added to achieve the desired output voltage, reducing the efficiency.

To reduce the required size of the flying and output capacitors, switching frequency is raised to a high level, creating multiple charges and discharges. However, increasing the switching frequency also increases the switching losses, since SCCs are operating with hard switching [12]. To overcome the losses caused by the hard switching, resonant switched-capacitor converters were developed, enabling soft switching and therefore reducing the switching losses.

1.1.6. Resonant switched-capacitor converters

In order to reduce the switching losses, operating in a resonant mode has been suggested. Adding an inductive element in series with the flying capacitor, as shown in Fig. 1.8, changes the charge and discharge profiles from an exponent to a 2nd order profile. Switching at exact half-resonance period, when the current crosses a zero value, creates a sinusoidal shaped current and switching can occur at zero current, namely zero current switching (ZCS), eliminating the switching losses. This feature enables the operation in high switching frequency, further reducing the components’ size.

\[
\begin{align*}
M_1 & \quad V_{in} \quad \text{Load} \\
C & \quad v_{c+} \quad i_{out} \\
M_2 & \quad v_{c-} \quad C_{out} \\
\downarrow & \quad L \quad \text{Load}
\end{align*}
\]

Fig. 1.8 A basic resonant (2nd order) switched-capacitor converter.
Introduction

A major drawback of soft switched SCCs is their inability to create an output voltage that is different from its natural target voltage (1:1, 2:1, etc.). In soft switched SCC, the resultant charge-balance of the flying capacitor differs from zero after a charge/discharge cycle when $V_2 \neq V_1$. The residual charge left in the flying capacitor impacts the average current and causes it to diverge, which, in turn, eventually increases/decreases the output voltage such that the charge-balance of the capacitor will be satisfied. To better view this problem, consider a generic 1:1 resonant SCC (see Fig. 1.8) with a desired output voltage of $V_2 < V_1$. The flying capacitor voltage and current are illustrated in Fig. 1.9. The current waveform shows that although ZCS is obtained, the charge delivered from the source is not equal to the one delivered to the output. This translates into an unbalanced capacitor voltage that continues to rise every cycle.

![Fig. 1.9](image)

**Fig. 1.9** Typical waveforms of the flying capacitor in the resonant SCC described in Fig. 1.8: dotted line - $I_c$, solid line - $V_C$, flat step - average $I_2$ corresponding to each switching cycle.

To overcome this drawback of soft switched SCCs, a new resonant SCC has been introduced and is discussed in the following subsection.

**1.1.7. Gyrator resonant switched-capacitor converter [13]**

This subsection presents a recently developed resonant switched-capacitor based converter. In contrast to traditional SCCs (either resonant or regular), the new converter disengages the efficiency of the system from the voltage gain. The converter operates as a gyrator, a voltage-dependent current source, namely gyrator resonant switched-capacitor converter (GRSCC). The GRSCC maintains soft switching for the entire operation range, and exhibits bi-directional power flow with wide voltage gains.

The topology in its generic form, as depicted in Fig. 1.10, requires bi-directional switches ($Q_1$, $Q_2$ and $Q_3$) that operate in synchronous/complementary action. This is required to support bi-directional and non-inverting step-up/down operations in a single configuration.
Introduction

However, for more specific cases, such as unidirectional power flow and/or specific conversion types (up or down), the number of switches and the configuration complexity can be significantly reduced.

1.1.7.1. Principle of operation

The operation of the GRSCC, shown in Fig. 1.10, is described for one steady-state charge/discharge/balance cycle and is assisted by Fig. 1.11 that illustrates the capacitor voltage, $V_C$, and the resonant tank current, $I_C$, for the case of a non-unity step-up conversion. The resistors $R_S$ in Fig. 1.10 represent the parasitic resistances in each loop and are assumed to be negligibly small in the analysis for the current and voltage conversion ratios.

By turning $Q_1$ on, a charge state (S1) is initiated, which charges the flying capacitor from the input $V_1$ in a resonant manner. At zero current, $Q_1$ is turned off and $Q_2$ is turned on (state S2) and at this point the flying capacitor discharges to the output. Since the input voltage $V_1$ and the output voltage $V_2$ have different values, only a portion of the charge is delivered to the output and results in $V_C$ that is different to its voltage at the starting point of S1. This voltage difference (neglecting parasitics) equals to twice the residual voltage of the flying capacitor. By turning $Q_3$ on (S3), the resonant tank is short-circuited. This creates the required charge-balance and reverses the flying capacitor voltage polarity such that the voltage at the end of S3 equals the voltage at the beginning of S1.
The drawback of resonant SCCs as described in section 1.1.6 is eliminated by the addition of the 3rd balancing state that causes charge balance of the capacitor. This charge-balancing state transforms this resonant SCC into a voltage-dependent current sourcing converter that, neglecting losses, is capable of accommodating any input to output voltage gain (below and above unity).
Voltage regulation may be applied by introducing a time delay between switching states, applying a delay between consecutive sequences, i.e. pulse density modulation (PDM), or by creating packets using on-off burst mode control [14], [15].

The topology of Fig. 1.10 may be extended to operate in naturally doubling and dividing configurations, i.e. shifting the peak efficiency points to \( A=2 \) or \( A=0.5 \), respectively. An attractive option that has voltage doubling properties may also be implemented as a bridge configuration as in Fig. 1.12. For the bridge configuration, the four-quadrant switches can be replaced by conventional MOSFETs, while retaining the converter characteristics.

![Fig. 1.12](image)

**Fig. 1.12** A GRSCC realized in a bridge configuration, with optimized efficiency at voltage gain of \( A=2 \) (or \( A=0.5 \), depend on the power flow direction).

### 1.1.8. DC-DC converter components design

Design of converter’s components is a critical stage in the design of switched-mode power supplies. The components selection has a crucial impact on the converter’s efficiency, size and cost [16]. Each application of power converter has its own specifications to handle. For example, in some VRM applications, the output voltage must be no more than ±3% away from the reference voltage, whereas in DC bus applications this tolerance can is much higher. This variety of applications specs require the design of the converter’s components to be optimized specifically for each application and specifications. This subsection discusses the design of the passive components of a converter, i.e. the inductor and capacitor, and addresses the physical size and volume of the components.

The inductor selection is usually based on selecting the current ripple in the inductor so it will be small compared to the nominal current. To balance between the different power losses that are related to the inductor (core loss and copper loss) and the required inductance, the inductor current ripple is typically designed to be around 20% of the nominal inductor current [4]. For example, for a 12V to 1.5V buck converter with nominal current of 20A operating at 500kHz, the inductor current ripple would be
Introduction

\[ \Delta I = \frac{V_{in} - V_{out}}{L} t_{on} = \frac{V_{in} - V_{out}}{L} \frac{D_{on}}{f_s} = \frac{V_{in} (V_{in} - V_{out})}{LV_{out} f_s}, \] (1.3)

which means that for \( \Delta I = 20 \times 0.2 = 4A \) the inductance value should be

\[ L = \frac{V_{in} (V_{in} - V_{out})}{\Delta IV_{out} f_s} = \frac{12 (12 - 1.5)}{4 \cdot 1.5 \cdot 500} = 0.42 \mu H. \] (1.4)

Apart from the inductance value, the selection of the proper magnetic element (size and core type) for the inductor should be selected according to product of the effective magnetic area \( A_e \) and the window area \( A_w \), that is

\[ A_p = A_e A_w. \] (1.5)

The resultant area of product \( A_p \) is given by

\[ A_p = \frac{LI_{pk} I_{RMS}}{JKB_{max}}, \] (1.6)

where \( L \) is the desirable inductance value, \( I_{pk} \) is the peak current that flows through the inductor, \( I_{RMS} \) is the maximal RMS value of the inductor current, \( J \) is the current density (typically 4-4.5A/mm²), \( K \) is the fill factor (typically 0.4-0.6) and \( B_{max} \) is the maximal flux density [4].

From the result in (1.6), the physical size of an inductor with given constraints (\( J, K \) and \( B_{max} \)) is determined by three parameters: the inductance value, the peak current and the RMS current. Therefore, by reducing each of these values, the size of the inductor is proportionally reduced.

Selection of the output capacitor of a converter is based on the maximal allowed output voltage deviation. In steady-state operation, when the load is constant, the capacitor value determines the output voltage ripple (neglecting the capacitor’s equivalent series resistance). However, in many applications the load current changes almost instantaneously, and the instantaneous current is flowing from the capacitor, discharging it and therefore changing its voltage. The voltage overshoot and undershoot depend on variety of things: the capacitance value, the control method, the inductor, the conversion ratio, the output voltage and some others as well.

To properly understand the selection procedure of the output capacitor, a 12V to 1.5V buck converter with nominal current of 20A operating at 500KHz with the inductor as in (1.4) is assumed, with a maximal allowed output voltage deviation of 50mV. The considered
load current change is from no-load to full-load (and vice versa), i.e. from 0A to 20A and from 20A to 0A. The control method for the converter is hybrid control (see subsection 1.3.4.1) built of steady-state PID controller and transient-mode time-optimal controller (see subsection 1.3.4.2).

For a loading transient from 0A to 20A, i.e. $\Delta I_{\text{out}} = 20A$, the voltage undershoot will be

$$\Delta V_{\text{loading}} = \frac{L \Delta I^2_{\text{out}}}{2C_{\text{out}} (V_{\text{in}} - V_{\text{out}})} ,$$

(1.7)

whereas for an unloading transient the voltage overshoot will be

$$\Delta V_{\text{unloading}} = \frac{L \Delta I^2_{\text{out}}}{2C_{\text{out}} V_{\text{out}}} .$$

(1.8)

Due to the difference in the applied voltage magnitude on the inductor between a loading transient and an unloading transient ($V_{\text{in}} - V_{\text{out}}$ compared to $-V_{\text{out}}$) for the designed buck converter, the voltage overshoot will be much greater than the voltage undershoot, i.e.

$$\Delta V_{\text{unloading}} > \Delta V_{\text{loading}} .$$

(1.9)

Therefore, the capacitor should be selected according to the worst case, the unloading case:

$$C_{\text{out}} = \frac{L \Delta I^2_{\text{out}}}{2V_{\text{out}} \Delta V} = \frac{0.42 \mu \cdot 20^2}{2 \cdot 1.5 \cdot 50m} = 1120 \mu F .$$

(1.10)

In terms of physical size of the capacitor, it is proportional to the stored energy in it, i.e. proportional to $CV^2$, where $V$ is the maximal voltage rating of the capacitor and $C$ is the capacitance value. Therefore, by reducing the capacitance value, its physical size is proportionally reduced as well.

This thesis aims to reduce the volume of switched-mode converters, and as will be demonstrated in the next chapters, a significant volume reduction can be achieved by applying advanced control methods or by some topologies modifications. There, reduction of the output voltage deviation and peak inductor current is achieved, reducing the overall volume of the capacitor and the inductor as detailed in this subsection.

1.2. State-space representation of switched-mode converters

Analyzing a switched-mode converter in the state-space can be a powerful tool for power electronics engineers. The state-space reveals the state trajectories and in many cases shows
Introduction

properties that are hard or even impossible to notice when analyzing a converter in the time-domain. The state-space representation is mainly used for designing controllers and in particular nonlinear controllers, study the large-signal properties of the converter and, as detailed in Chapter 3, to examine the stability of control methods.

Neglecting nonlinearities introduced by transformers or solid-state devices, in the case of a steady-state operation, a switched-mode converter’s linear small-signal model can be used to analyze its behavior. Therefore, it is easy to examine the converter’s characteristics by using any method related to the theory of linear circuits [17]. However, in transient operation, the linear small-signal model is no longer valid since a switched-mode converter becomes nonlinear, and analyzing it using linear methods becomes inaccurate. Transient response can be better analyzed using the state-space representation, which refers to system’s characterization and dynamic properties and can be applied to nonlinear systems. The analysis is aided by the state trajectories, described upon an appropriate state-space, which its coordinates are the system’s state variables. Nowadays, more and more applications mostly operate in the transient operation, and consequently the state-space representation is extensively used and studied in “modern” control methods [18], [19].

Moreover, instead of the conventional representation in terms of frequency response and transfer functions, the state-space representation is an excellent alternative way to describe the system’s model. There are several advantages for using the state-space representation when compared to the transfer function method, here are some of them:

1. State-space representation and analysis can be applied to nonlinear systems.
2. It can be applied to time invariant systems.
3. A more compact set of equations.
4. It is an effective option for the visualization of the system’s characteristics.
5. It enables an examination of the system’s behavior under different control strategies, including nonlinear control methods.
6. It can be easily applied to systems with multiple inputs and multiple outputs.
7. In contrast to a transfer function, which is defined only under zero state initial conditions, it is possible and easy to incorporate the effect of initial conditions in the solution.

The state-space is considered as a working region that describes the system and its operation, by states defined appropriately on the state-space. The state-space axes are defined as state variables, and the state of the system can be represented as a vector within
that space. Most common dc-dc converters contains one inductor and one capacitor, and therefore for these cases the order of the system is 2. The state-space is now the state-plane, where its horizontal axis is the capacitor voltage and the vertical axis is the inductor current.

The information gained through an examination of the state-plane state trajectories has led to the development of a new control methods such as the minimum-deviation control law for dc-dc converters [18], [19] and the control method that is presented in Chapter 4. This could provide a significant improvement in the system’s performance and characteristics.

1.2.1. State variables

State variables shall only be those variables that cannot change their values instantaneously. Such variables are all those who appear in mathematical expressions for energy, for example current in the expression of the inductor’s stored energy $Li^2/2$. Thus obvious candidates for state variables in a dc-dc converter are the inductor current and its capacitor voltage. Very often they can be expressed in terms of differential equations of the state variables, namely, state equations.

1.2.2. State equations of switched-mode converters

A switched-mode converter is a system with two possible operation states: when the switch is on and when the switch is off. Therefore, the number of state equations would be two times the number of the state variables, i.e. one set of two equations for the on state and one set of two equations for the off state. By using this approach, the construction of the state equations is straightforward. The converter is analyzed as two different linear circuits and the state equations for each of the circuits can be easily derived [20], [21].

An example of deriving the state equations is given for a buck converter loaded by a constant current load. First, the buck is separated into two different linear circuits for the on state and for the off state, as presented in Fig. 1.13.

![Buck converter circuit](image)

Fig. 1.13   Buck converter circuit for (a) on state (b) off state.

Then, the differential equations for the state variables are extracted by solving the two circuits, for the on state:
1.2.3. State trajectories construction

State trajectories are the natural state variables movement trajectories on the state-plane. Although the movement along the trajectories correlates to the change of the state variables with respect to time, the time parameter is implicit, i.e. the speed of movement cannot be determined from the trajectory itself.

The state trajectories construction is done by using the state equations for each of the two states. To write the trajectories expressions, it is first needed to find one state variable as a function of the other state variable, i.e.

\[ g(v_C, i_L, v_C, i_L) = 0, \quad (1.13) \]

where \( v_C \) and \( i_L \) are different initial conditions for the capacitor voltage and inductor current, and then it can be drawn in the state-plane \( v_C - i_L \). Since the time parameter is implicit in state-space representation, it is not mandatory to fully solve the differential equations and find the state variables with respect to time.

There are three main methods for drawing the state trajectories [22]:

1. Isoclines method - Finding the slope of the trajectories and substituting different points in the state-plane. The slope can be found by the expression

\[ m(v_C, i_L) = \frac{dL}{dv_C} = \frac{f_2(v_C, i_L)}{f_1(v_C, i_L)}, \quad (1.14) \]

It should be noted that this method is always applicable and can be used for every system.

2. Finding the exact expression (1.13), this can be done by solving the integral

\[ \int f_1(v_C, i_L)di_L = \int f_2(v_C, i_L)dv_C. \quad (1.15) \]

3. Finding each of the state variables expression with respect to time and then substitute the two equations to eliminate the time parameter.

A detailed example of deriving the state trajectories for buck and boost converters is given in the Appendix.
1.3. Control of switched-mode converters

The objective of most switched-mode converters is to create a desired dc output voltage, but due to non-idealities of the converters (e.g. parasitic resistances, diode forward voltage, changes of the input voltage, temperature), it is impossible to maintain a specific output voltage. To overcome this issue, a switched-mode converter must use a controller that senses the output voltage and adjusts its operation so that the output voltage will be the desired one. A switched-mode converter with a control loop for its output voltage is called a switched-mode power supply (SMPS).

There are various analog and digital control methods used for dc-dc converters and some have been adopted by the industry, including voltage-mode and current-mode control techniques. The dc-dc converter inputs are generally unregulated dc voltages and the required output should be a fixed voltage, irrespective of variations in load current or input voltage. Today, due to the advancement in power electronics and modern technology, the requirement for accurate and reliable voltage regulation has been raised [23]. This has led to the need for a more advanced and reliable design of controllers for converters. There are various types of dc-dc converters required for particular purposes like buck, boost, buck-boost and others. All of these converters have their specific configurations to complete their tasks. Varieties in dc-dc converters require different types of controlling techniques because a single technique cannot be applied to all converters due to different specifications for each one of them.

This section overviews the control methods used to facilitate the required performance for various kinds of dc-dc converters. A special emphasis is given to modern nonlinear control methods for IET converters that are defined on the state-space.

1.3.1. Linear control methods

1.3.1.1. Voltage-mode control

Voltage-mode control (VMC) is a control technique used in many power systems where the duty cycle is adjusted to regulate the output voltage, based on the value of the error between the sensed output voltage and the reference voltage [4]. Steady-state is achieved when the actual output voltage equals the voltage reference.

A generalized structure of voltage-mode control loop contains three main stages and is depicted in Fig. 1.14. These three stages are the power stage, the modulator, and the voltage
Introduction

loop compensation network that ideally allows the highest possible bandwidth that maintains the stability. The voltage loop compensation includes calculating the voltage error $v_e$ by comparing the voltage at the feedback to the reference voltage and then using an error amplifier to create a correction signal $v_c$. This signal enters a modulator and a PWM signal is generated with the compensated duty ratio. To properly understand each of the control loop stages, a voltage-mode controlled buck converter is depicted in Fig. 1.15.

![Fig. 1.14 Typical structure of voltage-mode controlled power stage.](image)

![Fig. 1.15 Buck converter controlled by a voltage-mode controller with a PI compensation network.](image)

Design of VMCs is based on the small-signal control-to-output transfer function of the converter so that the output voltage will track the reference voltage. The design aim is to produce the highest loop bandwidth possible, only limited by the switching frequency [4], where common compensators are proportional-integral (PI) and proportional-integral-derivative (PID). Although traditionally the design consideration is to track the reference voltage, in most applications the reference voltage is fixed, and the controller should handle changes in the load current or in the input voltage.
1.3.1.2. Current-mode control

Current-mode control (CMC) has been a popular and effective control technique for switched-mode converters [24]. It is based on sensing both the output voltage and the inductor current, where there are two control loops: inner loop for the inductor current and outer loop for the output voltage [25]. The current loop is a fast loop with a high bandwidth that equals the switching frequency. The voltage loop is much slower than the current loop, and its output determines the reference $v_e$ for the current loop, as depicted in Fig. 1.16.

![Current-mode control schematic of a synchronous buck converter.](image)

The current loop turns the inductor into a voltage-controlled current source, effectively removing the inductor from the outer voltage control loop transfer function at dc and low frequencies. The inner loop uses a PWM modulator which receives the sensed inductor current ramp, and a reference current obtained by the outer voltage loop to determine the switch control signal.

A significant difference between VMC and CMC is the PWM signal generation. For VMC a fixed external ramp is used, while for CMC the inductor current own ramp is used. CMC schemes have several advantages to offer over VMC. Since in CMC the inductor behaves as a current source, voltage variation at the input side doesn’t go through to the output, what makes the CMC more immune to an input disturbances compared to a VMC [4]. Also, the CMC control-to-output transfer function can be simplified to a first order system, compared to second order for the case of VMC, and therefore converters with CMC have simpler dynamics and system stabilization is easier to obtain. CMC is implemented mostly with two approaches: 1) Peak current-mode control (PCMC), 2) Average current-mode control (ACMC).

PCMC is a very popular control method and will be presented in the following subsection.
1.3.1.3. Peak current-mode control

Among the different ways to implement CMC, peak current-mode control (PCMC) is probably the earliest and simplest approach. A block diagram of a PCMC power converter is presented in Fig. 1.17. The inner current loop senses the inductor current and directly compare it to the reference current $i_{ref}$ using a comparator to monitor and maintain the peak inductor current equal to $i_{ref}$, as depicted in Fig. 1.18. The voltage loop compensator sets $i_{ref}$ based on the voltage error between the output voltage and the reference voltage $V_{ref}$. It should be noted that for conversion ratio that requires a duty ratio higher than 0.5, sub harmonic oscillations occur [4]. These oscillations can be solved by the addition of slope compensation for $i_{ref}$. A big advantage of PCMC is that it provides inherent over-current protection due to the immediate current limit by the comparator.

![Block diagram of a PCMC power converter](image1)

Fig. 1.17 Peak current-mode control of a synchronous buck converter.

![Typical waveforms of peak current-mode controlled converter](image2)

Fig. 1.18 Typical waveforms of peak current-mode controlled converter.
1.3.2. Digital control of switched-mode converters

In recent years, the interest in digital control for switched-mode converters has grown considerably [26]. The digital control approach potentially offers several advantages compared to the analog counterpart, such as the immunity to component variation, the ability to perform sophisticated control algorithm, self-calibrations, faster IC design using HDL synthesis and controller adaptation. In spite of these potential advantages, one of the limiting factors when using IC digital controller in high-frequency SMPS is the hard to achieve dynamic performance that is comparable to those of the analog controllers, especially in the presence of significant control delays and quantization effect. Thus, one of the major challenges in digital control for SMPS is the development of simple digital or mixed-signal control architectures with small additional silicon area required which ensures dynamic performances comparable to analog controllers. Such a controller usually requires high-resolution analog-to-digital converter (ADC) and digital-pulse-width modulator (DPWM), as shown in Fig. 1.19. The IC implementation of such a control is usually complex. It is also hampered by the undesirable quantization effect and limit cycle oscillations [27]-[28].

![Digital control block diagram](image)

**Fig. 1.19** Digitally controlled SMPS.

1.3.3. Nonlinear control methods

The switching action is an inherent property of switched-mode converter systems. In a mathematical sense such systems are discontinuous and thus nonlinear. Unfortunately it is this nonlinearity that, at the same time, represents both the main problem in circuit analysis as well as the bedrock for successful circuit design.

Conventional converter analysis approaches have therefore often tried to suppress the nonlinear characteristics. Techniques such as averaging and linearization have been widely used [4]. The resulting loss in information is significant; not only does the issue of ripple get
Introduction

neglected in these approaches, but also most of the ensuing mathematical models solely apply to the converters’ behavior.

This subsection will review two nonlinear control methods: sliding-mode control (SMC) and boundary control. These nonlinear control methods are suitable for switched-mode converters due to their inherent switching behavior.

1.3.3.1. Sliding-mode control

Most state of the art SMPS controllers are designed by using a state-space averaging method, which is essentially a small-signal approximation [4],[29]. Although this procedure works well for steady-state operation, it has mediocre performance while handling load transients. Most switched-mode converters operate in one of two structural modes: when the switch is on and when the switch is off. Due to the nonlinear nature of the switching operation used in the design of these regulators, they are classified as variable structure systems. SMC is a nonlinear control method that is suitable for variable structure systems and therefore it is a natural fit to utilize them in SMPSs [30].

Fundamental principle of the controller is to employ a certain sliding surface $\sigma(v_c,i_L)=0$ (typically defined in the state-space) as a reference path such that the controlled state variables can be directed toward a desired equilibrium point. Implementation of a sliding surface as a stabilizing reference path can be fully achieved by meeting the following three conditions [22]:

1. **Reachability condition**: the trajectories must reach the sliding surface for arbitrary initial conditions;
2. **Existence condition**: the state trajectories are directed toward the sliding surface when they are close to it;
3. **Stability condition**: the sliding surface will always direct the state trajectories toward a stable equilibrium point.

The principle of operation for SMC is to define a sliding (switching) surface that defines the control law for the converter, if the form of:

$$\begin{align*}
\sigma > 0, & \rightarrow \text{off} \\
\sigma < 0, & \rightarrow \text{on}
\end{align*}$$

To avoid switching in an infinite frequency along the switching surface, a hysteresis band is added. The hysteresis band width is $2\Delta$, where $\Delta$ is a small parameter. Within this definition of the control law, the reachability and existence conditions can written as
Introduction

\[
\frac{d\sigma}{dt} < 0 \quad \text{for } \sigma > 0 \quad (\text{off})
\]
\[
\frac{d\sigma}{dt} > 0 \quad \text{for } \sigma < 0 \quad (\text{on})
\]  \hspace{1cm} (1.17)

Fig. 1.20 shows typical SMC operation on the state-plane. As can be observed, the system starts at the initial condition \((v_{C0},i_{L0})\) and the control law determines that the state should now be the off state. The system state moves along the off state trajectory until it hits the switching surface \(\sigma\) where it changes to on state. From now on, the system state slides along the switching surface until it reaches the steady-state equilibrium point \((V_{ref},I_{ref})\).

![Sliding mode controller operation](image)

Fig. 1.20  Sliding-mode controller operation and the resultant controlled trajectories on the state-plane.

The system’s motion on the switching surface has an interesting geometric interpretation, as the “average” of the system’s dynamics on both sides of the surface and close to it. To analyze the system dynamics along the switching surface, the equivalent control \(u_{eq}\) can be used [22].

1.3.3.2. Boundary control

Boundary control is a geometric-based control method which defines a curve of the form \(\sigma = f(v_C,i_L) = 0\) on the state-plane called (switching) boundary. It is a generalization of well-known hysteretic type control methods such as voltage-mode hysteretic control and sliding-mode control. For converters with two possible switching states, a boundary defines when the converter is in on state and when it is in off state. Whenever the converter’s states are located on one side of the boundary, i.e. \(\sigma > 0\), the operation is governed by an on state, and whenever the states are located on the other side, i.e. \(\sigma < 0\), the operation is governed by an off state. Switching between the two states is made when the state trajectory crosses the boundary, thus, a boundary must pass through the desired steady-state operating point \((V_{ref},I_{ref})\) in order to be able to drive the converter to this point.
Points along the boundary can be classified to three types, according to how the on and off state trajectories behave when they cross the boundary, as depicted in Fig. 1.21:

a. Reflective: both on and off trajectories are directed toward the boundary.

b. Refractive: one state trajectory is directed toward the boundary and the other state trajectory is directed away from the boundary.

c. Rejective: both on and off state trajectories are directed away from the boundary.

![Fig. 1.21 Trajectories behavior at different boundary crossing points: (a) reflective point, (b) refractive point, (c) rejective point.](image)

The state-plane of a switched-mode converter can be separated to the three different regions, i.e. reflective, refractive and rejective, according to the properties of every point and the on and off state trajectories passing through it [31]. The lines separating these three regions are the load-line (see subsection 3.2 for further details) and the steady-state on and off state trajectories. As a consequence, the operation of a boundary controller can be classified to three modes as well, by the location of the boundary with respect to operation region. Operation in the reflective mode results in sliding-mode behavior, since the trajectories on both sides of the boundary are directed towards it. Once the state trajectory hits the boundary, the only movement possible is along the boundary. Operation in rejective mode results in movement away from the boundary, never crossing it again (all trajectories are pointed away from the boundary). Transitions between modes of operation are possible, but not all transitions exist if the system is large-signal stable. For example, operation in refractive mode can be followed be a reflective mode, but not the opposite.

A boundary controller is defined to be large-signal stable if it moves the converter’s state variables to the steady-state operating point and keeps them there, resulting in a state-error (voltage and current error) approaching zero, limited by the converter switching frequency.

### 1.3.4. Load transient oriented control methods

To minimize the size of reactive components, the controllers for SMPSs are often designed to have fast response to load transients and other disturbances, especially in the case of modern VRMs, where high current and low voltage are required at the output of the
SMPS. In low-to-medium power supplies, processing power from a fraction of watt to several hundreds of watts, where cost-effective implementation is of a key importance, analog controllers have been predominantly used [32]-[36]. There, a fast response is usually achieved by designing a wide bandwidth control loop. Recently emerged hardware-efficient digital controllers [37]-[43] enable the implementation of advanced nonlinear control methods for low-to-medium power systems, improving dynamic performance and, consequently, drastically reducing the size of the output capacitor. Among them, time-optimal [44]-[50], charge balance and minimum-deviation [18],[51] controllers have demonstrated transient response with virtually the smallest possible voltage deviation. These controllers are classified as hybrid controllers, due to their switching between multiple controllers depending on control objectives or operating conditions.

This subsection reviews the most recent load transient oriented controllers for SMPS.

1.3.4.1. Hybrid control

A Hybrid controller incorporates two or more control laws. The different control laws can be either different small-signal linear controllers, large-signal nonlinear controllers or a mixture of both. Switching between these control laws depends on the converter’s states, where the objective of switching between the controllers can be either to achieve faster dynamic response, lower voltage or current overshoots and undershoots, improving efficiency or any other control objective. For example, a hybrid controller such as in [44] can operate as a small-signal linear controller (e.g. PI, PID) when the converter’s states are within proximity of the steady-state operating point, and as time-optimal-like controller (see next subsection) for large-signal compensation when the converter’s states are away from the new steady-state operating point, in order to achieve the fastest possible dynamic response.

In a hybrid controller that combines large-signal and small-signal linear controllers, it is not a necessary condition for large-signal stability that the large-signal controller will decrease the state-error toward zero and will maintain it in this point. This is since the small-signal linear controller is in charge of keeping the converter’s states at the steady-state operating point, maintaining a zero state-error. The only condition for stability in such a hybrid controller is that the large-signal controller will move the converter’s states to the desired steady-state operating point. Thus, a hybrid controller large-signal stability exists if the large-signal compensator is capable of bringing the converter’s states from any initial condition to the steady-state operating point.
Introduction

1.3.4.2. Time-optimal control

Time-optimal control (TOC) has been widely studied in recent years [44]-[50]. It is a nonlinear control method that is designed to handle load transients with fastest possible response. The ideal TOC in the synchronous buck converter includes a single switch action, and its corresponding response including the state-plane trajectories are depicted in Fig. 1.22. The classical approaches for obtaining the ideal TOC based on Pontryagin’s minimum principle [52] are not practical in switched-mode converters, since: 1) the solution needs the exact dynamics of the system, which is usually not available; 2) the computations involved may be very complicated; and 3) TOC is sensitive to operating conditions, parameter tolerances, and parasitics. As a consequence, the time-optimal controllers still have not been widely adopted in the industry.

Fig. 1.22 Buck converter controlled by TOC response for a loading followed by an unloading transient. (a) Time response waveforms for inductor current and output voltage, (b) state-plane trajectories.

For direct energy transfer converters, the load transient response using TOC always results in the minimum possible output voltage deviation and, therefore, the minimum output capacitance value. However, for the IET converters such as boost that is not the case. There, as will be described in the Chapter 4, the time-optimal response produces a larger than the minimum output voltage deviation and an extra stress of the components.

1.3.4.3. Minimum-deviation control

The minimum-deviation control method has been introduced for buck converters in [51]. This hybrid control method has a bit different control objective than TOC. The objective is to minimize the components’ stress by reducing the peak inductor current and the output voltage deviation, while compromising the total transient time. For a loading transient, as in TOC, the inductor current is ramped up with the highest available slew rate. When the inductor current reaches the load current this is when the output voltage deviation is the highest, and from this point on the inductor peak current is limited and the output voltage slowly returns to its steady-state value, as shown in Fig. 1.23.
Introdu

1.3.4.4. Programmable-deviation control

A Programmable-deviation controller has been recently presented in [18]. The controller, schematically presented in Fig. 1.24, is designed to deal with loading and unloading transients of IET converters. It hybrids a conventional mixed-signal PCMC for steady-state voltage regulation and a boundary-type control law for the large-signal transient mode. For the operation of the boundary controller, two additional blocks were added, a transient suppression block and a self-tuning estimator. Upon a load transient detection, these blocks take over the task of creating the PWM signal from the conventional controller and provide transient response with voltage deviation as prescribed by the control objective. The transient suppression block implements a boundary-type control algorithm that dynamically changes the on and off transistor times, based on the information of the load current that is provided by the estimator. Once the transient recovery is completed the controller returns to steady-state operation.
Introduction

The controller recovers from a loading transient through a two-step process. Upon detection of a transient, during the first step, the transistor of the boost is turned on. Over this period, the controller estimates the new load current and accordingly, sets one switching boundary, i.e. threshold, for the inductor current $I_{th}$ such that it is slightly larger than the new steady-state value $I_{ref}$ (by $\varepsilon$), i.e.

$$I_{th} = I_{ref} + \varepsilon$$

(1.18)

where the value for $\varepsilon$ is used to limit the switching frequency.

![Diagram](image)

Fig. 1.25 Operation of the programmable-deviation controller in a boost converter for loading transient (maximum switching frequency is limited). Inductor and load current (top), output voltage (middle), and state-plane representation of the voltage and current (bottom).

Once the first current threshold has been reached (point ‘$a’$, Fig. 1.25), in the second step, the controller measures the output voltage and assigns two switching boundaries as $V_{ah} = v_{C,\text{point}}$ and $I_{th}=I_{ref}$. From this point and on, the transistor’s on time is governed by the voltage boundary and the off time by the current boundary. It should be noted that by assigning the boundaries as prescribed here, the controller operation depends on the quality of the load current estimator alone and is insensitive to any parameter variations or uncertainties. Within the context of this study, the transient action of the programmable-deviation controller can be defined by a boundary-type control where there are switching boundaries $\sigma_1$ for the off state ($I_{th}$) and $\sigma_2$ for the on state ($V_{ah}$), as demonstrated in Fig. 1.26, and have the expressions of the form:

$$\sigma_1 = I_L - I_{th}$$

where: $\sigma_1 < 0 \rightarrow \text{on}$

$\sigma_1 > 0 \rightarrow \text{off}$

$$\sigma_2 = v_C - V_{th}$$

where: $\sigma_2 < 0 \rightarrow \text{off}$

$\sigma_2 > 0 \rightarrow \text{on}$

(1.19)
Fig. 1.26 Programmable-deviation controller switching boundaries for (a) on state (b) off state.

As can be observed from Fig. 1.25, the minimum output voltage deviation point \((V_{\text{min}}, I_{\text{min}})\) is obtained where the first on state trajectory intersects the load-line. However, convergence to the steady-state operating point (point ‘o’) from this point would require operation at a very high switching frequency (theoretically infinite for the case when \(V_{th}\) is equal to \(V_{\text{min}}\)) and, as such, is not practical. Therefore, the switching frequency range is limited by the additional charging of \(\varepsilon I\) as depicted in Fig. 1.25. Moreover, the programmable-deviation controller can produce a time-optimal response as well, by selecting the specific \(\varepsilon I\) to obtain charge balance during a single on-off cycle. This makes the TOC a particular case of the programmable-deviation control, as demonstrated in Fig. 1.27. In this case, the boundary-type controller can be written as a single boundary expression:

\[
\sigma_{2,\text{TOC}} = V_C - V_C\big|_{\text{point 'o',TOC}}
\]

where: \(\sigma_2 < 0 \rightarrow \text{off}\)
\(\sigma_2 > 0 \rightarrow \text{on}\)  \hspace{1cm} (1.20)

Fig. 1.27 Time-optimal response of boost converter controlled by a programmable-deviation controller during a loading transient: inductor and load current (top), output voltage (middle), and state-plane representation of the voltage and current (bottom).

Section 3.3 delineates the region where stability of the programmable-deviation controller exists for the case of loading transients.
1.4. Topologies modifications and additional energy path (AEP)

As mentioned in the previous sections, to cope with fast load transients, multi-stage interleaved converters combined with analog controllers have been predominantly used [53]-[57]. There, fast response is usually achieved by designing a wide bandwidth control loop, requiring high switching frequency [4].

An alternative to the control methods presented above is to use an additional energy path (AEP) in order compensate the charge unbalance of the output capacitor, consequently reducing the transient time and output voltage deviation [58]-[80]. The impact on the energy transfer of the system with and without the AEP is illustrated in Fig. 1.28. During the steady-state operation in both cases, the energy is transferred from the source through the main converter to the load, as shown in Fig. 1.28(a) and Fig. 1.28(c) for the system without and with the AEP, respectively. Upon the load transient, in the case of the system without the AEP, the difference of energy demanded by the load and provided by the main power stage is compensated by stored energy in the output capacitor, as shown in Fig. 1.28(b). In this case, in order to reduce the output voltage deviation and the size of the output capacitor, aforementioned control methods can be employed. On the other hand, in the case of the system with the AEP, upon the same load transient and the same energy difference between the main converter and the load, only a small portion is extracted from the output capacitor, while the main part is provided through the AEP (Fig. 1.28(d)).
Introduction

By using this approach, during the steady-state operation the system with the AEP has high efficiency since the main converter is designed to operate at moderate switching frequency with relatively low-bandwidth control loop. This way the main converter is optimized to have minimum losses and to meet the static requirements, whereas the dynamic behavior during load transients is determined by the high-bandwidth AEP. The downside of the approach is that, during the load transients, the AEP is active and since it is optimized for fast dynamic response it generates additional losses. On the system level, depending on the load transient repetition rate, the overall efficiency can be improved. Due to these advantages of the system with AEP, this architecture has been selected as a focus of the investigation of this thesis and a new AEP solution is presented in Chapter 2. This Section reviews the difference approaches of implementing an AEP.

1.4.2. Beyond time-optimalilty

The approach of exceeding the physical limitations of the buck converter when handling load transient by using an AEP has been extensively studied [59]-[80]. To overcome the slew rate limitation of the inductor current to reach the load current, an AEP is used to transfer energy to the output from the input source in case of a loading transient and to transfer energy from the output to a resistor for an unloading transient. The solution in [60]-[69] used an AEP, but implemented a dissipative energy path using a linear regulator or a resistor, reducing the overall efficiency of the system. More advanced AEP solutions, connected at the input side and the output side are presented in the following subsections.

1.4.3. Input-side AEP

The input-side AEP solutions add an AEP built of an auxiliary circuit that is connected between the input source and the output, in parallel with the main converter as in [70]-[77], schematically presented in Fig. 1.29. The AEP can be either bidirectional or unidirectional, depend on the application. A bidirectional AEP acts as a fast auxiliary current source that can be implemented using an active region current injection circuit [70] or using a buck converter with small inductance [77]. Unidirectional solutions can be implemented using a small boost converter from the output to the input [75], [76]. These solutions usually handle only the unloading transient problem, since for high conversion ratio (which is usually the case for VRMs) the overshoot is much greater than the undershoot, as mention in [75] and in subsection 1.1.8.
Introduction

Fig. 1.29  Input-side auxiliary circuit as an AEP.

There are several drawbacks for using an input-side AEP. During a loading transient, the transient is reflected to the input since both converter and AEP are now trying to deliver power from the input to the output. This impacts the input capacitor filter of the converter, increasing its needed capacitance, and consequently dramatically increases its size since it is rated to relatively high voltage of the input (as detailed in subsection 1.1.8).

Another drawback of the input-side AEP is the usage of high voltage rating MOSFETs, which have higher on resistance $R_{DS(on)}$. Since the AEP must be faster than the main converter, its switching frequency is higher and due to the high voltage rating transistors the power loss due to conduction losses and switching losses is more significant.

To overcome these drawbacks, a load-side AEP has been presented, detailed in the following subsection.

1.4.4. Load-side AEP

Recent studies have reported improved loading and unloading transient performance, obtained by using an AEP auxiliary circuit that is connected to the load-side (output-side) [78]-[80], as shown in Fig. 1.30. There, an independent energy bank is used, eliminating the impact on the input. Moreover, the load-side voltage is low, and the required MOSFETs of the AEP are now smaller with lower $R_{DS(on)}$ and thus with lower power loss.

Fig. 1.30  Load-side auxiliary circuit as an AEP.

Although the solution requires additional sensors to regulate the auxiliary circuit’s operation and is limited by switching frequency to mid-range output voltages, it is a new concept to improve the performance of VRMs and therefore focused on this thesis (see Chapter 2).
Introduction

1.5. Motivation, objectives and significance of the research program

These days, switched-mode converters size and volume is dictated by their load transient response. Tighter output voltage regulation, faster response time to load changes and lower volume – the major concerns in the design of present-day SMPSs – are creating a ‘bottleneck’ in the advancement of the technology.

The primary objectives of this research program is to devise a new generation of highly flexible SMPSs for low to medium power applications, ranging from few watts to several hundred watts. Such flexible SMPSs would combine advanced digital control methods with novel converter topologies, thereby drastically minimizing the overall volume and improving power processing efficiency. It is expected that the combination of a converter configuration that can accommodate the load requirements and a controller that is specially ‘tailored’ to the converter’s characteristics will result in improved load transient response, lower device volume and lower cost of the converter.

More specifically, the objectives of the research program are:

1. To improve the load transient response of VRMs in order to reduce their overall volume and to improve their power processing efficiency.
2. To create a new framework and methodology for the examination of stability of controllers for IET converters.
3. To develop new control methods for IET converters that are specially designed to reduce the overall volume of these converters by producing fast load transient response without compromising the components’ size.
Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

2. Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

This chapter introduces a new VRM that hybrids a highly efficient switched-inductor converter as the main unit with a load-side AEP unit built of a switched-capacitor based converter to assist during load transient events. An overview of the topology is first presented, followed by an analysis of transient recovery by a load-side auxiliary circuit. Then, power processing analysis is provided for TOC and the new hybrid-VRM. The new controller operation is detailed and experimental results using a 20W, 12V-to-1.5V prototype are provided.

2.1. Overview

In recent years there has been a sharp rise in interest and demand for more compact, light, energy efficient and economical voltage regulation solutions. In particular, tighter output voltage regulation, faster response times and lower volume are of major concern in the design of present-day VRMs.

The objective of this chapter is to introduce a new compact VRM solution that hybrids a buck converter with a resonant switched-capacitor auxiliary circuit that is connected at the load side, as detailed in Fig. 2.1. By incorporating a new control concept, the auxiliary circuit effectively mimics increased capacitance during loading and unloading transient events, reducing the burden on both the input and output filters, and reduces the current stress. In addition, the presented hybrid-VRM requires indication from the output voltage alone, making this solution simple and cost-effective.

Fig. 2.1 Hybrid-VRM with load-side GRSCC auxiliary circuit. The area within the bottom box is implemented within an FPGA.
Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

The chapter is organized as follows: Section 2.2 describes the effect of different auxiliary current profiles on the transient recovery performance, Section 2.3 discusses the improvement in power processing efficiency. The implementation of the GRSCC as an auxiliary circuit is delineated in Section 2.4. Next, the details of the control scheme for the hybrid-VRM are given in Section 2.5. Experimental results and conclusions are then provided in Sections 2.6 and 2.7, respectively.

2.2. Transient recovery by a load-side auxiliary circuit

A key factor for assisting the recovery of the main converter from a load transient is the capability of the auxiliary circuit to rapidly sink or source the current mismatch between the new load state and the main inductor current. To analyze the required behavior and control mechanism of the auxiliary unit, an idealized bi-directional current source that is connected to the output terminals of the voltage regulator can be assumed as depicted in Fig. 2.2.

![Fig. 2.2](image)

Fig. 2.2 Simplified circuit with the auxiliary circuit modelled as a controlled current source, demonstrating the current relationships towards the load.

The analysis is aided by Fig. 2.3 which shows average waveforms for different sinking patterns of the current source to a current unloading step of $\Delta I_{\text{out}}$. It is further assumed that a time-optimal-like control is implemented for the main converter to maximally expedite the recovery phase.

![Fig. 2.3](image)

Fig. 2.3 Schematic response waveforms of the hybrid-VRM to an unloading step of $\Delta I_{\text{out}}$ for different auxiliary behaviour. (a) $I_{\text{aux}} = I_{\text{load}} - I_{\text{back}}$, (b) $I_{\text{aux}} = \Delta I_{\text{out}}/2$, (c) $I_{\text{aux}} > \Delta I_{\text{out}}/2$, segmented to match the overall charge $Q$. 

– 34 –

October 2015
Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

To eliminate any deviations of $v_{\text{out}}$ from the steady-state value, $V_{\text{out}}$, the auxiliary circuit is to mimic infinite capacitance, i.e. mirror the mismatch between $i_{\text{buck}}$ and $i_{\text{load}}$. As shown in Fig. 2.3(a), the auxiliary current, $i_{\text{aux}}$, is triangular, ramping down from $\Delta I_{\text{out}}$ and reaching zero when $i_{\text{buck}}$ equals $i_{\text{load}}$. In this case, the total transient time, $T_{tr}$, is governed by the main inductor’s slew-rate and current mismatch, and can be expressed as:

$$T_{tr,\text{loading}} = \frac{L}{V_{\text{in}}} \frac{\Delta I_{\text{out}}}{V_{\text{out}}}$$

$$T_{tr,\text{unloading}} = \frac{L}{V_{\text{out}}} \Delta I_{\text{out}}$$

(2.1)

where $L$ is the main inductor value and $V_{\text{in}}$ is the input voltage. This case produces a significantly shorter transient time than obtained using classical TOC approach since no additional discharging is required to drain excess charge from $C_{\text{out}}$.

Realization of an auxiliary unit as described by Fig. 2.3(a), rated for the peak load current is, to some extent, overly designed. It requires higher stress-rating components to accommodate for stress that exists for slight fractions of the transient time. Furthermore, an ideal response with zero voltage deviation is not an objective of a VRM. Since some amount of voltage deviation is still tolerable by standard, even in tight VRM applications [23], a more conservative approach can be taken. As shown in Fig. 2.3(b), improved unloading transient recovery, provided some allowed deviation margins, can be achieved by a constant current sinking profile of $I_{\text{aux}} = \Delta I_{\text{out}}/2$. It can be seen that although $v_{\text{out}}$ initially deviates from $V_{\text{out}}$, it is fully restored at $T_{tr}$. In the aforementioned cases the current source sinks an identical charge within $T_{tr}$, meaning that initial under-current is ultimately balanced by over-current at the second half of the transient. Considering a maximum allowable overshoot of $\Delta V_{\text{out}}$ and the greatest possible load change $\Delta I_{\text{max}}$, $C_{\text{out}}$ can be sized as follows:

$$C_{\text{out}} = \frac{\Delta I_{\text{max}}^2 L}{8 \Delta V_{\text{out}} V_{\text{out}}}$$

(2.2)

when compared to TOC, the shorter transient times and the smaller initial current mismatch are in favor of a hybrid-VRM, resulting in $C_{\text{out}}$ which is four times smaller.

The method shown in Fig. 2.3(b) reduces the complexity of the auxiliary circuit compared to the method in Fig. 2.3(a), however, it requires a fairly accurate estimation of the load current. To overcome this obstacle, a recovery pattern as shown in Fig. 2.3(c) is suggested. In this method the auxiliary current is set to $I_{\text{aux}} = \Delta I_{\text{max}}/2$ (by design) while the instantaneous $\Delta I_{\text{out}}$ is unknown. As long as $I_{\text{aux}} \geq \Delta I_{\text{out}}/2$, the resultant total transient time remains $T_{tr}$, governed by the main inductor’s slew-rate.
Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

The design of an auxiliary source that compensates for $\Delta I_{\text{max}}/2$ provides two main advantages: 1) the transient controller can be realized based purely on sensing the output voltage and without additional current sensing, and 2) the conditions for the end-of-transient are within the main inductor’s slew-rate for any given transient, without the need for extra time to reestablish the steady-state voltage.

2.3. Power processing efficiency

Present-day efficiency estimations for dc-dc converters are performed with general assumption of steady-state operation as the dominant working condition, defined here as static conversion efficiency. Neglecting switching losses and assuming steady-state operation, the main contributor for the conduction losses is the average inductor current since the rms current of the ripple component is negligibly small [4].

These estimations for the efficiency are relatively accurate for most applications in which the load is static or mostly-static. However, for modern applications with continuously varying loading conditions, the static conversion efficiency estimation might fail to predict the actual losses and as a consequence the required thermal design of the system. Fig. 2.4 shows comparison of a typical static efficiency curve compared with a dynamic loading one, for a similar average output power. As can be observed, the deviation of the static efficiency estimation from actual one significantly increases with the load repetition rate. It should also be noted that the situation worsen for applications with relatively high conversion ratios, such as the VRM case.

![Fig. 2.4](image)

Fig. 2.4 Power processing efficiency of a buck converter connected to a constant load, versus a 50kHz dynamic load with the same average current, 50% load duty-cycle (see Fig. 2.5). Series resistance is 10mΩ.

To analyze the converter efficiency under varying load conditions, three cases are compared as shown in Fig. 2.5: an ideal inductor current behavior, TOC [44] and beyond time-optimal one [68] which is adopted in this study. To focus on the difference between the
controllers types, it is assumed that all methods are governed by an identical steady-state control law.

Without loss of generality, the analysis to obtain the rms value of the inductor current for all cases is carried out under the assumption of a repetitive load transient with magnitude of $\Delta I_{\text{out}}$ and repetition rate of $f_{\text{tr}}$ and duty ratio of 50%. For the TOC case, the rms value of the inductor current can be expressed as

$$I_{\text{rms,TOC}} = \sqrt{I_{\text{min}}^2 + \frac{\Delta I_{\text{out}}}{2} + \frac{\Delta I_{\text{ripple}}}{12} \left(1 + \frac{\sqrt{D}}{1-f_{\text{tr}}} + \frac{\sqrt{1-D}}{f_{\text{tr}}}ight)} f_{\text{tr}}$$

(2.3)

where $I_{\text{min}}$ is the load current at light load, $I_{\text{min}} + \Delta I_{\text{out}}$ is the load current at heavy load, $\Delta I_{\text{ripple}}$ is the inductor’s steady-state current ripple and $D$ is the steady-state duty cycle, i.e. $D=V_{\text{out}}/V_{\text{in}}$.

Applying the hybrid-VRM control, the peaks, over and under the steady-state value are eliminated, the transient time is reduced, resulting in an rms current of:

$$I_{\text{rms,hybrid-VRM}} = \sqrt{I_{\text{min}}^2 + \frac{\Delta I_{\text{out}}}{2} + \frac{\Delta I_{\text{ripple}}^2}{12} \frac{L}{12D(V_{\text{in}}-V_{\text{out}})} f_{\text{tr}}}$$

(2.4)

Comparison of the resultant efficiency curves of (2.3), (2.4) and the ideal current waveform as a function of the load transients rate is shown in Fig. 2.6. As can be observed,
Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

the elimination of the additional restoration current, i.e. peaks, reduces the overall rms inductor current that in turn increases the power processing efficiency.

In addition, another design concern is the inductor sizing. As derived in [50], TOC results in current overshoot of $\Delta I_{\text{out}} \sqrt{D}$ and undershoot of $\Delta I_{\text{out}} \sqrt{1-D}$ during loading and unloading transients of $\Delta I_{\text{out}}$, respectively. Since these are eliminated by the hybrid-VRM approach, the sizing of the main inductor reduces as well.

2.4. Gyrator resonant switched-capacitor converter auxiliary circuit

The GRSCC topology has been recently presented in [13], based on the concept of a resonant switched-capacitor converter, but with the capability to maintain high efficiency over a wide and continuous step-up/down conversion ratio. Thanks to its soft-switching resonant nature it is applicable at high frequencies, and as a consequence, does not require a magnetic element. Furthermore, it has a bi-directional current sourcing behavior and is able to react immediately to create current step response with bandwidth of up to half its maximal switching frequency [81].

A voltage doubling variation of the GRSCC has been implemented in this study and is shown as the auxiliary circuit of Fig. 2.1. It is structured relying on a voltage multiplying resonant switched-capacitor converter topology, shifting the GRSCC’s optimal efficiency point from $V_{\text{out}}$ to $V_{\text{aux}} = 2V_{\text{out}}$. The main reason for the selection of this topology is to increase the power density of the auxiliary storage capacitor $C_{\text{aux}}$ by increasing its rated voltage, but without adding voltage stress to the transistors. Another advantage of the
Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

doubling realization is that the desired load-side current, i.e. $\Delta I_{\text{max}}/2$, can be obtained by a higher characteristic impedance of the resonant network. This implies that higher target efficiency of the GRSCC can be obtained for a given loop resistance.

The GRSCC is resonant in nature and can be completely halted at zero-current after each cycle. As a result, the nominal current can be resumed within one cycle. In the context of this study, this zero-order step capability enables the GRSCC to be used as the auxiliary current source unit. Moreover, there is no limitation to scalability, the resonant tank values can be determined for any desired $V_{\text{out}}$ and operating frequency with further option of interleaved operation. The bridge configuration also guarantees that the maximum stress on any given switch will be around $V_{\text{out}}$, which translates into small area requirements of the power switches.

To further reduce the overall volume of system and enhance the auxiliary circuit efficiency, it is realized in this study using three small interleaved GRSCC modules, each designed to output $\Delta I_{\text{max}}/6$, operating with phase delay of half-resonance period, as demonstrated in Fig. 2.7. By doing so, the auxiliary circuit rms current is reduced by a factor of $(2/3)^{0.5}$, when compared to a single-converter equivalent since there are more smaller pulses that are evenly distributed over the transient phase, for the same average current. This configuration also increases the accuracy and resolution as a current source. Furthermore, lower current is required per module, allowing higher impedance of the resonant network.

Fig. 2.7 Distribution of the auxiliary current between three interleaved GRSCCs operating at maximum frequency with half-resonance phase delay.
2.5. Hybrid-VRM controller

The configuration of the hybrid-VRM controller is divided into two main units as shown in Fig. 2.1, a steady-state voltage-mode controller that is entirely implemented on FPGA [82] and a transient-mode controller.

To facilitate fast transient detection and end-of-transient phase, the latter is assisted by two auxiliary comparators with two thresholds, well below the maximum allowed voltage deviation, to determine both loading and unloading transient events.

2.5.1. Principle of operation

The description of the hybrid-VRM controller operation is assisted by Fig. 2.8 which provides in-detail the response for an unloading transient event.

![Simulation results for the response of the hybrid-VRM to an unloading event.](image)

At \( t < t_0 \) the controller operates the buck converter with a voltage-mode steady-state compensator whereas the GRSCCs are idle. A load step at \( t_0 \) creates current mismatch between \( i_{\text{buck}} \) and \( i_{\text{load}} \) resulting in a rise of \( v_{\text{out}} \). At \( t_1 \), when \( v_{\text{out}} \) crosses \( V_{\text{ref,H}} \), an unloading event is detected by \( \text{cmp1} \) (Fig. 2.1) and a transient mode is initiated: \( Q_2 \) is turned on to ramp \( i_{\text{buck}} \) down with the highest slew-rate available. Simultaneously, the GRSCCs are activated to sink excess current and are set to \( I_{\text{aux}} = \Delta I_{\text{max}}/2 \). Since \( \Delta I_{\text{out}} < \Delta I_{\text{max}} \), at instance \( t_2 \), \( v_{\text{out}} \) returns within the steady-state range below \( V_{\text{ref,H}} \), the GRSCCs’ operation is halted while \( Q_2 \) remains on, however, \( i_{\text{buck}} \) is still larger than \( i_{\text{load}} \). This results in the output voltage rising over \( V_{\text{ref,H}} \) at \( t_3 \) which re-triggers the GRSCCs. When \( v_{\text{out}} \) is within the steady-state range at \( t_4 \), \( i_{\text{buck}} \) approximately equals to \( i_{\text{load}} \). The end of the transient phase (\( t_5 \)), in this case, is due to \( v_{\text{out}} \) crossing \( V_{\text{ref,L}} \), detected by \( \text{cmp2} \).
Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

The information on the end-of-transient is derived, in this study, from the output voltage measurement by observing the comparator states. However, the information that is obtained from the output voltage indicates on the current charge state of the output capacitor and not directly on the current mismatch between $i_{\text{buck}}$ and $i_{\text{load}}$. Given the example of Fig. 2.3(c), it can be observed that the output voltage is momentarily restored to the steady-state value without reaching the point that $i_{\text{buck}}$ equals $i_{\text{load}}$. The reason for this is that the charge balance has been achieved by the aid of the auxiliary circuit.

To overcome the problem of premature indication on the end-of-transient, without additional current sensors, a state-machine algorithm described by the flowchart of Fig. 2.9, was developed. The controller monitors the output voltage by observing the comparator states. When $v_{\text{out}}$ returns within the steady-state thresholds, the GRSCCs are immediately halted whereas the buck converter remains in transient mode. In case that a current mismatch still exists, the output voltage is shifted back beyond the boundaries, and the auxiliary circuit is re-triggered. A true end-of-transient indication (i.e., $i_{\text{buck}}$ is in the vicinity of $i_{\text{load}}$) is verified by either one of the necessary conditions: (a) the comparators state has been inverted from the original transient-mode trigger, or (b) a preset time has elapsed since the auxiliary circuit was halted without change in the comparator states.

![Flowchart of the end-of-transient algorithm](image)

2.5.2. Comparators threshold settings

A finite voltage difference between the comparators thresholds is required to prevent the controller from falsely entering or exiting the transient mode. To prevent false entry, it is sufficient to satisfy that the voltage difference between the thresholds is well above the
Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

steady-state voltage ripple and accounting for additional noise errors (e.g. ESR, switching noise, and measurement errors). However, to prevent a false indication of the comparators state and an early return to the steady-state mode, the difference between thresholds should be set such that the largest voltage deviation generated from a single discharge cycle of the auxiliary circuit is kept within the threshold boundaries. The largest value for this deviation occurs when current mismatch is small ($i_{\text{buck}} \approx i_{\text{load}}$), that is:

$$V_{\text{ref,H}} - V_{\text{ref,L}} \geq Q_g/C_{\text{out}} = 4V_{\text{out}}C_g/C_{\text{out}},$$

where $Q_g$ is the charge delivered from the auxiliary circuit during a single discharge cycle and $C_g$ is the GRSCC resonant tank capacitor. Selection of the voltage detection window according to (2.5) assures that the voltage-drop due to a single gyrator pulse is contained within threshold levels.

2.5.3. Auxiliart circuit halt time – $T_{\text{preset}}$

As described earlier, steady-state operation may be resumed by either inversion of the comparators state or after specific time has elapsed since the auxiliary circuit was halted ($T_{\text{preset}}$ in Fig. 2.9). Given the controller sequence when steady-state is resumed, and an estimation on the range of error for the buck inductor current at that instance, the preset time can be set to assure that the steady-state operation is restarted without creating additional oscillations. In this study, it is defined that the first switching action of the steady-state controller is the opposite of the one obtained in the nonlinear mode, i.e. resuming from an unloading event starts with an on state, whereas an on state during a loading event is followed by an off state. This implies that the preferred instance to switch back to the steady-state is when the inductor current has passed the target load current value since less error in the inductor current is accumulated by the following switching action. The ideal case would be at the point that the inductor current is beyond the load value by $\Delta I_{\text{ripple}}/2$, then the steady-state current is already within the target margins within the first switching action. Since this case cannot be guaranteed by voltage sensing alone, it is essential to map the range of the possible error in the current with respect to the preset halt time.

Fig. 2.10 shows a zoomed-in view to the preset instance, describing $i_{\text{buck}}$ within two worst-case scenarios. The time index, $t_{\text{last}}$, indicates the instance of the last trigger event of the auxiliary circuit. The lower boundary of the inductor current is characterized as the condition when the inductor current reached the load current at $t_{\text{last}}$, given by:

$$i_{\text{buck,min}}(t_{\text{last}} + t) = I_{\text{load}} + at,$$  

(2.6)
Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

where \(a\) is the slope of the buck inductor current during the transient, given by:

\[
a = -\frac{V_{\text{out}}}{L}, \quad \text{unloading}
\]
\[
a = \left(\frac{V_{\text{in}} - V_{\text{out}}}{L}\right), \quad \text{loading}
\]

The upper boundary of the inductor current is due to an additional charge injection by the auxiliary circuit, \(Q_a\), at the instance of \(t_{\text{last}}\), given by:

\[
t_{\text{buck,max}}(t_{\text{last}} + t) = I_{\text{load}} - a \left(\frac{2Q_a}{a}\right) + at.
\]

Equating (2.8) to \(I_{\text{load}}\) and solving for \(t\), yields the necessary condition to assure that the worst-case inductor current has reached the load current, that is:

\[
T_{\text{match}} = \sqrt{\frac{2Q_a}{|a|}},
\]

namely, the auxiliary circuit has completed its operation for the particular transient mode.

\[
I_{\text{load}}(t) = I_{\text{load}} + at + \sqrt{\frac{2Q_a}{|a|}}
\]

\[
\Delta I_{\text{target min}}, \quad \Delta I_{\text{target}}, \quad \Delta I_{\text{target max}}
\]

\[
T_{\text{match}}
\]

\[
T_{\text{min}}, \quad T_{\text{max}}
\]

\[
T_{\text{preset}}
\]

Fig. 2.10 Possible range of the buck inductor current around the \(T_{\text{preset}}\) instance.

To further reduce the error of the inductor current to the allowed range of \(\Delta I_{\text{target max}}, \Delta I_{\text{target min}}\), a target time range for return to steady-state is specified, as shown in Fig. 2.10. Equating (2.6) to the lower current boundary and (2.8) to the upper one, yields the margin criterion, \(T_{\text{min}}\) and \(T_{\text{max}}\), for \(T_{\text{preset}}\) as:

\[
T_{\text{min}} = \Delta I_{\text{target min}} / |a| + \sqrt{\frac{2Q_a}{|a|}}
\]
\[
T_{\text{max}} = \Delta I_{\text{target max}} / |a|
\]

(2.10)

It should be noted that it is required to assure that the defined \(T_{\text{preset}}\) satisfies the conditions in (2.10) and the minimum time condition in (2.9), that is,

\[
\max(T_{\text{min}}, T_{\text{match}}) \leq T_{\text{preset}} \leq T_{\text{max}}
\]

(2.11)
Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

Furthermore, to avoid dependence of $T_{\text{preset}}$ on the converter parameters and present dependence on the design considerations alone, (2.9) and (2.10) can be reorganized as:

$$
T_{\text{min}} = \frac{\Delta I_{\text{target,min}} (1-D)}{KI_{\text{nom}} f_s} + \sqrt{\frac{\Delta I_{\text{max}}}{KI_{\text{nom}} f_s f_g}}
$$

$$
T_{\text{max}} = \Delta I_{\text{target,max}} (1-D) / K I_{\text{nom}} f_s
$$

$$
T_{\text{match}} = \sqrt{\Delta I_{\text{max}} / K I_{\text{nom}} f_s f_g}
$$

(2.12)

where $f_s$ is main converter switching frequency and $f_g$ is the GRSCC maximal frequency, $I_{\text{nom}}$ is the nominal load current at steady-state, and $K = \Delta I_{\text{ripple}} / I_{\text{nom}}$ is the proportionality factor between the ripple and nominal currents. The criterion for a loading event can be extracted in a similar manner.

2.5.4. Auxiliary capacitor voltage reset

The amount of energy that is processed by the auxiliary circuit during a transient event depends on the conversion ratio of the buck converter. In this study of a 12V to 1.5V converter, during an unloading transient more charge is processed by the auxiliary circuit than during a loading transient of a similar magnitude. To maintain the ability to sink or source sufficient current from the output capacitor, prevent $C_{\text{aux}}$ from over-charging, and restore excess energy, a reset procedure for the independent auxiliary capacitor is essential.

A key consideration in the design of the reset procedure is to avoid interference with the desired steady-state operation of the main converter, i.e. that the reset procedure will not cause a significant change of the output voltage. This implies that the auxiliary circuit reset current has to sink or source sufficiently small amount of charge per pulse and to be distributed over a longer period of time compared to the total load transient time. To this end, in this study, one of the three GRSCC modules is further employed during the steady-state phase to balance the auxiliary charge and reset the capacitor voltage back to its target value. Since the output voltage is well-regulated by the steady-state controller, the module is allowed to operate as a classical open-loop resonant switched-capacitor converter, forcing the auxiliary capacitor to converge to $2V_{\text{out}}$, without any additional sensors. To limit the average current injected by the module during the reset phase, the effective operating frequency can be reduced by additional time delay between RSCC cycles [12].

Fig. 2.11 can be used to demonstrate the reset procedure. It shows an unloading transient that causes $v_{\text{aux}}$ to rise due to the current sinking operation. It is then followed by a reset
Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

performed using one GRSCC module operating as a RSCC at lower effective frequency which restores $v_{aux}$ back to the target value of $2V_{out}$. It can also be observed that the voltage-mode control law maintains $v_{out}$ within its steady-state margins.

![Simulated unloading transient followed by a reset of $v_{aux}$ back to $2V_{out}$](image)

2.6. Experimental verification

In order to validate the operation of the hybrid-VRM, a 20W 12V-to-1.5V prototype was built and tested, with a measured peak efficiency of 93%. The auxiliary circuit was realized by three interleaved GRSCCs as described in Section 2.4. TABLE I lists the component values and parameters of the experimental prototype. The digital controller comprises steady-state voltage-mode control and transient-mode control, realized on an Altera Cyclone IV FPGA [83]. Steady-state control is assisted by high-performance integrated ADC and DPWM on-FPGA realizations as described in [82]. Load transient signals were generated by an external signal generator, independently, without synchronization to the controller.

**TABLE I. EXPERIMENTAL PROTOTYPE VALUES**

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage $V_{in}$</td>
<td>12 V</td>
</tr>
<tr>
<td>Output voltage $V_{out}$</td>
<td>1.5 V</td>
</tr>
<tr>
<td>Main inductor $L$</td>
<td>1.3 uH</td>
</tr>
<tr>
<td>Output capacitor $C_{out}$</td>
<td>150 uF</td>
</tr>
<tr>
<td>Buck converter switching freq. $f_s$</td>
<td>500 kHz</td>
</tr>
<tr>
<td>GRSCC maximal switching freq. $f_g$</td>
<td>$\sim 1.7$ MHz</td>
</tr>
<tr>
<td>Auxiliary capacitor $C_{aux}$</td>
<td>20 uF</td>
</tr>
<tr>
<td>GRSCCs resonant tank capacitor $C_g$</td>
<td>0.3 uF</td>
</tr>
<tr>
<td>GRSCCs resonant tank inductor $L_g$</td>
<td>$\sim 10$ nH (stray inductance)</td>
</tr>
<tr>
<td>Number of GRSCC stages</td>
<td>3</td>
</tr>
</tbody>
</table>
Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

Fig. 2.12 presents the hybrid-VRM response to loading and unloading transient events of 7A in comparison to a buck converter operating under TOC, using same transient detection circuit. Fig. 2.12(a) and Fig. 2.12(b) show the response to a loading transient event of 7A (4.5A to 11.5A) for the hybrid-VRM and for TOC, respectively. For the hybrid-VRM, the performance of the system results in output voltage undershoot of 40mV and settling time of 2μs, compared with 80mV and 7μs using TOC. An unloading transient of 7A (11.5A to 4.5A) is depicted in Fig. 2.12(c) and Fig. 2.12(d). For this case, the output voltage overshoot using the hybrid-VRM is 40mV with total settling time of 8μs, whereas for the TOC case the output voltage overshoot is 150mV with settling time of 14μs. As can be observed in Fig. 2.12(c), the GRSCCs are triggered more than once, since the output voltage returns to the steady-state range before the inductor current has reached the new steady-state value, causing the output voltage to rise again, re-triggering the GRSCCs.

![Fig. 2.12 Experimental results showing a 7A load transient response of the hybrid-VRM [(a),(c)] versus TOC [(b),(d)]. Signals from top to bottom: \( v_{out} \) (100mV/div, ac coupled), \( i_{buck} \) (5A/div), and load-step signal. Time scale is 5μs/div. (a),(b) 4.5A-11.5A loading event. (c),(d) 11.5A-4.5A unloading event.

The system responses to larger load transients of 10A are given in Fig. 2.13. The loading event (1.5A to 11.5A) for the hybrid-VRM and TOC are presented in Fig. 2.13(a) and Fig. 2.13(b), respectively. The measured output voltage undershoot and total transient time for the hybrid-VRM are 60mV and 3μs and for the TOC case they are 120mV and 9μs. An unloading event (11.5A to 1.5A) for the two cases is presented in Fig. 2.13(c) and Fig. 2.13(d).
2.13(d). The hybrid-VRM response results in output voltage overshoot of 100mV with settling time of 12μs, and using TOC the voltage overshoot sums to be 390mV with 21μs settling time.

Fig. 2.13 Experimental results showing a 10A load transient response of the hybrid-VRM [(a), (c)] versus TOC [(b),(d)]. Signals from top to bottom: $v_{out}$ [(a), (b) 100mV/div, (c), (d) 200mV/div, ac coupled], $i_{back}$ (5A/div), and load-step signal. Time scale is 5μs/div. (a), (b) 1.5A-11.5A loading event. (c), (d) 11.5-1.5A unloading event.

Fig. 2.14 shows the hybrid-VRM’s response to a repetitive load transients of 7A (4.5A to 11.5A) at a frequency of 1 KHz with 50% load duty ratio. As can be observed, the output voltage overshoots and undershoots remain the same as in Fig. 2.12, validating the capability of the system to handle consecutive transients.

Fig. 2.14 Screenshot demonstrating the hybrid-VRM’s response to a repetitive 1 KHz loading-unloading transients from 4.5A to 11.5A. Output capacitor voltage 100mV/div, inductor current 5A/div, time scale 500μs/div.
Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

Fig. 2.15 shows the auxiliary capacitor voltage reset procedure, confirming its capability to balance the charge of the auxiliary capacitor without affecting the steady-state operation.

Fig. 2.15  Experimental results showing the auxiliary capacitor voltage reset procedure that follows an unloading transient. Signals from top to bottom: $v_{aux}$ (500mv/div), $v_{out}$ (100mV/div, ac coupled) $i_{buck}$ (5A/div), and load-step signal. Time scale is 50µs/div.

A transient efficiency measurement for the hybrid-VRM has been conducted and is presented in Fig. 2.16. As can be observed, the efficiency of the system reduces in a linear manner as the load transient rate is increases, as analyzed in Section 2.3.

Fig. 2.16  Experimental efficiency measurement of the hybrid-VRM for consecutive loading-unloading transients from 4.5A to 11.5A (see Fig. 2.14 for waveforms) with different load transients frequencies.

2.7. Conclusion

A voltage regulator module with improved loading and unloading transient response has been presented. The improvement has been achieved by the addition of a load-side auxiliary circuit that comprises three interleaved converters, implemented using a recently presented GRSCC topology. This VRM has the potential to be space conserving and cost-effective when implemented into an IC design. The output capacitance is significantly reduced at the cost of small additional semiconductors and few capacitors, and does not require ferromagnetic elements.

The experimental results exemplify the performance of the design for both loading and unloading events, reducing output overshoots by up to 390% and transient time by up to
Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gyrator Circuit

175% compared to TOC, without affecting the input side. In particular for the relatively high conversion ratio case, significant improvement has been demonstrated in the response to an unloading event, compensating for the moderate current slew rate of the buck inductor.

The hybrid-VRM operates autonomously with reduced circuit complexity, i.e. no additional current-sense circuitry or pre-transient information is required. In addition, since no complex mathematical estimations are needed, the complete FPGA implementation for the control (Including the ADC and DPWM peripherals) sums less than 8000 logic elements, providing a cost-effective and simple controller solution.
3. Stability Analysis of Boundary and Hybrid Controllers for Indirect Energy Transfer Converters

In boost converters and other IET topologies, transient-oriented controllers are designed to facilitate a dynamic response that may range from minimum time up to minimum output voltage deviation. Since analytical definitions for these control laws can become quite complex, a large-signal stability verification is not immediate. This chapter explores the existence of stability of IET converters that are controlled by either boundary or hybrid controllers and introduces a new simplified procedure for examination of large-signal stability of a given converter and load type using a graphical-analytical approach. The stability analysis and examination method are demonstrated on a boost converter loaded by resistive load and constant current load.

3.1. Overview

To obtain fast transient response, several transient-oriented controllers, e.g., time-optimal controllers have been introduced [44]-[50]. These controllers integrate nonlinear, state-variable based control laws, which allow convergence limited by the slew-rate of the reactive components. To further improve the system performance and reduce the total volume of the converter, in particular for boost-type converters, reduction of the components’ stress has been assigned as the primary performance goal [84]. This is achieved by defining the output voltage deviation as the control objective rather than the convergence time [18],[51].

Transient-oriented controllers can be generally divided into two types, boundary or hybrid. Boundary controllers [85]-[90], among them hysteretic and sliding-mode controllers, are geometry based methods that split the state-plane such that in one side of the boundary the operation is governed by the on state and by the off state at the other side of the boundary. Hybrid controllers [18], [44]-[51], [68], [91]-[94] switch between two or more control laws based on the system state variables in order to obtain the performance goals. Within the context of switched-mode applications, the hybrid control law typically incorporates a steady-state linear controller (i.e. PI or PID), to allow constant operating frequency, which simplifies the design of the power converter.

Following the proliferation of digital control technology [37]-[43], both boundary and hybrid control methods have regained popularity. In particular, sliding-mode
Stability Analysis of Boundary and Hybrid Controllers for Indirect Energy Transfer Converters

control [30], [95]-[97] and its extension have been exemplified for buck converters [98]-[101]. As frequently reported in many cases, realization of these controllers requires extensive computation resources as well as precise information on the system parameters to assure the desired performance and stability of the system. These would prohibit penetration of the controllers into real-world applications.

To overcome the challenges, hardware-efficient control methods with reduced sensitivity to variations of parameters for buck and boost converters have been recently presented in [44], [51] and [18], respectively. There, a hybrid controller combines a boundary-type control for large-signal transient events with a linear steady-state control law. The computing effort and parameter sensitivity can be reduced significantly by the realization of the boundary control law by comparators with reference assignment based on the system behavior during a transient event which is obtained from its state-space representation. The main limitation for the majority of these controllers is that their stability cannot be directly guaranteed using the known techniques since an analytical formulation of the control law is not immediate.

Stability investigations of boundary control and its derivatives, or large-signal stability, for switched-mode converters have been widely studied in the literature by observation and analysis of the state trajectories, either on the state-space [84],[20]-[21] or on the state-energy plane [102] with a primary control objective to obtain fast transient response. Since typical trajectories of switched-mode converters include spirals and hyperboles, it is quite difficult to formulate a control law for both well-defined behavior, simple implementation and that its stability can be assured by simple derivations. An example where existence of stability has been described and analyzed can be found in [44] for the specific case of direct energy transfer buck converter controlled by a hybrid-type, sliding-mode TOC. In cases where the control objective is beyond the simplistic case of fast response such as lower voltage deviation or other constraints added, and in particular IET converters, the pursuit after stability existence criteria to-date, is still ongoing.

The objective of this chapter is to explore the stability criteria of boundary and hybrid control methods for IET converters, delineate the necessary and sufficient conditions for large-signal stability, and to present a graphical-analytical approach to examine the large-signal stability of an arbitrarily given control law that is described on the state-plane. It is a further objective of this study to examine the behavior and the stability of the programmable-deviation controller for boost converters in [18] which includes the TOC as a particular case.
It should be noted that in this study, the analysis is not limited by the realization method of the controller (whether analog, digital or mixed-mode) as long that its operation can be described on the state-space.

The rest of the chapter is organized as follows: Section 3.2 reviews and discusses the properties of the load-line and its dependency on the load’s type. A stability analysis of boost converter loaded by resistive load and constant current load is presented in Section 3.3, including a physical interpretation and a procedure to examine large-signal stability of a given converter. Section 3.3 further extends a generalization of the stability analysis for unknown load type and other indirect energy transfer converters topologies. Experimental results and conclusion are then provided in Sections 3.4 and 3.5, respectively.

3.2. Review: the load-line

The load-line of a converter is defined by the set of all its asymptotic points (i.e. possible steady-state operating points) on the state-space for \( D \in [0,1] \) and for a given load value, where \( D \) is the duty ratio of the controlled switch.

Using any of the three methods described in [31] to obtain the load-line of a boost converter loaded by a constant current load (CCL), it is given by

\[
LL_{CCL}\{v_C,i_L\} = \{v_C,i_L : i_L = \frac{I_o}{V_{in}}v_C\}
\]  

(3.1)

and its state-plane is depicted in Fig. 3.1. For the CCL case, the on trajectories are straight lines and the off trajectories are ellipses.

Fig. 3.1 On and off trajectories and the load-line of a boost converter loaded by a CCL.
Stability Analysis of Boundary and Hybrid Controllers for Indirect Energy Transfer Converters

In a similar manner for a boost converter loaded by a resistive load (RL), the load-line can be expressed as

\[ LL_{RL}(v_C, i_L) = \left\{ v_C, i_L : i_L = \frac{1}{RV_{in}}v_C^2 \right\}. \]  

(3.2)

For this case, the on trajectories are exponential and the off trajectories are spirals instead of ellipses. However, within the region of interest for a boost converter where \( v_C > V_{in} \) and \( i_L > 0 \), the off trajectories can be well-approximated to ellipses. The differences between the load-lines of the two cases are depicted in Fig. 3.2. As can be observed, the load-line of a CCL is higher in \( i_L \) than the load-line of a RL, for \( v_C < V_{ref} \), which is the relevant region for loading transients.

Fig. 3.2 On and off trajectories and load-line (black) of a boost converter loaded by a RL and the CCL load-line from Fig. 3.1 (green).

3.3. Stability analysis

This section aims to delineate the region on the state-plane where large-signal stability exists. In the context of IET converters, the objective of the transient controllers ranges from minimum convergence time, i.e. TOC, up to minimum output voltage deviation. Therefore, examination of large-signal stability is essential within the control objective range.

Since the analytical definition and derivations for stability of a large-signal controller may become quite complex, the methodology of this study is to first define the limits of the stability region on the state-plane for a given converter and load type. Since the analysis for the stability region is based on the physical properties of the converter alone, then the evaluation per controller can be obtain graphically on any controller that can be drawn on
Stability Analysis of Boundary and Hybrid Controllers for Indirect Energy Transfer Converters

the state-plane. By doing so, the steps of the procedure are similar to any small-signal linear analysis that is in practice today, e.g. Bode, Nyquist or Nichols.

The limits of the stability region for a given converter are obtained by analysis of a control method that describes a curve (i.e. switching surface) in the state-plane. In particular, the well-known sliding-mode control is adopted because of its well-defined analytical description as well as the stability analysis for switched-mode converters [30]. The shape, or template, of the sliding-mode controller is chosen such that it is related to the physical properties of the converter, i.e. its load-line. This choice assists to conclude the results based on the converter’s physical properties, rather than on a specific control method.

The outcome of the analysis leads to a definition of the large-signal region-of-convergence (ROC), where the convergence to zero state-error is guaranteed for boundary controllers and passing through the steady-state operating point is guaranteed for hybrid controllers. Based on the analysis, a simplified procedure to examine large-signal stability of any arbitrary controller by a graphical-analytical approach is provided in subsection D.

In the following stability analyses an ideal boost converter is assumed, neglecting the capacitor’s ESR, MOSFET’s $R_{DS(on)}$ and diode forward voltage $V_D$. It should be noted that since the stability analysis is carried out under the assumption of small ripple approximation [30], the output voltage ripple has not been taken into account. The effect of the capacitor’s ESR on the stability analysis is negligibly small and estimated as the increment of the output voltage ripple. This shifts the stability boundaries on the output voltage axis by the value of the additional voltage ripple due to the ESR. It is also assumed that the delay caused by the load transient detection does not affect the system’s response as detailed in [18].

3.3.1. Resistive load stability analysis

For a boost converter loaded by a RL, the load-line is a parabola, therefore a parabolic switching surface $\sigma_{RL}$ is selected:

$$\sigma_{RL} = i_L - I_{ref} - \lambda_{RL} \left( v_C^2 - V_{ref}^2 \right)$$  \hspace{1cm} (3.3)

The converter’s average model can be expressed as

$$\frac{dv_C}{dt} = -\frac{v_C}{RC} + \frac{i_L}{C} (1-u)$$

$$\frac{di_L}{dt} = \frac{V_m - v_C}{L} (1-u) - \frac{54}{L}$$  \hspace{1cm} (3.4)
Stability Analysis of Boundary and Hybrid Controllers for Indirect Energy Transfer Converters

where \( u \) is the control input. The equivalent control \( u_{eq} \) along the switching surface is derived by taking the derivative of \( \sigma_{RL} \) with respect to time and setting \( \sigma \) [22] and can be expressed as

\[
u_{eq} = 1 - \bar{u}_{eq}, \quad \bar{u}_{eq} = \frac{V_{in} - L \frac{di_L}{dt}}{v_C}.
\]

Assuming small current ripple, \( V_{in} >> L\frac{di_L}{dt} \) [30], hence \( u_{eq} = 1 - \frac{v_C}{V_{in}} \). Substituting \( u_{eq} \) into (3.4) yields

\[
i_L = \frac{V_{in}^2}{RV_{in}} + \frac{C}{V_{in}} \frac{dv_C}{dt}.
\]

To examine whether the trajectories along the switching surface lead to a unique steady-state operating point, let \( \sim \) and \( \tilde{f} \) be the current and voltage errors, respectively, defined by the following relationship

\[
\sim = \frac{\sim}{f}.
\]

Substituting (3.6) into (3.7) yields

\[
\frac{\sim}{RV_{in}} + \frac{\sim}{V_{in}} \frac{d}{dt}.
\]

The expression obtained in (3.8) can be separated into two parts, one that represents the dc component, \( I_{DC} \), and the other that represents the time-dependent ac component \( i_{AC} \):

\[
I_{DC} = I_{ref} = \frac{V_{ref}^2}{RV_{in}}.
\]

\[
i_{AC} = \frac{\sim}{RV_{in}} + \frac{\sim}{V_{in}} \frac{d}{dt} + \frac{2V_{in}}{dt}.
\]

The dc part is, in fact, the desired steady-state operating point. Therefore, if \( i_{AC} \to 0 \) along the switching surface, the system is asymptotically stable and converges to the dc steady-state point. By substituting (3.7) and (3.10) into the switching surface \( \sigma_{RL} = 0 \) defined in (3.3) and after some manipulations, the following nonlinear differential equation is obtained:

\[
\frac{d}{dt} \left( \frac{\sim}{C} + \frac{1}{RV_{in}} - \lambda_{RL} \right) \sim.
\]
Stability Analysis of Boundary and Hybrid Controllers for Indirect Energy Transfer Converters

A variable replacement of $x = x^\sim$ results in the following first-order linear differential equation:

$$\frac{dx}{dt} + \frac{2V_{in}}{C} \left( \frac{1}{RV_{in}} - \lambda_{RL} \right) x = 0.$$  

(3.12)

Using (3.12), the stability condition of the switching surface can be obtained. The equation is stable for

$$\lambda_{RL} < \frac{1}{RV_{in}} = \lambda_{RL,\text{max}},$$  

(3.13)

i.e. $x \xrightarrow{t \to 0} 0 \Leftrightarrow \lambda_{RL} < \lambda_{RL,\text{max}}$. Therefore, $x^\sim$ is asymptotically stable and converges toward either one of two equilibria $x^\sim$. Since $x^\sim$ means that $v_C$ converges to $-V_{ref}$, a negative output voltage, this equilibrium is not valid for a boost converter. Since $x^\sim \xrightarrow{t \to 0} 0$ then $i_{dc} \xrightarrow{t \to 0} 0$ as well, and the state variables converges to $(V_{ref}, I_{ref})$. Hence, by selecting the switching surface (3.3) that satisfies condition (3.13), an asymptotical stability is guaranteed.

Sliding-mode control is a particular case of boundary control and requires two more conditions: existence and reachability. The existence condition is related to the reflective region, and sliding-mode operation occurs when the system is operating in reflective mode. Reachability condition is related to the operation in the reflective or refractive regions, but not in the rejective one. Although the switching surface of (3.3) is always reachable, it needs to be reachable near the steady-state operating point as well, otherwise the system converges to undesirable limit-cycles. Thus, another condition to guarantee that the switching surface does not pass in a rejective region is essential, as follows

$$\left. \frac{di_{dc}}{dv_C} \right|_{(v_{in},i_{in}) \to (v_{ref},i_{ref})} = 2\lambda_{RL} \frac{V_{ref}}{L_{ref}} > -\frac{R C V_{in}}{L_{ref}} = \left. \frac{di_{dc}}{dv_C} \right|_{(v_{in},i_{in}) \to (v_{ref},i_{ref})},$$  

(3.14)

therefore,

$$\lambda_{RL,\text{min}} = -\frac{R C V_{in}}{2L_{ref}^2}.$$  

(3.15)

Combining (3.13) and (3.15) results in the stability limits for any boost converter loaded by a RL as:

$$-\frac{R C V_{in}}{2L_{ref}^2} \leq \lambda_{RL} \leq \frac{1}{RV_{in}}.$$  

(3.16)
Stability Analysis of Boundary and Hybrid Controllers for Indirect Energy Transfer Converters

which guarantees that for any controller that is defined within these limits, the system will operate either in reflective mode or refractive mode (or both) and will be asymptotically stable. Thus, the ROC for this case can be depicted on the state-plane as in Fig. 3.3(a), bounded by the curve $\sigma_{RL,\lambda,\text{max}}$ which is the load-line and the curve $\sigma_{RL,\lambda,\text{min}}$ which is the upper limit, namely stability bound.

3.3.2. Constant current load stability analysis

For a boost converter loaded by a CCL the load-line is linear, a linear switching surface $\sigma_{CCL}$ is selected:

$$\sigma_{CCL} = i_L - I_{ref} - \lambda_{CCL} (V_C - V_{ref}),$$

(3.17)

and the converter’s average model can be expressed as

$$\frac{dv_C}{dt} = -\frac{I_o}{C} + \frac{i_L}{C} (1-u)$$

$$\frac{di_L}{dt} = \frac{V_{in}}{L} - \frac{v_C}{L} (1-u).$$

(3.18)

In a similar manner to the stability analysis in the earlier subsection for the RL case, the asymptotical stability condition for the CCL case can be expressed as:

$$\lambda_{CCL} < \frac{I_o}{V_{in}} = \lambda_{CCL,\text{max}}$$

(3.19)

which guarantees convergence of the state variables to $(V_{ref}, I_{ref})$. In the case of CCL, as opposed to RL, reachability is not guaranteed for every $\lambda_{CCL}$, therefore another condition is necessary to guarantee reachability of the switching surface, obtained from the slope of the on trajectory that passes through the steady-state operating point, that is:

$$\lambda_{CCL} > -\frac{C V_{in}}{L I_o} = \lambda_{CCL,\min}.$$ 

(3.20)

Combining (3.19) and (3.20) results in the stability limits of:

$$-\frac{C V_{in}}{L I_o} < \lambda_{CCL} < \frac{I_o}{V_{in}}.$$ 

(3.21)

The ROC for this case is depicted in Fig. 3.3(b). As demonstrated in Fig. 3.2, the load-line of the CCL case is higher (in $i_L$) than the load-line of the RL case, therefore, it can be
Stability Analysis of Boundary and Hybrid Controllers for Indirect Energy Transfer Converters

concluded that the lower bound of the ROC (e.g. its load-line) for the CCL case is stricter than the lower bound of the RL case in case of a loading transient.

\[
\begin{align*}
\sigma_{RL,\min} &= i_L - I_{ref} - \frac{CV_{in}}{2P_{out}}(V_{ref}^2 - V_C^2) \\
\sigma_{CCL,\max} &= i_L + I_{ref} + \frac{P_{out}}{V_{ref}}(V_{ref} - V_C) \\
\end{align*}
\]

Therefore, the ROC for an unknown type of load can be expressed as:

\[
ROC = \left\{ V_C, i_L : I_{ref} + \frac{P_{out}}{V_{ref}}(V_C - V_{ref}) < i_L < I_{ref} - \frac{CV_{in}}{2P_{out}}(V_C^2 - V_{ref}^2) \right\}.
\]
3.3.3. \textit{Physical interpretation of the stability conditions}

From conditions (3.13) and (3.19) for boost converter loaded by a RL and CCL, respectively, it can be deduced that in order to ensure stability, the switching surface must be above (in $i_L$) the load-line, for both cases. This observation can also be reinforced by a physical investigation of the converter.

The controller of the converter is in charge of bringing the state variables from an initial steady-state operating point to a new one. Each steady-state point indicates an instantaneous energy stored in the reactive components of the converter, i.e. $E = \frac{1}{2} C V^2_{\text{ref}} + \frac{1}{2} L i^2_L$. For a new loading event, the stored energy $E_{\text{old}} = \frac{1}{2} C V^2_{\text{ref}} + \frac{1}{2} L i^2_L$ must rise up to a new, higher energy $E_{\text{new}} = \frac{1}{2} C V^2_{\text{ref}} + \frac{1}{2} L i^2_{\text{ref}}$. To increase the stored energy over time, the input power $P_{\text{in}}$ of the converter must be higher than its output power $P_{\text{out}}$.

According to [86],[95], the load-line represents the states where $P_{\text{in}} = P_{\text{out}}$, and separates the state-plane to three regions, $P_{\text{in}} > P_{\text{out}}$, $P_{\text{in}} < P_{\text{out}}$ and $P_{\text{in}} = P_{\text{out}}$, as demonstrated in Fig. 3.5. This means that in order to increase the stored energy from $E_{\text{old}}$ to the new steady-state energy $E_{\text{new}}$, the state variables must be located at the region where $P_{\text{in}} > P_{\text{out}}$, i.e. above the load-line (in $i_L$), which is in agreement and guaranteed by satisfying conditions (3.13) and (3.19) for switching surfaces (3.3) and (3.17) of RL and CCL cases, respectively.

![Fig. 3.5](image-url)  
*Fig. 3.5 Input and output power on the boost converter loaded by a RL state-plane.*

The implication of the above statement is that any control method that will move the state variables toward the region on the state-plane where $P_{\text{in}} > P_{\text{out}}$ and will keep them in this region, will be able to converge toward the desired steady-state point. It should be noted that this intuitive observation assumes, without loss of generality, an idealized converter that does take into account losses for power balance. This however, does not affect the results, or strength of the analysis, since the derivations were obtained from a control theory perspective rather than power balance.
Stability Analysis of Boundary and Hybrid Controllers for Indirect Energy Transfer Converters

3.3.4. Stability examination procedure

Using the above analysis and observations, a generalized method to examine the large-signal stability for a given converter and load type is provided. The procedure is as follows:

a. Derive and draw the converter’s on and off state trajectories on the state-plane.
b. On the same plot, draw the load-line per the specific load type, or assume constant current load for more strict requirements.
c. Using the same plot, draw the stability bound per the load type,
   • Given output power level and in case that the load type is unknown, (3.23) can be used to obtain the ROC.
d. Draw the controller curve or switching surface per the control objective.
e. Verify that the controller maintains the converter’s states within the ROC, i.e. the load-line and the stability bound. If so, the system is asymptotically stable, otherwise, it is unstable.

Following the above procedure, rigorous theoretical analysis per case of a system-controller setting is no longer required. That is, mathematically describing and solving for the large-signal stability can be avoided and replaced by the graphical-analytical method of this study.

To demonstrate the stability examination procedure and verify its validity, a simulation test bench has been created. The results, presented in Fig. 3.6, have been carried out on a boost converter loaded by RL and controlled by a boundary and programmable-deviation controllers for loading transient. Fig. 3.6(a) shows a stable operation of boundary controller with switching surface within the ROC and indeed the system converges toward the new steady-state operating point. Fig. 3.6(b) depicts the operation of a boundary controller with switching surface outside the ROC, lower than the load-line, and the system diverges and cannot reach the new steady-state operating point. Fig. 3.6(c) presents the programmable-deviation controller operation. As can be observed, the controller maintains the state variables within the ROC and the system passes through the steady-state operating point, where the steady-state linear controller operation takes over. Fig. 3.6(d) shows the programmable-deviation controller when operating as a time-optimal controller. The stability of the controller is verified by following the above procedure and setting the controller in this case as described in (1.20). It can be seen that the controller maintains the state variables within the ROC and the system is asymptotically stable.
Stability Analysis of Boundary and Hybrid Controllers for Indirect Energy Transfer Converters

Fig. 3.6  Simulated boost converter loaded by a RL loading transient from $I_{\text{out,old}} = 0.55\, \text{A}$ to $I_{\text{out,new}} = 4\, \text{A}$.  (a) $\lambda_{\text{RL}} = 0.5 \lambda_{\text{RL,max}} < \lambda_{\text{RL,max}}$, switching surface is above the load-line (bottom – magenta), i.e. within the ROC, and the state variables converge to the new steady-state operating point $(V_{\text{ref}},I_{\text{ref}})$.  (b) $\lambda_{\text{RL}} = 1.07 \lambda_{\text{RL,max}} > \lambda_{\text{RL,max}}$, switching surface is outside the ROC, and the state variables diverge from the new steady-state operating point $(V_{\text{ref}},I_{\text{ref}})$.  (c) programmable-deviation control: The controller keeps the state variables within the ROC and they converge to the new steady-state operating point $(V_{\text{ref}},I_{\text{ref}})$.  (d) using programmable-deviation operating as time-optimal controller: The controller keeps the state variables within the ROC and they converge to the new steady-state operating point $(V_{\text{ref}},I_{\text{ref}})$. Top – inductor current, middle – output voltage, bottom – plane of inductor current and capacitor voltage.
The relationship between the controller location on the state-plane (with respect to its geometrical distance from the load-line and the stability bound) and the resultant time response is qualitatively characterized in Fig. 3.7. For few demonstrative illustrations, the time response resembles the behavior of a second order system with RHP zero. As can be observed, proximity to the load-line results in over-damped response whereas approaching the stability bound, a higher Q under-damped behavior is observed. Setting the controller outside the ROC results in either low Q-like divergence below the load-line (Fig. 3.7(a)) or oscillatory divergence above the stability bound (Fig. 3.7(e)).

3.3.5. Expansion of the Stability Analysis to Other Second-Order Indirect Energy Transfer Converters

By inspection of the state-plane for IET converters with two reactive components, high resemblance is found in their on and off state trajectories to a boost converter. For example, in the case of a non-inverting buck-boost (NIBB) converter, the on state trajectories are exactly matched with the ones in a boost converter and the off state trajectories of the NIBB converter are shifted left by a constant value of $V_{in}$ (for the same converter’s parameters – $L$, $C$, $V_{in}$, $V_o$, $P_{out}$). Using this insight, the stability analysis of subsections 3.3.1 and 3.3.2 can be expanded to other converters as well, by applying a simple transformation of the system’s parameters and the state variables ($v_C$, $i_L$), with respect to the input voltage $V_{in}$ and the load status ($I_o$ for a CCL case and $R$ for a RL case). The core concept is to transform $(v_{C}, i_{L}, V_{in}, I_o, R)$
Stability Analysis of Boundary and Hybrid Controllers for Indirect Energy Transfer Converters

(as defined in Fig. 3.8) into \((v'_C, i'_L, v'_i, i'_o, R')\) and then analyze the converter as if it is a boost converter with the provided stability analysis.

The transformation is detailed here for the NIBB converter, and the transformations for other converters is given in TABLE II.

Fig. 3.8 Second order IET converters: (a) Non-inverting buck-boost converter. (b) Buck-boost converter. (c) Flyback converter.

The state equations of NIBB converter loaded by a RL are

\[
\begin{align*}
\text{on} : & \quad \frac{dv_C}{dt} = -\frac{v_C}{RC} , \quad \frac{di_L}{dt} = \frac{V_{in}}{L} \\
\text{off} : & \quad \frac{dv_C}{dt} = \frac{Ri_L - v_C}{RC} , \quad \frac{di_L}{dt} = -\frac{v'_C}{L}
\end{align*}
\]

and the required transformation is as follows:

\[
v'_C = v_C + V_{in} , \quad i'_L = i_L , \quad V'_i = V_{in} , \quad R' = \frac{v'_C}{v_C} \frac{v_C - V_{in}}{v_C - V_{in}} R .
\]

Substituting (3.25) into (3.24) yields the state equations of a boost converter loaded by a RL as depicted in Fig. 3.9:

\[
\begin{align*}
\text{on} : & \quad \frac{dv'_C}{dt} = -\frac{v'_C}{RC} , \quad \frac{di'_L}{dt} = \frac{V'_i}{L} \\
\text{off} : & \quad \frac{dv'_C}{dt} = \frac{Ri'_L - v'_C}{RC} , \quad \frac{di'_L}{dt} = \frac{V'_i - v'_C}{L}
\end{align*}
\]

Fig. 3.9 Boost converter represented with transformed parameters and state variables of other indirect energy transfer converters.

In a similar manner, the transformations required for a CCL case are

\[
v'_C = v_C + V_{in} , \quad i'_L = i_L , \quad V'_i = V_{in} , \quad I'_o = I_o .
\]
Stability Analysis of Boundary and Hybrid Controllers for Indirect Energy Transfer Converters

As delineated by the derivation concept, the resultant state equations represent a boost converter with the structure as in Fig. 3.9, from which the analysis has already been established in subsections 3.3.1 and 3.3.2.

### TABLE II. Transformations of the System's Parameters of Second Order Indirect Energy Transfer Converters

<table>
<thead>
<tr>
<th></th>
<th>Constant Current Load</th>
<th>Resistive Load</th>
</tr>
</thead>
</table>
| **Non-Inverting Buck-Boost** | $v_C' = v_C + V_{in}$  
$i_L' = i_L$  
$V_{in}' = V_{in}$  
$I_o' = I_o$                                                                 | $v_C' = v_C + V_{in}$  
$i_L' = i_L$  
$V_{in}' = V_{in}$  
$R' = \frac{v_C'}{v_C - V_{in}} - R$                                                                 |
| **Buck-Boost** | $v_C' = V_{in} - v_C$  
$i_L' = i_L$  
$V_{in}' = V_{in}$  
$I_o' = I_o$                                                                 | $v_C' = V_{in} - v_C$  
$i_L' = i_L$  
$V_{in}' = V_{in}$  
$R' = \frac{v_C'}{v_C - V_{in}} - R$                                                                 |
| **Flyback**    | $v_C' = v_C + nV_{in}$  
$i_L' = i_L$  
$V_{in}' = nV_{in}$  
$I_o' = I_o$                                                                 | $v_C' = v_C + nV_{in}$  
$i_L' = i_L$  
$V_{in}' = nV_{in}$  
$R' = \frac{v_C'}{v_C - nV_{in}} - R$                                                                 |

#### 3.4. Experimental verification

To validate the results of the stability analysis, a 30W 3.3V-to-12V boost converter prototype was built and tested, using 6.8µH inductor and 30µF output capacitance and operating at switching frequency of 200kHz. The converter was loaded by a resistive load type. The prototype is controlled by a hybrid programmable-deviation controller and PCMC, implemented on an all-digital FPGA platform [83], including integrated high-performance ADC and DPWM [82].

Fig. 3.10(a) shows the system’s response to a 0.5A to 2.4A loading transient. As can be observed, the programmable-deviation controller keeps the converter’s states within the stability region, i.e. above the load-line and below the stability bound, resulting in stable operation and passing through the new steady-state operating point, where the PCMC...
controller takes over and maintains the steady-state operation. Fig. 3.10(b) shows the same loading transient response, but in this case the settings for the programmable-deviation controller were set in the same manner with a single difference on the resume conditions of the steady-state controller. This is done to represent operation of the system in the refractive mode, passing through the voltage steady-state value and the small-signal controller (that its stability can be easily guaranteed) is in charge of the bringing the converter’s states to the new operating point with zero error.

Fig. 3.10(c) shows the system’s response to a 0.5A to 2.4A loading transient with transient controller settings below the load-line. As can be observed, the controller cannot maintain the converter’s states within the stability region, resulting in unstable operation and divergence away from the new steady-state operating point.

A time-optimal response for the same loading conditions is depicted in Fig. 3.10(d). The time-optimal controller has been realized as a particular case of the programmable-deviation controller as described by (1.20). As can be seen, the trajectories are maintained within the ROC in compliance with analysis procedure of subsection 3.3.
Fig. 3.10 System’s response to a 0.5A to 2.4A loading transient: (a) using a programmable-deviation controller with boundaries maintaining the converter’s states within the ROC. (b) using a programmable-deviation controller with boundaries maintaining the converter’s states within the stability region, followed by steady-state CPMC controller to achieve zero-error state. (c) using a controller settings below the load-line that cannot maintain the converter’s states within the ROC. (d) using a programmable-deviation controller operating as time-optimal controller with boundary maintaining the converter’s states within the ROC. Time scale 20 µs/div. Inductor current (red) 2A/div [for (d) 2.5A/div], output voltage (blue) 0.5V/div AC coupled, and state-plane representation of inductor current and output voltage (bottom).
3.5. Conclusion

A large-signal stability analysis for IET converters has been presented, based on the physical properties of a converter and its load type. A generalized method for examination of large-signal stability of a given converter and load type is provided, delineating the region-of-convergence where large-signal stability exists, using a graphical-analytical approach. Once the region-of-convergence is extracted, the stability examination method is applicable to any control law that can be described on the state-plane. The conditions for stability, extracted from the stability analysis, were verified on both simulations and experimental test benches, testing the recently presented programmable-deviation controller and verifying the stability of time-optimal controller for a boost converter loaded by a resistive load and a constant current load. The stability analysis and examination method were found to be in excellent agreement with the simulated and experimental results.
4. Minimum-Time within a Deviation-Constrained Hybrid Controller for Boost Converters

This chapter introduces a new transient-oriented controller for boost-type converters. The controller incorporates a PCMC for steady-state operation and a nonlinear, state-plane based transient-mode control for load transients. The new hybrid controller facilitate convergence from a loading transient to the new steady-state point within the minimum possible time while constraining the output voltage deviation to a desired (minimal) value. As a result, the loading transient performance of IET converters may be significantly improved since two control objectives (time and undershoot) are simultaneously obtained. A detailed principle of operation of the controller is provided and explained through a state-plane analysis. The operation of the controller is experimentally verified, demonstrating a significantly lower output voltage deviation and lower peak inductor current when compared to TOC, allowing for significant volume reduction of the converter.

4.1. Overview

The implications of the control method on the resultant response may vary from one converter configuration to another. For example, with direct energy transfer converters, e.g. buck or forward, the TOC produces the fastest possible dynamic response to load transients with the minimum possible output voltage deviation. However, when applying TOC on IET converters, the fast dynamic response comes at the cost of higher output voltage deviation, increasing the sizing requirements from the output capacitor. On the other hand, minimum output voltage deviation for boost-type converters results in prolong transient time, infinite in the ideal case [18].

The main goal of this chapter is to introduce a new controller for boost converters that, compared to time-optimal solutions, constrains the output voltage deviation while maintaining fast convergence in response to load transients, allowing for output capacitance reduction. The minimum-time within a deviation-constrained (MTDC) hybrid controller is depicted in Fig. 4.1. It incorporates a steady-state PCMC and a transient-mode controller. The transient-mode controller utilizes a new nonlinear, state-plane based control and is designed to produce a load transient response that constrains the output voltage deviation to a desired value while minimizing the total transient time within this constraint.

The chapter is organized as follows: Section 4.2 delineates the state-plane and time representation. The controller’s design and control scheme are detailed in Section 4.3. Next,
Section 4.4 presents the minimum expected voltage drop for the controller. Experimental results and conclusion are then provided in Sections 4.5 and 4.6, respectively.

![Diagram of MTDC hybrid controller regulating operation of a boost converter.](image)

**Fig. 4.1**  MTDC hybrid controller regulating operation of a boost converter.

### 4.2. State-plane and time representation

In state-plane representation the time parameter is implicit and as a result, evaluation of the convergence period from one operating conditions to another is not immediate. However, the rate of convergence of a switched-mode converter can be expressed by means of energy and power with respect to the state variables. This section aims to describe the relationship between the time of convergence and the movement of the state variables on the state-plane by an example of a loading transient on a boost converter that is loaded by a resistive load (RL).

The controller of the converter is in charge of bringing the state variables from an initial steady-state operating point to a new one. Each steady-state point indicates an instantaneous energy stored in the reactive components of the converter, i.e. \( E = \frac{1}{2} C V_C^2 + \frac{1}{2} L i_L^2 \). For a new loading transient event, the stored energy \( E_{\text{old}} = \frac{1}{2} C V_{\text{ref}}^2 + \frac{1}{2} L i_{\text{ref}}^2 \) must rise up to a new, higher energy \( E_{\text{ref}} = \frac{1}{2} C V_{\text{ref}}^2 + \frac{1}{2} L i_{\text{ref}}^2 \). The rate of energy change in the converter can be obtained by taking the energy derivative with respect to time, as follows

\[
\frac{dE}{dt} = C V_C \frac{dV_C}{dt} + L i_L \frac{di_L}{dt} = V_{\text{in}} i_L - \frac{V_C^2}{R} = P_{\text{in}} - P_{\text{out}} = \Delta P. \tag{4.1}
\]
Minimum-Time within a Deviation-Constrained Hybrid Controller for Boost Converters

This implies that the energy rises faster for higher difference between the input and output power. For a boost converter case, (4.1) is valid for both the on and off state trajectories.

According to [31], [95], the load-line represents the states where $P_{in} = P_{out}$, i.e. $\Delta P = 0$. Accordingly, the points on the state-plane where $i_L = \frac{v_C^2}{RV_{in}} + A$, $A > 0$, represent points where $\Delta P = AV_{in}$. As demonstrated in Fig. 4.2, higher $i_L$ results in higher $\Delta P$, and when above the load-line, $\Delta P$ will be greater than zero which will expedite the convergence for a loading transient. Using this observation and taking into account the possible trajectories of the converter, an enhanced convergence time controller can be designed as detailed in the next section.

![Fig. 4.2](image)

**Fig. 4.2** Power representation on the state-plane of a boost converter loaded by a RL.

### 4.3. Minimum-time within a deviation-constrained hybrid controller

The objective of transient-oriented controllers ranges from minimum recovery time to minimum output voltage deviation and usually focus on one of them. As opposed direct energy transfer converters, e.g. buck or forward, where minimum convergence time results in minimum voltage deviation, a control objective of minimum voltage drop for an IET converter, results in long transient time which is, in fact, infinite in the ideal case [18]. The reason for this behavior is that the first point in the region of convergence is located on the load-line where $\Delta P = 0$, and therefore the convergence rate is slow. Based on the energetic description of the previous section, a controller that combines a minimum recovery time for an allowed voltage deviation constraint has been developed. The new controller provides an extremely fast dynamic response for loading transients without adding components’ stress due to high voltage deviation or high peak current.

The explanation for the design of the controller is aided by the state-plane illustration of Fig. 4.3. At the detection of a loading transient, by turning the transistor on, the on
Minimum-Time within a Deviation-Constrained Hybrid Controller for Boost Converters

trajectory brings the state variables to the \((V_{\text{min}}, I_{\text{min}})\) point (the intersection with the load-line, see subsection 4.4). Following the possible trajectories of a boost converter, convergence to the new steady-state \((V_{\text{ref}}, I_{\text{ref}})\) is impossible without a further increment of the inductor current and as a result, increasing the voltage drop. Employing the observations of the previous section, the fastest way to increase the stored energy without increasing the voltage deviation is to ramp up the inductor current vertically, along \(V_{\text{th}}\). Since such trajectories do not exist, a simple hysteretic-type sliding mode control has been added, creating a pseudo-vertical trajectory by a sequenced on and off states and moving the state variables in the desired direction. This control law can be realized by a simple comparator with hysteresis, and as a sliding-mode controller can be expressed as:

\[
\sigma(v_c, i_L) = v_c - V_{\text{th}}
\]

\(\text{on: } \sigma > 0\)

\(\text{off: } \sigma < 0\) \hspace{1cm} (4.2)

\[
\Delta P_1 = P_3 \quad \Delta P_2 = P_1 \quad (V_{\text{ref}}, I_{\text{ref}})
\]

\[
\Delta P = P_2 \quad \Delta P = P_1 \quad (V_{\text{min}}, I_{\text{min}})
\]

\(V_{\text{th}}\) \(v_L\) \(I_{\text{final}}\) \(P_1 < P_2 < P_3\)

\[
\sigma = 0 \quad \text{on trajectory}
\]

\[
I_{\text{final}} \quad \frac{V_{\text{ref}}}{R} + \sqrt{\frac{C}{L} \left( \frac{V_{\text{ref}}}{R V_{\text{in}}} - V_{\text{in}} \right)^2 + \left( \frac{V_{\text{ref}}}{R V_{\text{in}}} - \frac{V_{\text{ref}}}{R} \right)^2} \quad (4.3)
\]

\[
\Delta P = P_2 \quad \Delta P = P_1 \quad (V_{\text{ref}}, I_{\text{ref}})
\]

\[
(V_{\text{th}}, I_{\text{th}})
\]

Fig. 4.3 Desired movement of the state variables on the state-plane for a loading transient.

4.3.2. Principle of operation

During steady-state operation, the PCMC controller is active. Upon detection of a loading transient, from \(I_{\text{old}}\) to \(I_{\text{ref}}\), the transient controller recovers from a loading transient in a three-step process, as demonstrated in Fig. 4.4. First, the PCMC controller is bypassed and the transistor of the boost is turned on. During this time, the controller sets two thresholds, one for the output voltage \(V_{\text{th}}\) and the other for the inductor current \(I_{\text{final}}\). \(V_{\text{th}}\) is the deviation constraint and \(I_{\text{final}}\) is determined by the off state trajectory passing through the new steady-state operating point and \(V_{\text{th}}\), given by
Minimum-Time within a Deviation-Constrained Hybrid Controller for Boost Converters

Once $V_{th}$ has been reached, during the second step, the controller operates as sliding-mode controller along the boundary (4.2), causing the inductor current to rise up without changing the voltage. The end of the second step is defined when the inductor current has reached $I_{final}$. Then, the controller enters the third and last step, turning the transistor off and ramping down the inductor current by charging the output capacitor back to the steady-state voltage $V_{ref}$. Once reaching $V_{ref}$, the transient recovery is completed and the steady-state PCMC controller is resumed.

![Simulated response of the MTDC hybrid controller to a loading transient of a boost converter loaded by a RL. Output voltage (top - blue), inductor current (middle - red), and state-plane representation of the voltage and current (bottom).]({})

**Fig. 4.4** Simulated response of the MTDC hybrid controller to a loading transient of a boost converter loaded by a RL. Output voltage (top - blue), inductor current (middle - red), and state-plane representation of the voltage and current (bottom).

### 4.4. Minimum expected voltage drop

In the design of the MTDC controller and the converter’s components, information on the expected voltage drop is essential to determine feasibility of convergence [2]. In this section, the minimum possible output voltage deviation that enables the converter to converge toward the new steady-state operating point for the case of a loading transient of a boost converter is analyzed.
Minimum-Time within a Deviation-Constrained Hybrid Controller for Boost Converters

The definitions made for the analysis are as follows, the minimum output voltage deviation point $V_{\text{min}}$ is the upper limit for $V_{\text{th}}$, i.e. $V_{\text{th}} < V_{\text{min}}$ must hold in order to converge toward the steady-state operating point [2]. The lower limit of $V_{\text{th}}$ is $V_{\text{th,TOC}}$, where $V_{\text{th,TOC}}$ is the minimum output voltage that is obtained by TOC. Setting $V_{\text{th}}$ further lower than $V_{\text{th,TOC}}$ results in a voltage overshoot once the voltage has recovered due to overcharging of the inductor [50].

The extraction of the $V_{\text{min}}$ is carried out by examination of the converter’s state trajectories and the load-line [31]. Exemplified on a boost converter, the state-plane trajectories and the load-line for the case when loaded by a constant current load (CCL) can be extracted from the set of differential equations:

\[
\begin{align*}
\text{on} & : \quad \frac{dv_C}{dt} = -\frac{I_o}{C}, \quad \frac{di_L}{dt} = \frac{V_{\text{in}}}{L} \\
\text{off} & : \quad \frac{dv_C}{dt} = \frac{i_L - I_o}{C}, \quad \frac{di_L}{dt} = \frac{V_{\text{in}} - v_C}{L}.
\end{align*}
\] (4.4)

Using any of the three methods presented in [31] to obtain the load-line, it is given by (3.1) and its state-plane is depicted in Fig. 3.1. For this type of load, the on trajectories are straight lines and the off trajectories are ellipses. In a similar manner for a RL case, the state-plane trajectories of a boost converter are derived from

\[
\begin{align*}
\text{on} & : \quad \frac{dv_C}{dt} = -\frac{v_C}{RC}, \quad \frac{di_L}{dt} = \frac{V_{\text{in}}}{L} \\
\text{off} & : \quad \frac{dv_C}{dt} = \frac{Ri_L - v_C}{RC}, \quad \frac{di_L}{dt} = \frac{V_{\text{in}} - v_C}{L}.
\end{align*}
\] (4.5)

and the load-line can be expressed as (3.2).

For this case, the on trajectories are exponential and the off trajectories are spirals instead of ellipses. However, within the region of interest for a boost converter where $v_C > V_{\text{in}}$ and $i_L > 0$, the off trajectories can be well-approximated to an ellipses. As demonstrated in Fig. 3.2 and mentioned earlier, for the same output power, the load-line of the CCL case is higher in $i_L$ than the load-line of the RL case for $v_C < V_{\text{ref}}$, which is the relevant region for loading transients.

The smallest possible output voltage deviation is obtained on the state-plane by the intersection of the on state trajectory, starting at the previous steady-state point, with the load-line. As shown in Fig. 4.5, the minimum voltage deviation varies with the load type for a load transient of the same magnitude $\Delta I_{\text{out}}$. As can be observed, the intersection point of the RL case ($V_{\text{min,RL}}, I_{\text{min,RL}}$) occurs at higher voltage and lower current compared to the
Minimum-Time within a Deviation-Constrained Hybrid Controller for Boost Converters

intersection of the CCL case \((V_{\text{min,CCL}}, I_{\text{min,CCL}})\), i.e. \(\Delta V_{\text{RL}} < \Delta V_{\text{CCL}}\) and \(I_{\text{min,CCL}} > I_{\text{min,RL}}\). The on state trajectory for the CCL case is given by

\[
i_L = I_{\text{old}} - \frac{CV_{\text{in}}}{LI_{\text{o}}}(v_C - V_{\text{ref}}) \tag{4.6}
\]

and for the RL case is given by

\[
i_L = I_{\text{old}} - \frac{RCV_{\text{in}}}{L} \ln \left(\frac{v_C}{V_{\text{ref}}}\right) \tag{4.7}
\]

Fig. 4.5 First on state trajectories and the load-lines intersections for CCL case (dotted) and RL case (solid).

For an arbitrary operating point \((V_{\text{ref}}, I_{\text{old}})\), \(V_{\text{min,CCL}}\) can be calculated by solving (3.1) and (4.6), and is given by

\[
V_{\text{min,CCL}} = \frac{CV_{\text{ref}}^2V_{\text{ref}} + LV_{\text{in}}I_{\text{o}}I_{\text{old}}}{LI_{\text{o}}^2 + CV_{\text{in}}^2} \tag{4.8}
\]

where the inductor current at this point is

\[
I_{\text{min,CCL}} = \frac{I_{\text{old}}V_{\text{min,CCL}}}{V_{\text{in}}} \tag{4.9}
\]

For the RL case, the exact solution for the minimum output voltage deviation \(\Delta V_{\text{RL}}\) can only be calculated using numerical methods due to the complexity of the trajectories. By approximating the first on state trajectory to a straight line, under the assumption that the voltage deviation \(\Delta V_{\text{RL}}\) is relatively small, a solution exists and \(V_{\text{min,RL}}\) and \(I_{\text{min,RL}}\) are given by

\[
V_{\text{min,RL}} = \frac{CRV_{\text{in}}^2V_{\text{ref}} + LRV_{\text{in}}V_{\text{ref}}I_{\text{old}}}{LV_{\text{ref}}^2 + CRV_{\text{in}}^2} \tag{4.10}
\]

where the inductor current at this point is

\[
I_{\text{min,RL}} = \frac{V_{\text{min,RL}}^2}{RV_{\text{in}}} \tag{4.11}
\]
Minimum-Time within a Deviation-Constrained Hybrid Controller for Boost Converters

4.5. Experimental verification

To validate the operation of the MTDC controller, a 30W 3.3V-to-12V boost converter was built and tested, using 6.8\(\mu\)H inductor and 30\(\mu\)F output capacitance and operating at a switching frequency of 200kHz. The converter was loaded by a resistive load type. The MTDC controller was realized on an all-digital FPGA platform [83] including high-performance ADC and DPWM [82] with the addition of one voltage hysteresis comparator.

A dynamic response comparison of the MTDC controller for two different voltage deviations and TOC for a loading transient of 0.5A to 2.4A is depicted in Fig. 4.6. Fig. 4.6(a) show the dynamic response when \(V_{th}\) is set to be slightly lower than \(V_{\text{min}}\) with a 1.55V output voltage deviation, resulting in a total transient time of 75\(\mu\)s and peak inductor current of 14.2A. The dynamic response when setting a larger output voltage deviation of 1.75V is depicted in Fig. 4.6(b), accelerating the response with total transient time of 60\(\mu\)s with a slightly larger peak inductor current of 14.5A. Fig. 4.6(c) shows the TOC dynamic response. As can be observed, a faster response with total time of 45\(\mu\)s is achieved at the cost of significantly larger output voltage deviation of 3.25V and high 17A peak inductor current.

Fig. 4.6  Boost converter’s response to a 0.5A to 2.4A loading transient using the MTDC and time-optimal controllers: (a) MTDC controller with \(V_{th} \approx V_{\text{min}}\), (b) MTDC controller with \(V_{th} < V_{\text{min}}\), (c) time-optimal controller. Time scale 20\(\mu\)s/div, output voltage (0.5V/div, AC coupled, top - blue), inductor current [(a) 2A/div, (b) 2A/div, (c) 2.5A/div, middle - red], and state-plane representation of output voltage and inductor current.

4.6. Conclusion

A minimum-time within a constrained output voltage deviation hybrid controller for boost converters has been presented. The controller hybrids a steady-state PCMC controller for steady-state operation and a nonlinear transient-mode controller for load transients. A
Minimum-Time within a Deviation-Constrained Hybrid Controller for Boost Converters

state-plane and time analysis has been carried out, followed by a controller design that is based on the theoretical investigation. The transient-mode controller implementation is straightforward and simple, consisting of a three-step transient recovery process, and only requires one additional hysteresis comparator. An analysis of the minimum possible output voltage deviation has been presented, providing the required margins for the design of the controller and the expected voltage drop.

Experimental results of a 30W 3.3V-to-12V boost converter prototype are provided. For loading transients, compared to TOC, the MTDC controller produce significant lower output voltage deviation and lower current stress, enabling volume reduction of the reactive components, with small addition to the total transient time.
5. Discussion

5.1. Contribution of the research

Hybrid voltage regulator module – To handle the extremely fast load changes of voltage regulator modules, the hybrid-VRM hybrids a switched-inductor converter and a resonant switched-capacitor converter, each of them excels in different tasks. The switched-inductor converter excels in steady-state operation to maintain good efficiency and the resonant switched-capacitor converter can produce current step response to handle load transients. The combination of two types of converters for VRMs forms a new concept and has been proven throughout the research that it can reduce the overall volume of VRMs and improve the power processing efficiency.

Definition of the region-of-convergence for IET converters – Full analytic extraction of the region-of-convergence based on the physical properties of a converter and its load type, providing tangible assistance for the design of new control methods for IET converters.

Simplified stability examination procedure for IET converters - A generalized method for examination of large-signal stability of a given converter and load type is provided, delineating the region-of-convergence where large-signal stability exists, using a graphical-analytical approach. Once the region-of-convergence is extracted, the stability examination method is applicable to any control law that can be described on the state-plane.

Stability proof of the programmable-deviation controller and time-optimal controller for IET converters - A large-signal stability proof for different modern control methods that has yet to be proven using the above stability examination procedure has been presented, supporting their applicability in real-world applications.

Minimum-time within a deviation-constrained hybrid controller – reducing the overall volume of IET converters by reducing the reactive components’ stress while maintaining extremely fast load transient response.

Practical considerations for the design of controllers for IET converters – Accurate definition of the minimum output voltage deviation that is required to successfully recover from loading transients, providing simple information regarding the sizing requirements of the passive components of a given converter.
5.2. Suggestions for future research

Some suggestions for future lines of investigation that can be developed as a result of this thesis are outlined below:

**Auxiliary capacitor voltage reset for the hybrid-VRM** – A better definition of the auxiliary capacitor voltage reset is required, more specifically regarding the timing of the reset procedure and the amount of current that should be sank or sourced without affecting the steady-state controller.

**Development of new nonlinear control methods for IET converters** – Using the stability examination procedure and the region-of-convergence for IET converters, new application-oriented control methods that produce a required dynamic response, e.g. with absolutely no current overshoot, can be developed.
6. Appendix – Derivation of the state trajectories for buck and boost converters

An example of deriving the state trajectories is given for a buck converter loaded by a constant current load from the state equations (1.11) and (1.12). The trajectories are derived by using the second method for state trajectories drawing (see subsection 1.2.3) by solving the integral.

Solving the integral for the on state trajectories

\[
\int \frac{i_L - I_o}{C} \, di_L = \int \frac{V_{in} - v_C}{L} \, dv_C
\]

yields the following expression

\[
C(v_C - V_{in})^2 + L(i_L - I_o)^2 = C(v_C - V_{in})^2 + L(i_L - I_o)^2,
\]

that represents an ellipse in the state-plane with a center at the point \( (V_{in}, I_o) \).

The same procedure can be used to find the off state trajectories, this yields the expression

\[
Cv_C^2 + L(i_L - I_o)^2 = Cv_C^2 + L(i_L - I_o)^2,
\]

that represents an ellipse in the state-plane with a center at the point \( (0, I_o) \). Fig. 6.1 shows the on and off state trajectories for different initial conditions.

Fig. 6.1 State-plane state trajectories of a buck converter. On state trajectories are in red, off state trajectories are in blue.
Appendix – Derivation of the state trajectories for buck and boost converters

Another example is the state trajectories of boost converter loaded by a constant current load. For this case, the on state trajectories are straight lines whereas the off state trajectories are ellipses with center at the point \((V_{\text{in}}, I_0)\), as shown in Fig. 6.2.

![State-plane state trajectories of a boost converter. On state trajectories are in red, off state trajectories are in blue.](image)

The state-plane and state trajectories of the boost converter reveals an interesting property regarding the RHP zero. As can be observed, all the on trajectories are directed towards the negative value of the horizontal axis, the capacitor voltage axis. This means that during on state the capacitor voltage is decreasing, which is a property of indirect energy transfer converters with RHP zero.
7. References


References


References

References


References


