A CMOS TERNARY ROM CHIP

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ABSTRACT

This paper presents a read only memory based on three valued memory cells. The ROM has been designed for use in a ternary digital system. It is a 2187x5 trit, contact programmed device. The Northern Telecom CMOS 3 micron, double metal process has been used in the implementation of the device.

1. INTRODUCTION

Read Only Memories (ROMs) are used for many purposes in digital systems. Microprogramming and program code are the usual contents for ROMs but logic functions may also be implemented using the ROM.

This paper presents a ROM using three-valued memory cells. The ROM has been designed for a ternary digital system and therefore has both ternary inputs and outputs. It has been submitted for fabrication to the Northern Telecom Silicon foundry through the Canadian Microelectronics Corporation.

1.1 Previous ROM Designs

The ROM has a major advantage over other memory devices. This feature is the non-volatile nature of the memory device. If the power supply is shut off, the ROM will retain data. This makes the device well suited for storing data which should be kept in the system for a long period of time, and especially when the system power supply is shut off.

The ROM achieves this by storing the bits as devices or contacts in a memory matrix. The typical representation would be the presence of a transistor if the memory location were to store a zero and the absence of a transistor if the memory location were to store a one.

There are two basic ROM structures, the NOR array and the NAND array [HODG83]. The NAND structure is very compact, and achieved by using serially connected transistors in the memory matrix. This structure, with the load, yields a NAND gate. The NOR structure uses the memory matrix transistors in a parallel structure. Although the geometric layouts differ, the functional operation of most ROMs follow either the NAND or NOR arrangement.

Early ROMs are based on an array of transistors, arranged in rows and columns [HNAT77]. This has made the layout of the devices very simple but has not yielded the most area efficient layout available.

The next step in minimizing the area of the memory cell has been the use of shared contacts [HNAT77]. The regular array structure is maintained but the contacts are shared.

The array type structure has been developed to a stage where the area this type of structure occupies has been minimized. It was evident that further minimization of area would be possible only if the basic cell structure was changed. This further minimization has been achieved by the use of the X-cell structure. The use of virtual grounds and the arranging of transistors so that they form an X around shared contacts has minimized area [PRIN83].

Obviously, the only way to further increase density is to reduce the feature size. This is a problem with binary ROMs. The data capacity of the binary ROM is dependent on the continued reduction of the transistor size.

Some designers have concentrated on attempting to place more data per memory cell. If a memory cell can be designed to hold more data than the usual one bit, yet maintain approximately the same size, then higher data density can be achieved. This may be possible by the use of multi-valued logic design.

One of the first multi-valued designs has been used in two Intel chips. The 8087 numeric co- processor and the Intel 432 I/O processor both use an nmos ROM based on four-valued cells [AGAR84].

Motorola has a commercial device, the MCM65256, which is a four-valued CMOS ROM, based on a combination of multi-valued cells and an X-cell type structure [DONO85]. General Instruments also realized a ROM with the same data capacity. This device is also based on the four-valued cell [RICH86][RICH85].

At ISMVL85, another NMOS ROM based on the four state memory cell has been presented [ETIE85]. It is a small device, offering 1K bytes of storage. It is based on the older array type structure, but has used shared contacts.

Concentrating on ternary systems, two previous ROMs have been designed. Mouftah [MOUF77] based his ROM design on a structure called the Modified Ternary Inverter (MTI). Each memory cell in the ROM includes a n-type device, a p- type device and a voltage divider. The position of the contact determines the programming of the cell.

Another ternary ROM design is based on the

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transmission gate [MOUF84]. In this case, the memory cell is a transmission gate connected to either the high or low power supply. The output of the gate is connected through a resistor to ground to provide the intermediate level. The programming of the cell is accomplished by connecting the gate to the low, or high power supply for the low and high states respectively, and left unconnected if the middle state is to be the output.

1.2 Programming Issues

Programming a ROM is an important consideration. If the step which implements the programming can be kept to one of the last processing steps in fabrication, then the actual firmware development may continue during the initial stages of chip fabrication.

Each of the above ROM types are programmed differently. The earliest ROMs have the programming done at one of the last stages in processing; the metallization layer. These ROMs are programmed by connecting the appropriate device contacts to the bit lines.

The shared contact memory structure is based on the presence or absence of a transistor at the memory location representing the bit. The programming for this structure occurs at either the diffusion or polysilicon fabrication step [PRIN83]. The X-cell structure is programmed in a similar fashion [PRIN83]. An implant may also be used to alter the transistor threshold voltage, and thereby program the device [HNAT77].

The multi-valued ROMS are also programmed in different ways. The ROM presented in [ETIE85], the Intel ROM [AGAR84] and the Motorola ROM [DONO85] are all programmed by adjusting the width to length ratio of the memory cell transistors. The General Instruments design [RICH85] uses implants to vary transistor thresholds.

The variable width to length ratio technique is called variable geometry and from the point of view of fabrication, it is preferable to the variable threshold method [DONO85]. It uses the varying sizes of the transistors to control the current and voltage drop across the transistor. This means a standard fabrication process can be used, rather than a specialized one, such as the additional implant steps used in the General Instruments ROM.

2. THE TERNARY ROM

The ternary ROM (TROM) presented in this paper is a pure ternary device, as far as the system designer is concerned. It is designed for a ternary system and therefore the address inputs and the outputs of the device are ternary. The TROM uses a split power supply and the output logic levels are at +3 volts for the high level, 0 volts for the middle level and -3 volts for the low level. The normal ternary logic representation of (2,1,0) corresponds to the high, middle and low logic levels.

The device has seven address lines and five output data lines. Data is placed onto the output pins when the chip enable is placed in logic low. The operation of the ROM is static.

3. CHIP INTERNAL DESIGN

The TROM has five major subsystems. These are the input protection subsystem, the address to memory matrix decoding subsystem, the memory matrix subsystem, the sense amplifier subsystem and the output subsystem. The block diagram of the TROM is presented in Figure 1.

3.1 Input Protection Circuit

The input protection circuitry used in the TROM is the standard diode-based input protection pad described in many VLSI textbooks. It is a well-tested cell since it has been used successfully in many other integrated circuit projects at Queen's. This cell is part of Q'CELL, the Queen's University double metal standard cell library [QUEE87].

3.2 The Address to Memory Matrix Decoding Subsystem

This subsystem decodes the seven trit address to a particular row in the memory subsystem and a particular bit line. The address is divided into two parts. The lower four trits are used to determine the row address and the upper three trits are used for the determination of the trit line.

The ternary logic functions are implemented with variable geometry circuits. An example using inverters is shown in Figure 2.

The four address lines used in the row decoding are converted to twelve lines by four one-to-three decoders, as shown in Figure 3. These twelve lines are used by another set of decoders to actually select the row. Since the output of the one-to-three decoders is binary, binary circuits are used for this further level of decoding.

The row decoding from the twelve signal lines is accomplished by a static CMOS row decoder (Figure 4). It is a four input system, and is composed of two binary NAND gates and a binary NOR gate. The static decoder allows the chip enable to control the output. This is preferable when testing the TROM. The two different decoders are assembled as shown in Figure 5.

There are three address lines reserved for selecting the column of the ROM matrix, i.e. the trit line. These three address lines are passed through one-to-three decoders to obtain nine lines. The nine lines control a tree decoder structure, which is used to select the correct trit line from the twenty-seven available for each bank.

3.3 The Memory Matrix

The memory matrix has been one of the major design problems in multi-valued ROMS. The choice of the memory matrix determines the sense amplifiers required, the necessary references and the programming method.

The other multi-valued ROM designs have used either variable geometry transistors or variable threshold voltages. The CMOS process available to Queen's does allow a variable threshold process. Thus the TROM design was initially to use variable geometry transistors.

The variable geometry approach to memory cell design has flaws [ADLH85]. The most important

objection is the balancing of the pullup transistor to the pulldown transistor. A set of dimensions has to be determined for at least two of the three states. Also, to improve the reliability of the device, reference cells have to be included in the matrix, resulting in less cost-effective memory area.

The symmetry of the ternary logic levels allows the use of the memory cell design used in this TROM. Unlike the four valued ROM cells, a ternary memory cell has to provide two levels other than the high logic level. Therefore a contact programmed ROM, where the pulldown transistor is connected to either the middle or low logic level, can be used.

An important factor in the design is the problem of programming the TROM. For this TROM, all the programming is done manually. The programming task is tedious and therefore prone to error. The contact programming method requires the minimum number of steps per cell.

A further extension to this TROM design is the use of shared transistors. The trit lines are passed between two transistors, one of which is connected to the ground and the other to the negative potential. The contact to the trit line is made to one transistor if the zero level is desired from the cell, and to the other transistor if the low level is required. This strategy is shown in Figure 6. This required the use of large load transistors, which slows the charging of the trit line.

When two adjacent trit lines are to have the same value for a given row, then the transistor between the trit lines is shared,if possible. Since the majority carrier mobility of the pulldown transistor is approximately three times the majority carrier mobility of the pullup p-type transistor, the correct logic level is delivered from the cell despite having to sink double the current of the single trit line case.

The transistors in the memory matrix are all of minimum size. In the 3 micron process being used, the n-type transistor is 3 microns by 3 microns. This results in a very compact matrix. Realizing a TROM using variable geometry would result in a considerable increase in the usage of area. The transistors are interleaved, resulting in an efficient layout. An example layout is presented in Figure 7.

The p-type transistors which are used as loads on the trit lines are 33 microns long by 3 microns wide. These transistors are always on, keeping the trit lines charged to +3 volts.

The resulting geometry in the TROM uses five banks of these memory elements. Each bank is composed of 2248 transistors, arranged in 81 rows, each of 28 transistors. Twenty-seven trit lines are located in each of these banks. Each trit line is connected to a p-device load transistor. This results in a total of 2187 trits per bank.

3.4 Sense Amplifier Subsystem

The sense amplifier used in the TROM is the one-to-three decoder. This is the same circuit used in the address decoders and has good characteristics for a single ended sense amplifier. Single ended sense amplifiers may cause problems if the output of the memory matrix is far from the designed logic levels. This may happen due to some variation in the fabrication process for the particular lot. This is the main reason for the large p- transistor loads.

3.5 Output Subsystem

ROMs are to be connected on data busses. The TROM must have some way of isolating the bus from the random outputs of the memory matrix. This is provided by a quadstate device, which is analogous to the tristate driver in binary systems. The high resistance state occurs when the chip enable signal is high.

The basic structure for the quadstate centers around the sense amplifier. The one-to-three decoder has converted the output of the memory matrix into a high level on one of three outputs from the decoder. These are combined with a positive enable signal. The combinational circuit is based on a NAND gate and an inverter for the low and middle logic drivers. A NAND gate is used for the positive voltage driver.
As shown in Figures 8a and 8b, the output of the combinational circuit activates the voltage drivers. These are transistors connected to the power rails and sized to deliver sixteen times the current drive of a minimum sized inverter.

A metallization plot of the complete chip is presented in Figure 9.

4. SUBSYSTEM SIMULATION

An important part in the VLSI design methodology is the simulation of the circuits incorporated into the chip. To simulate the TROM, two simulators were used.

Early in the design stage, much of the control logic verification was carried out by QUAIL, the Queen's University Asynchronous Interactive Logic simulator. It is capable of handling multiple-valued functions. QUAIL simulated the decoder logic in the TROM.

SPICE is still used at the circuit level. The ROM matrix and a sample system have been simulated. The SPICE deck has been extracted from the layout.

The simulation of the decoder logic and the sample system are presented in Figure 10. This simulation also includes the estimated capacitance of the trit line. The SPICE parameters for the Northern Telecom CMOS3DLM process are listed in Appendix 1 [CMC87]. Memory output voltage levels are provided in Appendix 2.

5. CONCLUSIONS

This paper has described a design for a ternary read-only memory. It has a memory capacity of 2187 five trit words. This is addressed by seven three-level address inputs. This device fits into a 0.45x0.45 cm die.

It is difficult to compare the TROM with a binary ROM. The TROM has a considerable advantage in the number of states per memory cell. But the binary ROM structures tend to be more area-efficient. The compression of the TROM matrix is one area for

further investigation.

This design will be used in future chip implementations of ternary logic systems where read only memory is necessary. One plan being currently developed is to interface the chip- based ROM with the ternary computer QTC-1 [MOUF84]. This will allow the continued development of an integrated circuit ternary microprocessor.

6. REFERENCES

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APPENDIX 1

CMOS3DLM Spice Parameters

SPICE Model Parameters used in the simulation.

```
.MODEL N NMOS (LEVEL=1 VTO=0.7 KP=40E-6 GAMMA=1.1
PHI=0.6 + LAMBDA=0.01 PB=0.7 CGSO=3.0E-10
CGDO=3.0E-10 CGBO=5.0E-10 + RSH=25 CJ=4.4E-4 MJ=0.5
CJSW=4.0E-10 MJSW=0.3 JS=1.0E-5 + TOX=5.0E-8
NSUB=1.7E16 TPG=1 XJ=6.0E-7 LD=3.5E-7 UO=775 )

.MODEL P PMOS (LEVEL=1 VTO=-0.8 KP=12E-6 GAMMA=0.6
PHI=0.6 + LAMBDA=0.03 PB=0.6 CGSO=2.5E-10
CGDO=2.5E-10 CGBO=5.0E-10 + RSH=80 CJ=1.5E-4 MJ=0.6
CJSW=4.0E-10 MJSW=0.6 JS=1.0E-5 + TOX=5.0E-8
NSUB=5.0E15 TPG=1 XJ=5.0E-7 LD=2.5E-7 UO=250 )
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APPENDIX 2

Memory Cell Output Voltage Levels

Low Level (Single P-Load) -2.993 V

Middle Level (Single P-Load) 1.493E-2 V

Low Level (Shared P-Loads) -2.986 V

Middle Level (Shared P-Loads) -2.992E-2 V

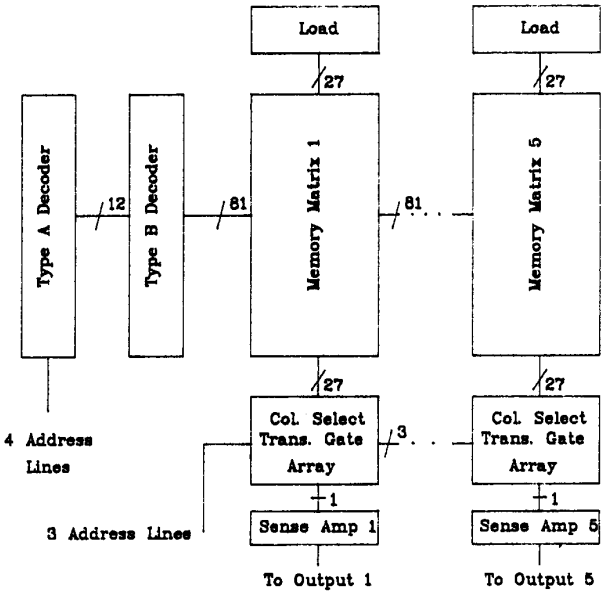
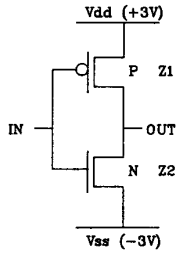


Figure 1. Block Diagram of the TROM



Width to Length Ratios

Basic Gates	Z1	Z2
PTI	7	1
NTI	0.5	1
SBI	3	1

PTI Positive Ternary Inverter
NTI Negative Ternary Inverter
SBI Standard Binary Inverter

Figure 2. Variable Geometry Inverters

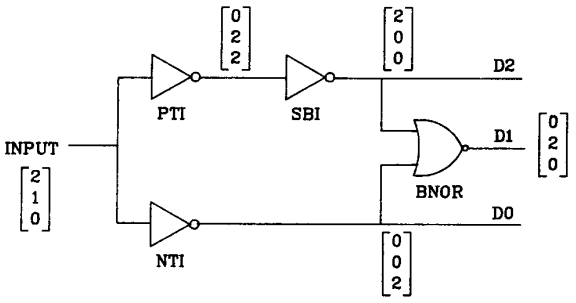


Figure 3. Type A Decoder
– One to Three Decoder –

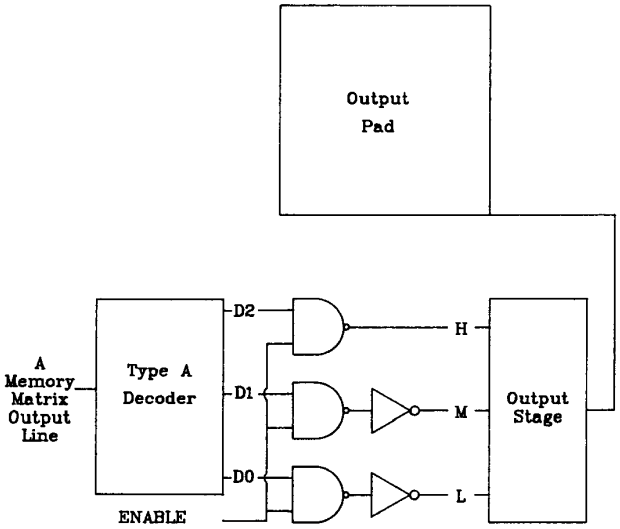


Figure 8a. Logic Schematic of the Quadstate Driver

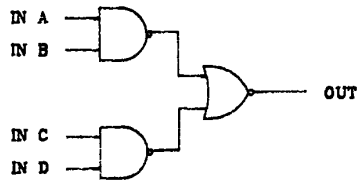


Figure 4. Type B Decoder

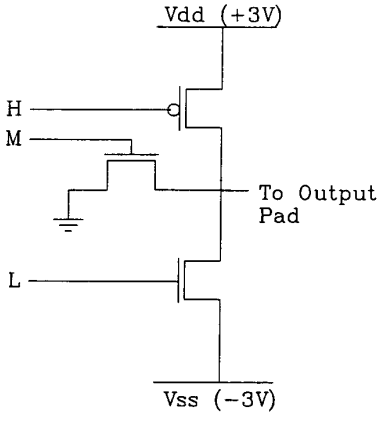


Figure 8b. Output Stage of the Quadstate Driver

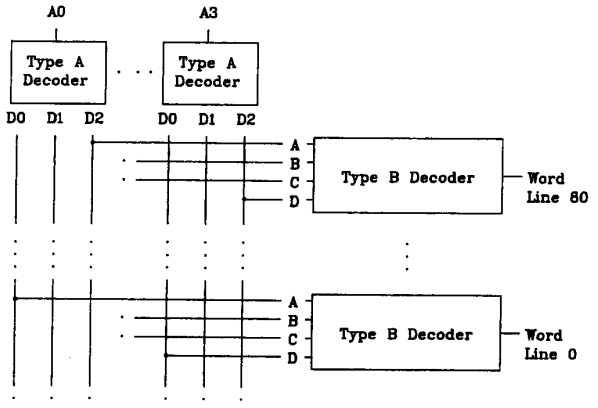


Figure 5. Complete Decoder Arrangement

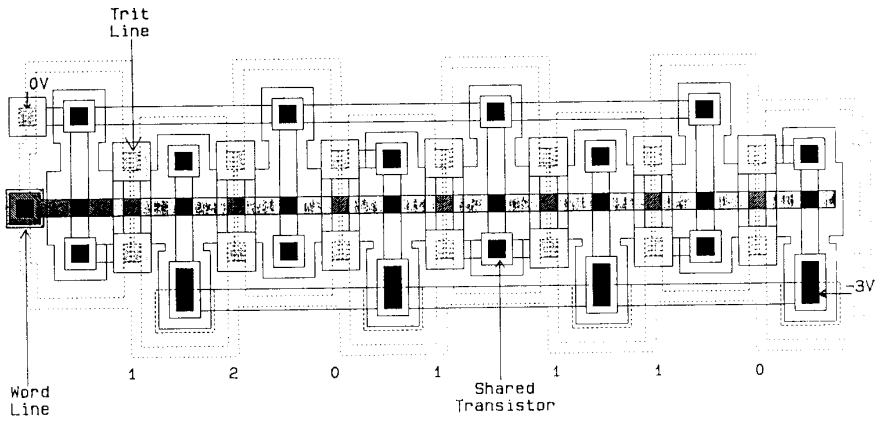


Figure 7. Example Layout of Programmed TROM Memory Cells

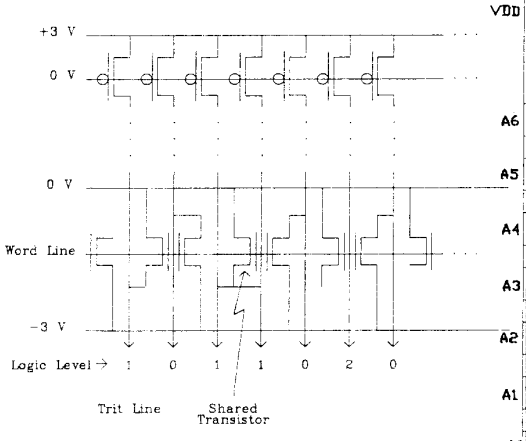


Figure 6. TROM Memory Cell Arrangement

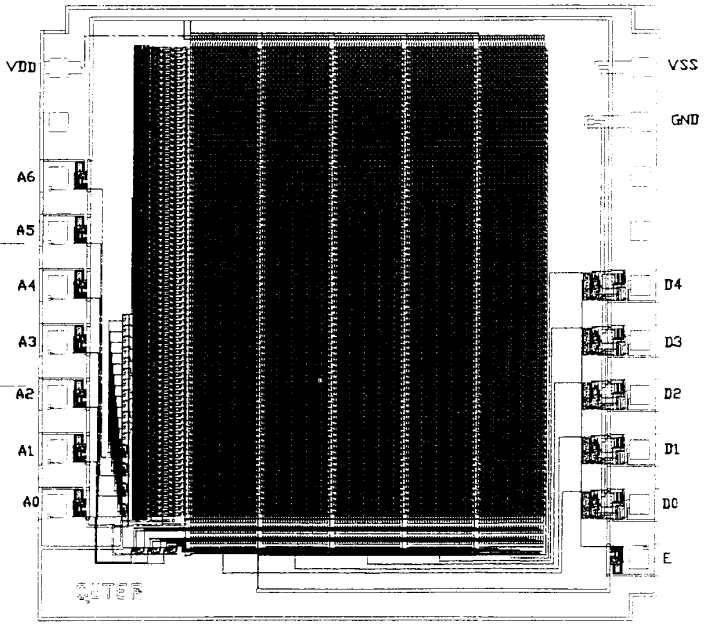


Figure 9. Metallization Plot of the TROM (4510 x 4510 microns)

A0 – A6	Input Address Lines
D0 – D4	Output Data Lines
E	Enable
VDD, VSS, GND	+3V, −3V, 0V

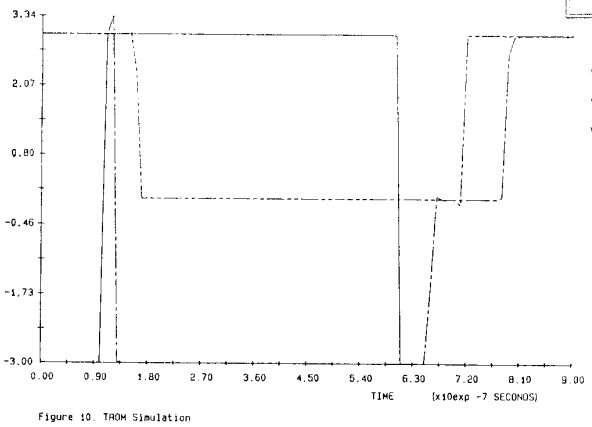


Figure 10. TROM Simulation