2. Elementary Electronic Circuits with a BJT Transistor

Our main aim in the two next lectures is to build *all* the possible *practical* circuits (amplifiers) by using a BJT transistor and a resistor. (We use the resistor to translate the output current of the circuit into voltage; otherwise the circuit will not be able to provide a voltage gain.) We then analyze and compare the circuits' small-signals gains to understand for what applications they can be suitable. We are particularly interested in the applications where there is a need to amplify power and dc signals.

In this lecture, we develop all the models for the transistors – as we did this for the diode – and then will build and analyze – with the help of these small-signal models – all the possible single-transistor amplifiers.

2.1. *BJT transistor: symbol, physical structure, analytical model, and graphical characteristics*

The symbols of the *npn* and *pnp* BJT transistors and the physical structure of the *npn* transistor are given in Fig. 1. We will analyze in the lectures only *npn* transistors. The only difference between the *npn* and *pnp* transistors is in their static states: the static state of the *pnp* transistors is reverse to that of the *npn* ones because of their opposite structures. There will be no difference in the small-signal behavior and models. The circuits analyzed in home exercises, the lab, and the exam *will* comprise both *npn* and *pnp* transistors.

In analog circuits, the operating point of transistors is usually defined in active (linear) region, where the emitter junction is forward biased and the collector junction is reverse biased. Thus, the emitter *injects* the electrons into the base, and the collector *collects* them. The amount of the injected electrons is controlled by the emitter-base voltage, v_{BE} (or base-to-emitter current, i_B). The collector collects almost all the electrons from the base if its potential is sufficiently high: is greater or equal to that of the base. The base is very thin and the electrons prefer entering the collector – even its potential equals that of the base – and not the base, because the resistance that they see looking into the base is much greater than that they see looking into the collector.

To define the operating point of the transistor in active region, we ground the emitter and bias the transistor junctions with a current and voltage source as shown in Fig. 1. A single transistor circuit (with no other components, except independent sources) with grounded emitter is called the common-emitter configuration. Although we develop all the models of the transistor for the common-emitter configuration, they can also be used (see the Appendix) for any transistor in a circuit, no matter which terminal of the transistor is grounded (if at all).

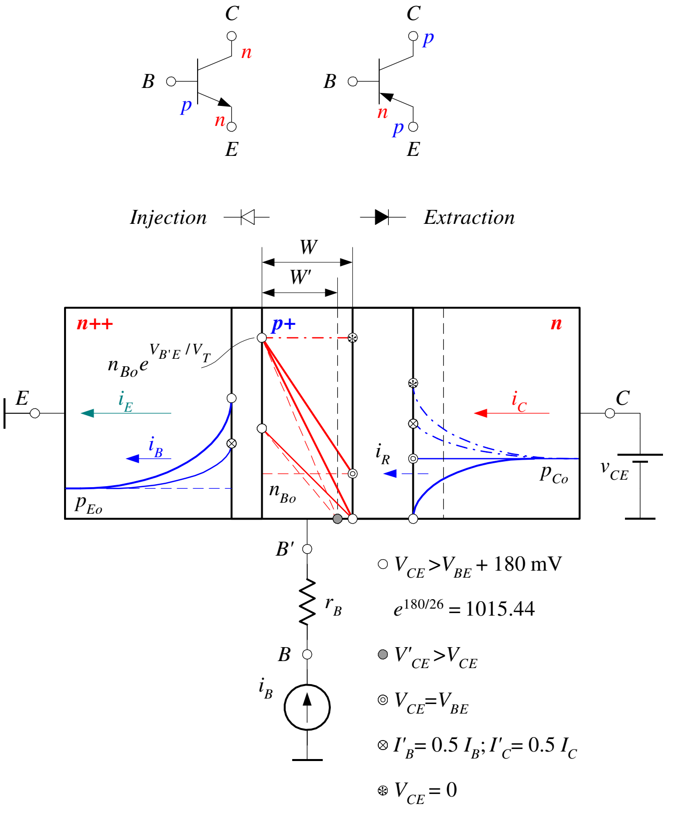

Fig. 1. Symbol of the *n-p-n* and *p-n-p* BJT transistors and the physical structure of the *npn* transistor. Note that for a fixed i_B, v_{BE} is also fixed.

Analytical model: transistor equations

Let us first write the equations for the transistor current based on the concentrations of the minor charge carriers in Fig. 1:

$$\left|i_C\right| = D_n \left|q\right| \frac{n_{Bo} e^{v_{B'E}/V_T}}{w} A_{BE} + i_R \Bigg|_{i_C >> i_R}$$

$$= \underbrace{D_n \left|q\right| \frac{n_{Bo}}{w} A_{BE}}_{I_{CS}} \, e^{v_{B'E}/V_T} = I_{CS}\, e^{v_{B'E}/V_T} \quad . \qquad (1)$$

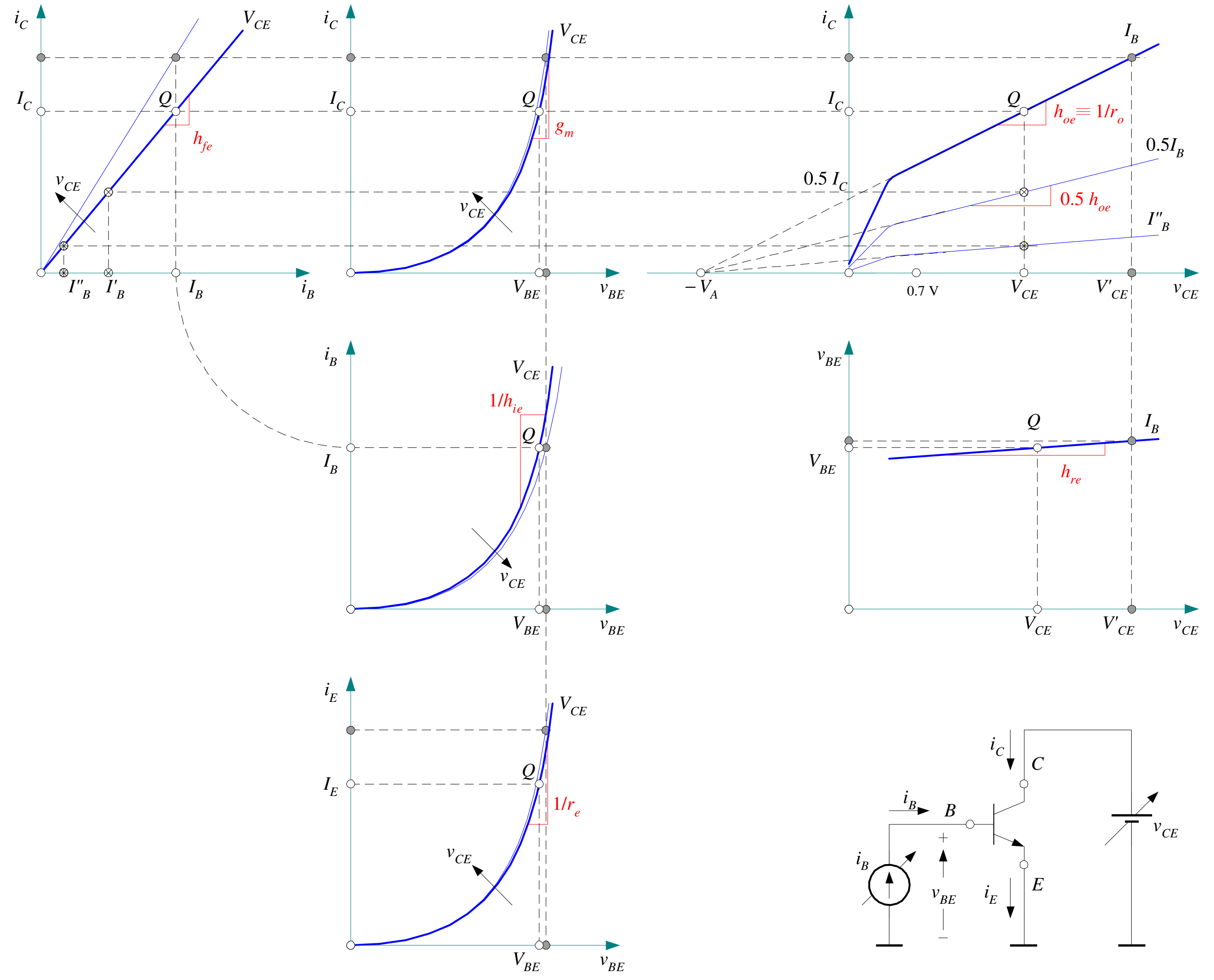

Fig. 2. Common-emitter characteristics of an *npn* transistor.

$$\left|i_B\right| = \underbrace{\frac{D_p |q| A_{B'E}\, p_{Eo}}{L_{pE}}}_{I_{BS}} \left(e^{v_{BE}/V_T} - 1\right)\Bigg|_{i_B >> i_{BS}} = I_{BS}\, e^{v_{B'E}/V_T} \quad . \tag{2}$$

$$\left|i_E\right| = i_C + i_B = I_{CS}\, e^{v_{B'E}/V_T} + I_{BS}\, e^{v_{B'E}/V_T} = \underbrace{(I_{CS} + I_{BS})}_{I_{ES}}\, e^{v_{B'E}/V_T} = I_{ES}\, e^{v_{B'E}/V_T} \quad . \tag{3}$$

We now can define the static current gains

$$\beta_F \equiv \frac{i_C}{i_B} = \frac{D_n |q| \frac{n_{Bo}}{w} A_{BE}\, e^{v_{B'E}/V_T}}{\frac{D_p |q| A_{BE}\, p_{Eo}}{L_{pE}}\, e^{v_{B'E}/V_T}} = \frac{D_n n_{Bo} L_{pE}}{D_p\, p_{Eo} w}\Bigg|_{n_{Bo} >> p_{Eo};\, L_{pE} >> W} >> 1 \tag{4}$$

and

$$\alpha_F \equiv \frac{i_C}{i_E} = \frac{i_C}{i_B + i_C} = \frac{i_C / i_B}{1 + i_C / i_B} = \frac{\beta_F}{1 + \beta_F}\Bigg|_{\beta_F >> 1} \to 1 \quad . \tag{5}$$

Note that according to (4), the transistor i_C-i_B characteristic should be a linear one (see Fig. 2), of course, provided that β_F is constant (in a real transistor, β_F depends on i_B, but we will neglect this in our theory). It is also apparent from (1)-(3) that the i_C-v_{BE}, i_B-v_{BE}, and i_E-v_{BE} characteristics are exponential.

Since according to (1), the collector current is a function of the base width, w, and w decreases with increasing v_{CE}, the transistor output characteristics have a slope that is proportional to I_C. (This is unlike the Ebers-Moll model, where the transistor output characteristics are horizontal.) Indeed,

$$\left|\frac{\partial i_C}{\partial w}\right|_Q = \left|\frac{\partial\left(D_n|q|\dfrac{n_{Bo}}{w}A_{BE}e^{v_{B'E}/V_T}\right)}{\partial w}\right|_Q$$

$$= \frac{1}{W}D_n|q|\frac{n_{Bo}}{W}A_{BE}e^{V_{B'E}/V_T} = \frac{1}{W}I_C$$

$$\Rightarrow |\partial i_C| = \left|\frac{\partial w}{W}I_C\right|. \qquad (6)$$

For $\left|\dfrac{\partial w}{W}\right| \propto \left|\dfrac{\partial v_{CE}}{V_{CE}}\right|$:

$$|\partial i_C| = \frac{\partial v_{CE}}{V_{CE}}I_C \Rightarrow |\partial i_C| \propto |I_C|.$$

Due to the linear dependence of the slope of the output characteristics on I_C, their extrapolations meet at the one and the same point on the v_{CE} axis, so-called Early voltage, V_A.

When v_{CE} increases, the base width w decreases, and the base resistance, r_B, increases. Therefore, the static V_{BE} voltage should increase for the same static bias current I_B (see the i_B-v_{BE} and v_{BE}-v_{CE} characteristics in Fig. 2). As a result, the i_B-v_{BE}, characteristic decreases a bit with increasing V_{CE}. Since decreasing w causes much more substantial increase in i_C and i_E than in v_{BE}, the i_C-v_{BE} and i_E-v_{BE} characteristics increase with increasing v_{CE}.

The effect associated with the change (modulation) of the base width by the collector voltage, v_{CE}, and with the corresponding behavior of the transistor characteristics is called Early effect.

Small-signal parameters

Having all the needed transistor characteristics, we can define the small-signal gains as the slopes of the characteristic at their operating points.

The small-signal current gains

$$h_{fe} \equiv \left.\frac{i_c}{i_b}\right|_{Q,\,v_{ce}=0} = \beta_F\,, \qquad (7)$$

$$\alpha_f \equiv \left.\frac{i_c}{i_e}\right|_{Q,\,v_{ce}=0} = \left.\frac{i_c}{i_b+i_c}\right|_{Q,\,v_{ce}=0} = \left.\frac{i_c/i_b}{1+i_c/i_b}\right|_{Q,\,v_{ce}=0} \quad . \qquad (8)$$

$$= \frac{h_{fe}}{1+h_{fe}} = \frac{\beta_F}{1+\beta_F} = \alpha_F$$

The small-signal conductance and resistance of the emitter

$$\frac{1}{r_e} \equiv \left.\frac{i_e}{v_{b'e}}\right|_{v_{ce}=0} = \frac{I_{ES}e^{V_{B'E}/V_T}}{V_T} = \frac{I_E}{V_T} \quad . \qquad (9)$$

$$r_e = \left.\frac{V_T}{I_E}\right|_{300^\circ\,\mathrm{K},\,I_E=1\,\mathrm{mA}} = 26\,\Omega$$

The small-signal (mutual) conductance gain

$$g_m \equiv \left.\frac{i_c}{v_{b'e}}\right|_{Q,\,v_{ce}=0} = \frac{I_{CS}e^{V_{B'E}/V_T}}{V_T} = \frac{I_C}{V_T}, \quad . \qquad (10)$$

$$g_m \equiv \left.\frac{i_c}{v_{be}}\right|_{v_{ce}=0} = \left.\frac{\alpha_f\,i_e}{v_{b'e}}\right|_{v_{ce}=0} = \frac{\alpha_f}{r_e}$$

The small-signal input conductance and resistance

$$\frac{1}{h_{ie}} \equiv \left.\frac{i_b}{v_{b'e}}\right|_{v_{ce}=0} = \left.\frac{i_c/h_{fe}}{v_{be}}\right|_{v_{ce}=0} = \left.\frac{\alpha_f\,i_e/h_{fe}}{v_{be}}\right|_{v_{ce}=0}$$

$$= \left.\frac{i_e}{(1+h_{fe})v_{b'e}}\right|_{v_{ce}=0} = \frac{1}{(1+h_{fe})r_e}; \quad . \qquad (11)$$

$$h_{ie} = (1+h_{fe})r_e\big|_{300^\circ\,\mathrm{K},\,I_E=1\,\mathrm{mA},\,h_{fe}=100} = 2.6\,\mathrm{k}\Omega$$

The small-signal output conductance and resistance ("*r-out*", not "*r-zero*")

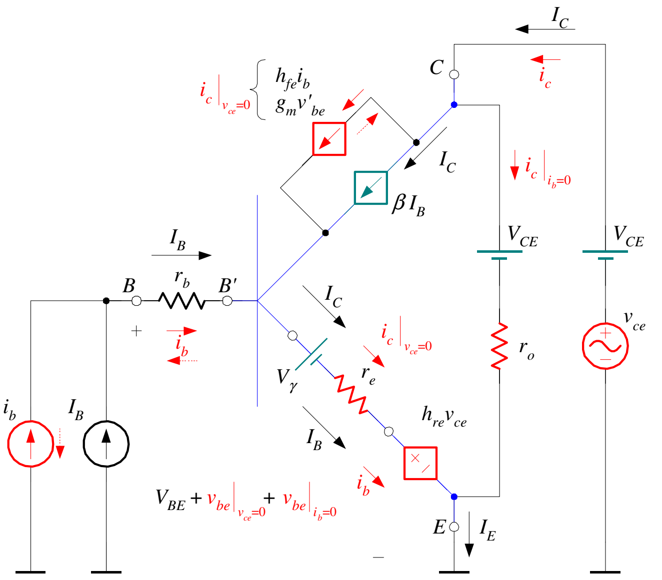

Fig. 3. "Large"-signal equivalent circuit (model) for the transistor. Note that another V_{CE} source is added to cancel the effect of the static collector-to-emitter voltage, V_{CE}, on the current through r_o. Thus, only the small-signal collector-to-emitter voltage, v_{ce}, generates the small-signal current through r_o, which is in accordance with the Early effect. Note also that alternating the polarity of the v_s source causes the corresponding alternating the polarity of the $h_{fe}i_b$ source.

$$h_{oe} \equiv \frac{1}{r_{oe}} \equiv \left.\frac{i_c}{v_{ce}}\right|_{Q,\, i_b=0} = \frac{I_C}{V_A + V_{CE}} \quad . \qquad (12)$$

$$r_o = \left.\frac{V_A + V_{CE}}{I_C}\right|_{I_C = 1\text{ mA},\, V_A = 100\text{ V} >> V_{CE}} = 100\text{ k}\Omega$$

And finally, the small-signal reverse-voltage gain

$$h_{re} \equiv \left.\frac{v_{b'e}}{v_{ce}}\right|_{Q,\, i_b=0} \quad . \qquad (13)$$

"Large"-signal model for the transistor

To develop a "large"-signal model (see Fig. 3) for the transistor, we first replace the base-emitter diode with the "large"-signal model of the diode, add the βI_B dependent source (this completes the static signal translation), and then add the $h_{fe}i_b$, or what is the same $g_m v_{be}$ dependent source to represent the effect of v_{be} on i_c, add r_o together with an additional independent voltage source V_{CE} to represent the effect of v_{ce} on i_c, and finally add the $h_{re}v_{ce}$ source to represent the effect of v_{ce} on v_{be}. Note that we add another V_{CE} source to cancel the effect of the static collector-to-emitter voltage, V_{CE}, on the current through r_o. Only the small-signal collector-to-emitter voltage, v_{ce}, should generate the small-signal current through r_o, which is in accordance with the Early effect.

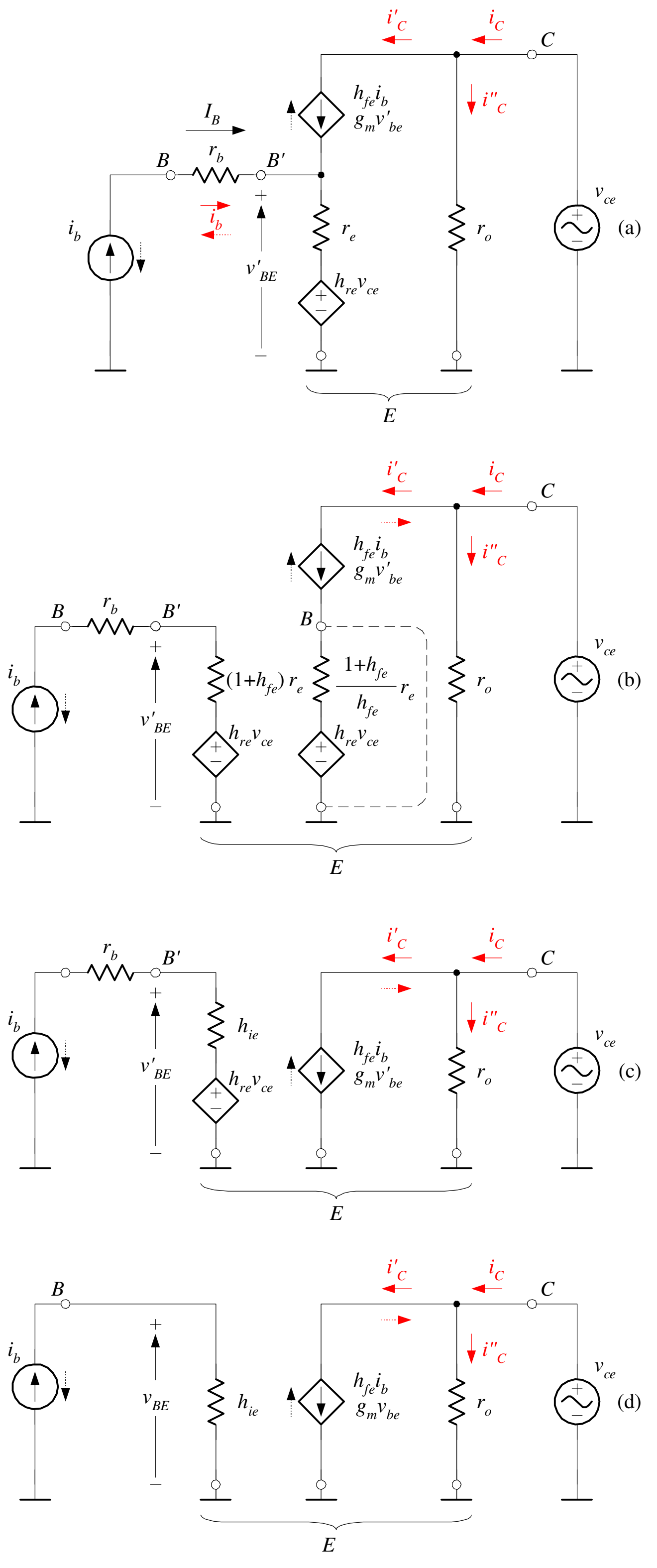

Fig. 4. Small-signal equivalent circuits (models) for the transistor. (a) *T* small-signal model of the BJT transistor, (b) separating the input and output loops of the *T* model by applying the Miller theorem, (c) hybrid-π small-signal model, (d) simplified hybrid-π model with the $h_{re}v_{ce}$ source and r_b neglected.

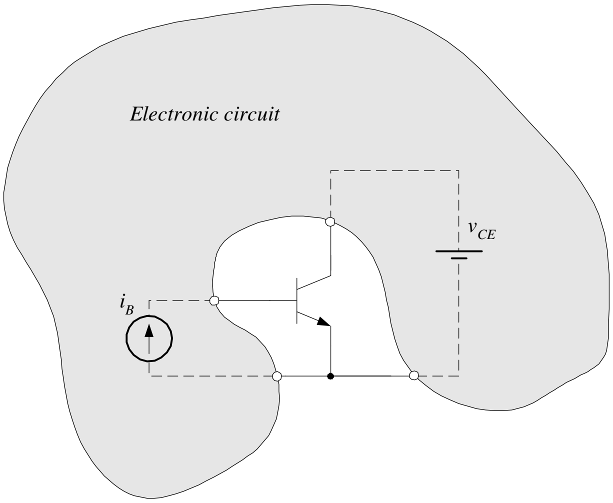

Fig. A1. Transistor in an arbitrary electronic circuit connected to equivalent signal sources. According to the *substitution theorem*, a branch of the network that is not coupled to other branches can be replaced by an equivalent independent current or voltage source without affecting any other branch current or branch voltage. To apply the substitution theorem, the network has to have a unique solution for all its branch currents and branch voltages. The network does not have to be linear.

Small-signal model for the transistor

Note that the circuit in Fig. 3 is a linear one. Hence, to obtain a small-signal model for the transistor [see Fig. 4(a)], we simply suppress all the static sources in Fig. 3. The circuit in Fig 4(a) is called the T small-signal model of the BJT transistor.

The T model can be simplified by separating its input and output loops [see Fig. 4(b)] by applying the Miller theorem for currents (see the Appendix). Such a separation provides us with so-called hybrid-π small-signal model shown in Fig 4(c). Note that in Fig. 4(b) we short-circuited the resistor and the voltage source that are connected in series with the $h_{fe}i_b$ source. We can omit these two components because they do not affect the $h_{fe}i_b$ source and, therefore, do not affect the model output voltage and current: v_{ce} and i_c.

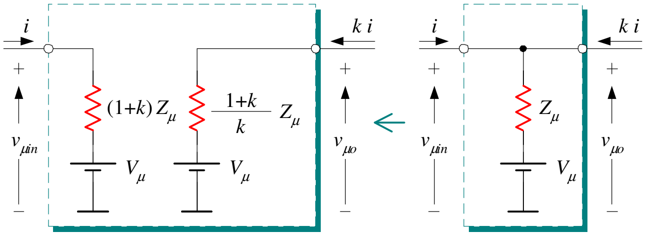

Fig. A2. Miller's theorem (for currents).

Neglecting the $h_{re}v_{ce}$ source (the typical value of h_{re} is very small, about 10^{-3}), we obtained in Fig. 4(d) a simplified hybrid-π model. We will use this model in all our further analysis.

Either the T or π models can be used in a small-signal analysis to replace a transistor in an electronic circuit. Naturally, all the small-signal parameters of the models should be found in advance as a function of the transistor operating point.

APPENDIX

Fig A1 illustrates that the effect of the electronic circuit on a transistor can be modeled with two independent sources.

Fig. A2 illustrates the Miller theorem for currents: the input and output loops of a T network can be separated without changing the states of the network ports if the values of the impedances $Z_{\mu in}$ and $Z_{\mu o}$ are increased to compensate for the reduction of the currents through them relative to the current in the impedance Z_μ of the original T network.

REFERENCES

[1] J. Millman and C. C. Halkias, Integrated electronics, McGraw-Hill.
[2] A. S. Sedra and K. C.Smith, Microelectronic circuits.