4. Biasing Transistor Circuits

Our main aim is to analyze the drawbacks of the bias in the elementary transistor circuits and to suggest a better solution for both discrete and integrated electronic circuits.

2.1. *Drawbacks of the bias in the elementary transistor circuits*

The elementary biasing has the two following main drawbacks.

Excessive use of static sources

The first drawback is related to the need to use too many static signal sources in multi-stage electronic circuits. The V_{BE} source in Fig. 1(a) is not *universal*: it cannot be used for biasing other stages. Transistors in other stages may need a different base-emitter voltage, either due to the difference in their parameters or the difference in their static states. It is also a complex task to connect a single V_{BE} source to a number of stages and to decouple it from individual signal sources in each stage.

Thermal instability

The second drawback of the elementary biasing is related to its thermal instability caused by:

$\delta\beta_F$=0.1 – 0.3%/°C,

ΔV_{BE}=–2 mV/°C [see Fig. 1 (b)],

δI_{CBo}=100%/10°C [see Fig. 1 (c)],

where δ denotes the relative change, Δ denotes the absolute change in the corresponding variable, and I_{CBo} is the leakage current due to the discontinuity of the semiconductor just beneath its surface [see Fig. 1(c)].

The silicon atoms that are located just beneath the surface do not have neighbors above them. As a result, each of them has a vacancy that can be used by electrons to travel from atom to atom. The typical value of the leakage current is below 100 pA. (It is obvious that the leakage current is proportional to the voltage between the terminals, there is no leakage if there is no difference between the electrical potential of the terminals.)

To consider the leakage current we add in Fig. 1(d) an I_{CBo} source to the ideal, leakage-free transistor. Note that we consider only the leakage current of the reverse biased C-B junction and do not consider the leakage current of the forward biased B-E junction. This is because both the static and dynamic impedances of a forward biased junction are relatively low, and the connected in parallel relatively high

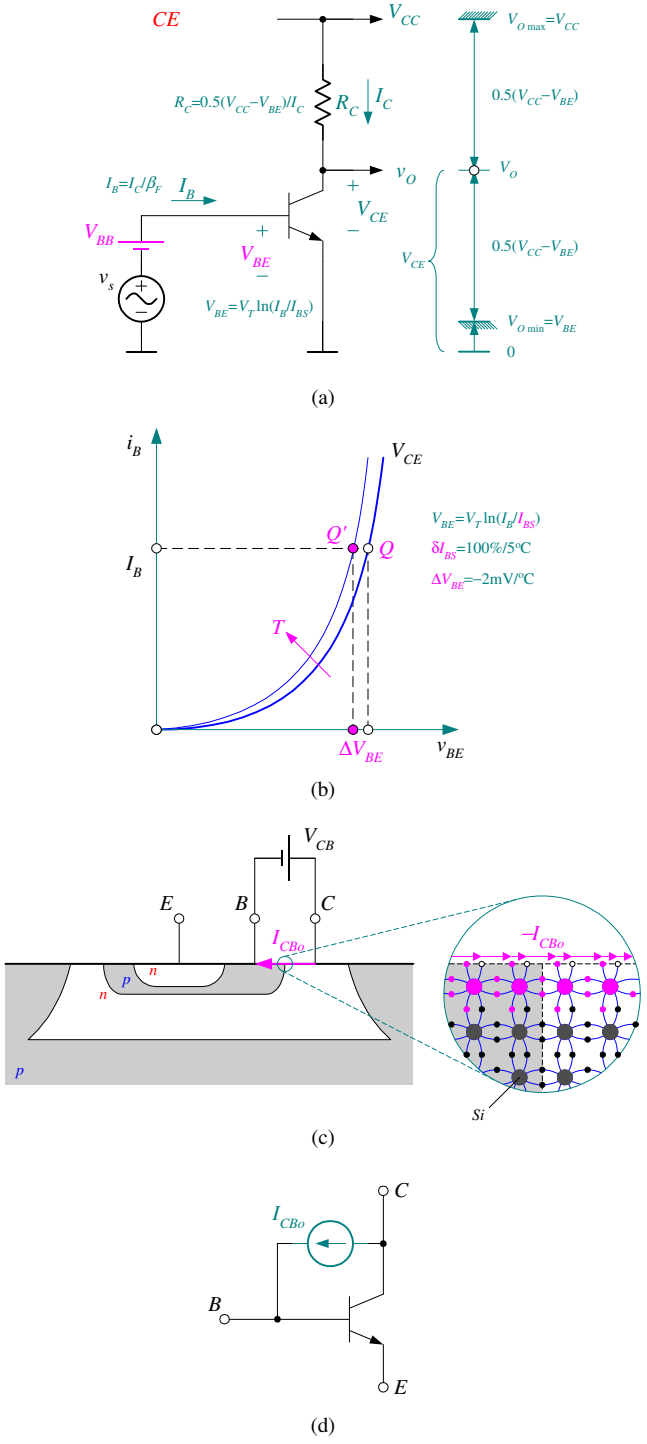


Fig. 1. Biasing the elementary CE amplifier. (a) Circuit. (b) The dependence of V_{BE} on temperature (for a fixed I_B). (c) The leakage current I_{CBo} due to the discontinuity of the semiconductor just beneath its surface. (d) Including the leakage current into the transistor model.

leakage impedance can be neglected.

2.2. *Biasing practical discrete circuits*

Discrete circuits are assembled from separate components, each manufactured by special technology. There are no principal limitations, and the designer can enjoy the possibility of using the wide variety of components, their values, and tolerances. However, the principal disadvantage of the discrete design is the impossibility of using identical transistors (see Section 2.3).

To improve the elementary biasing the following is usually done in the design of discrete circuit. To get rid of the non-universal source V_{BE}, it is simply replaced [see Fig. 2(a)] by a voltage divider R_{B1}, R_{B2}, and the signal source v_s is connected to the circuit via a coupling capacitor C_C. (Note that otherwise the v_s source would ground the static voltage of the transistor base. Note also that the coupling capacitor does not let us amplify dc small signals. It may be a serious drawback if we do have to amplify them.)

To increase the thermal stability of the bias, a feedback resistor R_E is connected between the emitter of the transistor and the ground. If now the collector current will rise with transistor temperature, I_E and, hence, V_E=$I_E R_E$ will rise as well. For a constant V_{BB} and nearly constant V_{BE}, increasing V_E will increase V_B, decrease the voltage across R_B, decrease I_B, and hold back in this way the rise of the collector current (negative feedback). In order not to let R_E to hold back the ac small-signal collector current, a bypass capacitor C_B is connected in parallel to R_E.

To analyze the thermal stability — the sensitivity of I_C to $\beta_F(T)$, $V_{BE}(T)$, and $I_{CBo}(T)$ — of the circuit in Fig. 2(a), we first apply the Thévenin theorem to V_{CC}, R_{B1}, and R_{B2}. The result is shown in Fig. 2(b). We now can easily find

$$I_C = \beta_F I'_B + I_{CBo}\,. \tag{1}$$

$$V_{BB} = (1+\beta_F)\, I'_B\, R_E + V_{BE} + (I'_B - I_{CBo})R_B$$

$$\Rightarrow \tag{2}$$

$$I'_B = \frac{V_{BB} - V_{BE} + I_{CBo}R_B}{(1+\beta_F)R_E + R_B}$$

$$I_C = \beta_F \frac{V_{BB} - V_{BE} + I_{CBo}R_B}{(1+\beta_F)R_E + R_B} + I_{CBo}$$

$$= \frac{\beta_F (V_{BB} - V_{BE}) + (1+\beta_F) I_{CBo}(R_E + R_B)}{(1+\beta_F)R_E + R_B} \tag{3}$$

The sensitivity of I_C to $I_{CBo}(T)$, $V_{BE}(T)$, and $\beta_F(T)$ can be found as follows:

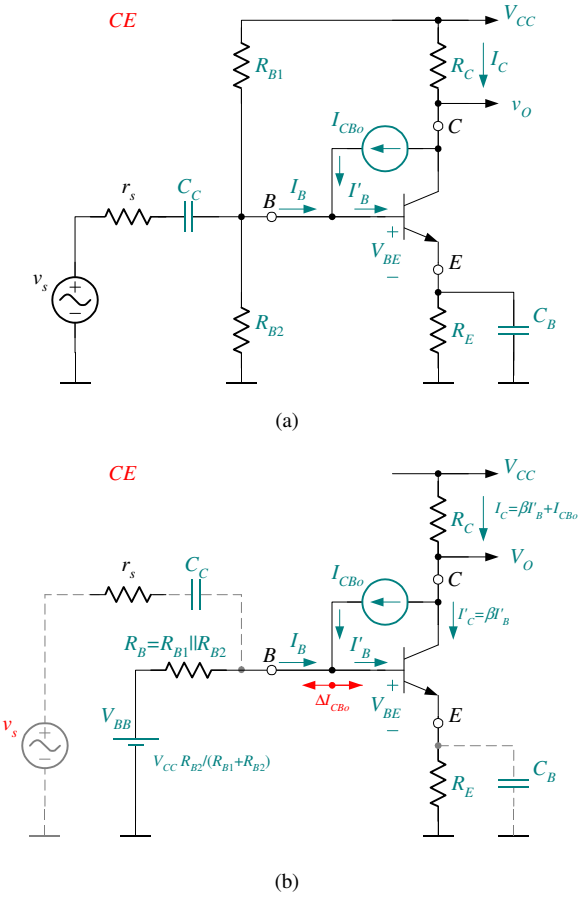


Fig. 2. Biasing discrete circuits. (a) A practical circuit and (b) its equivalent for finding the static state after applying the Thévenin theorem to V_{CC}, R_{B1}, and R_{B2}.

$$\Delta I_C \approx \frac{\partial I_C}{\partial I_{CBo}}\Delta I_{CBo} + \frac{\partial I_C}{\partial V_{BE}}\Delta V_{BE} + \frac{\partial I_C}{\partial \beta_F}\Delta\beta_F$$

$$= S_I \Delta I_{CBo} + S_V \Delta V_{BE} + S_\beta \Delta\beta_F \tag{4}$$

where S_I, S_V, and S_β are the sensitivity factors giving the sensitivity of I_C to $\beta_F(T)$, $V_{BE}(T)$, and $I_{CBo}(T)$, respectively.

$$S_I = 1 + \left.\frac{\beta_F \breve{R}_B}{\breve{R}_B + (1+\beta_F)R_E}\right|_{R_B\to 0} = S_{I\min} = 1$$

$$S_V = \left.\frac{-\beta_F}{\breve{R}_B + (1+\breve{\beta}_F)\breve{R}_E}\right|_{R_E\to\infty} = S_{V\min} \tag{5}$$

$$S_\beta = \left.\frac{(V_{BB} - V_{BE} + I_{CBo}R_B)(R_B + R_E)}{[R_B + (1+\breve{\beta}_F)\breve{R}_E]^2}\right|_{\substack{R_E\to\infty \\ \beta\to\infty}} = S_{\beta\min}$$

Note that both S_V and ΔV_{BE} in (4) are negative, therefore, ΔI_C

due to ΔV_{BE} is positive.

The sensitivity factors in (5) should approach their minima to improve the bias thermal stability. One can see that this is obtained when $R_B \to 0$ (we denote this as $\breve{R}_B$), and $\beta_F \to \infty$, $R_E \to \infty$ (we denote this as $\hat{\beta}_F$ and $\hat{R}_E$). Decreasing R_B decreases the part of the leakage current increment, ΔI_{CBo}, entering the transistor base. Increasing β_F and R_E increases the negative feedback through R_E.

We cannot use too small R_B because this equivalent resistance not only shortens some part of the leakage current to ground but also does the same to the input signal [see Fig. 2(b)]. In a practical circuit we can only use transistors with limited β_F and cannot use too great R_E. The voltage drop across too great R_E reduces too much the range of the output voltage (see Fig. 3).

A general compromise for choosing R_B and R_E is as follows:

$$\begin{cases} I_{R_{B2}} = 10 \cdot I_B \\ \\ I_E R_E = 0.1\ V_{CC} \end{cases} . \qquad (6)$$

Example circuits

Fig. 3 shows a circuit with the static state chosen in accordance to (6).

2.3. *Biasing integrated circuits*

Integrated, solid-state circuits comprise thin-film components located on the substrate of silicon. Hence, there are principal technology limitations that restrict the size of components, their extreme values, and tolerances. An important advantage of integrated circuits is the possibility to use a large number of identical transistors [see Fig. 4(a)]. (A couple of transistors can be nearly identical provided they are close each other on the same silicon substrate. More distant transistors are much more different because they pass the technological process in substantially more different conditions. It is impossible to maintain exactly the same technological parameters across the entire substrate surface.)

To simplify the technology and reduce the area of the chip, the integrated circuit design is aimed at using only transistors. Only a few resistors and capacitors, if at all, are allowed. Therefore, we have to find a different solution to eliminate the drawbacks of the elementary bias.

We will see in Section 2.4, that having a couple of identical transistors, and we do have plenty on them on a chip, we can easily build an independent current source. Defining the collector current in a CE amplifier through biasing the emitter current by the independent current source I_E [see Fig. 4(b)] helps us to both get rid of the non-universal V_{BE} source and to improve the bias stability. Moreover, we do not also have to use neither coupling nor bypass capacitors. We simply

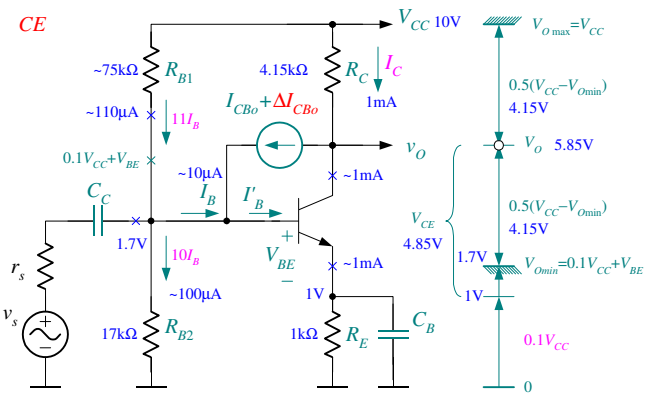
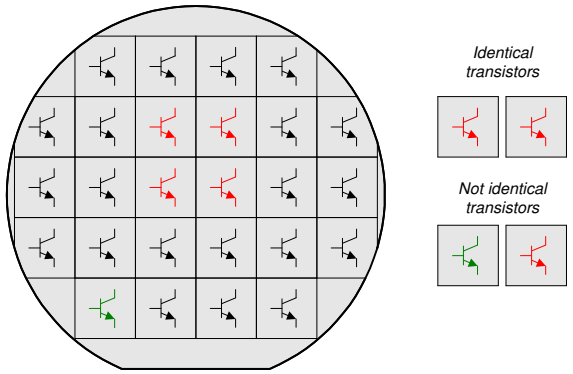
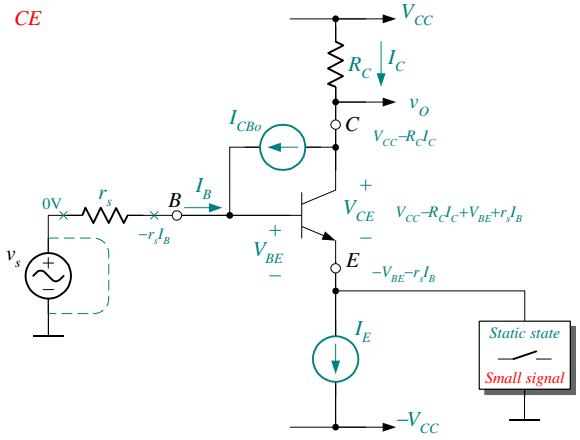


Fig. 3. Example circuit.



(a)



(b)

Fig. 4. Biasing integrated circuits. (a) Transistors in a wafer. (b) A practical circuit employing a current source to apply I_E.

connect the signal source directly to the base, without sacrificing the dc gain. We do not also suffer from the thermal sensitivity of I_C on β_F, because the I_E–I_C translation is via α_F, which is almost insensitive to temperature (think why?). We

do not suffer from the amplification of the leakage current I_{CBo} since $I_C=\alpha_F I_C+I_{CBo}$, and this sets S_I at its minimum, $S_{I\min}=1$. Furthermore, later in the course we will also get rid of R_C by replacing it with a transistor. The only task we will have to solve is how to connect the emitter of the CE amplifier to ground for small signals [see Fig. 4(b)], including dc ones. (Prove that leaving this task unsolved will reduce to zero the voltage gain of the CE amplifier.)

2.4. *Current mirror*

Let us now design a practical current source. Our aim is to provide an almost *constant* current through a *variable* load R_L connected to a static voltage supply V_{CC} [see Fig. 5(a)]. (The load may represent not just a resistor but also an entire circuit we would like to bias.) Since current sources are absent in nature, we will convert the static V_{CC} into a constant, or almost constant, current. We will first convert V_{CC} into the constant collector current of a master transistor and then copy or mirror it with an identical slave transistor connected to the load [see Fig. 5(a)]. We need the master transistor since the R_L value can fluctuate in a general case. Instead of a not necessarily constant load, R_L, we use a constant reference load (a resistor), R_r, and this provides us with a constant *reference* current:

$$I_r = \left.\frac{V_{CC}-(V_{BE}\pm\Delta V_{BE})}{R_r}\right|_{V_{CC}>>\Delta V_{BE}} \neq f(T). \qquad (7)$$

Note that despite the shortening the base and the collector, the transistor still operates in the active region (the collector-base junction is not biased in the forward direction) and, therefore, $I_{CM}=\beta_F I_{BM}$.

To copy $I_{CM}\approx I_R$, we first copy the V_{BE} voltage of the master by connecting to it the base-emitter junction of the slave. For $V_{CES}=V_{CEM}$, the same V_{BE} provides, the same, collector currents in both the transistors: $I_{CM}=I_{CS}$. To check the situation for $V_{CES}>V_{CEM}$, let us consider the graphical solution in Fig. 5(b). Note that to find the load line of the master transistor in Fig. 5(b), we apply in Fig. 5(a) Miller's theorem for currents and find the equivalent load, $R_r(1+2/\beta)$, at the collector of the master transistor.

From Figs. 5(a) and (b), we can conclude that

$$I_{CS}=I_L=\underbrace{\underbrace{\frac{V_{CC}-V_{BE}}{R_r\dfrac{2+\beta_F}{\beta_F}}}_{I_{CM}}-\frac{V_{BE}}{r_o}}_{I_N}+\underbrace{\frac{V_{CES}}{r_o}}_{I\text{ through }R_N}, \qquad (8)$$

which is the equation of a non-ideal (practical) current source: an ideal current source and a resistor in parallel to it [see Fig. 5(c)]. We can also say that (8) is the Norton equivalent of the slave transistor with the equivalent current source $I_N=\beta_F(V_{CC}-V_{BE})/R_r(2+\beta_F)$ and the Norton resistance $R_N=r_o$ [see Fig. 5(c)].

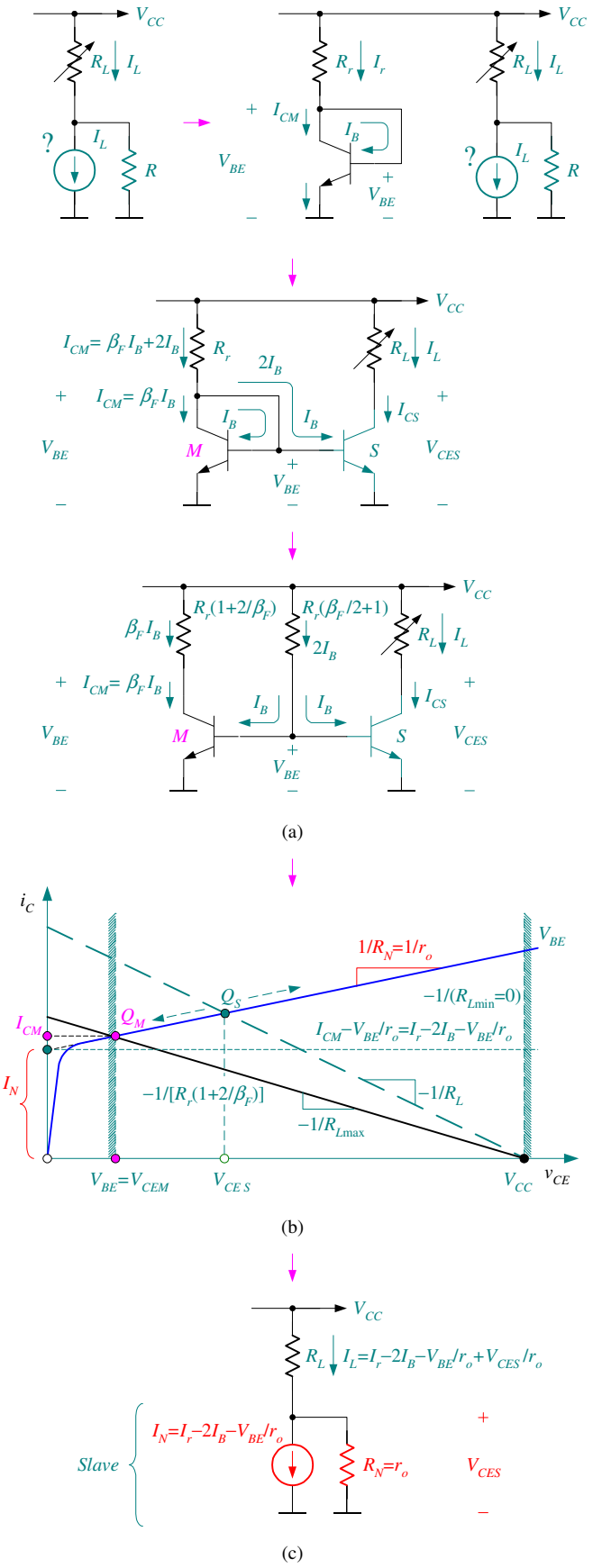


Fig. 5. Current mirror. (a) Developing the circuit. (b) Graphical solution. (c) Equivalent circuit.

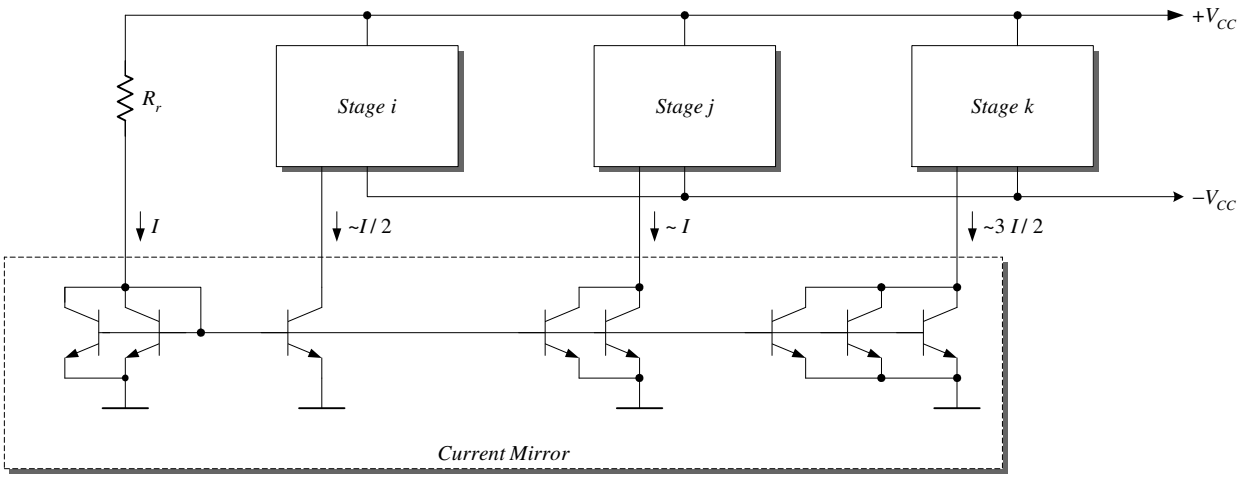


Fig. 6. Multi-output current mirror with a single R_r.

Thus, we get exactly what we need: a current source that keeps almost *constant* current through a *variable* load.

Note that the slave can be able to copy not exactly the same I_{CM}. For example, it is possible to copy 1/2, or 1/3, or 2/1 of I_{CM} if the cross-sectional area of the slave base-emitter junction, A_{BES}, is 1/2, or 1/3, or 2/1 of A_{BEM}. (Recall that $I_C = I_{CS}e^{V_{BE}/V_T}$, and $I_{CS} \propto A_{BE}$.) Note also that it is possible to connect to a master a number of slaves (see Fig. 6) each providing a *scaled* I_{CS}, relative to I_{CM}, for the stage it has to bias. Naturally, the $2I_B$ term in (8) should be replaced by $\sum_{i=1}^{n} I_{Bi}$, where n is the number of the slave transistors.

REFERENCES

[1] A. S. Sedra and K. C.Smith, *Microelectronic circuits*.