THE BEST OF TWO WORLDS:

A MIXED-MODE FRONT-END CONTROLLER IC

by
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I. Introduction

Up until the last couple of years, analog electronics has been used almost exclusively in the implementation of power supply controllers. It is generally recognized though, that the analog solution has some deficiencies when compared to the digital control approach: it requires a relatively large number of components (resistors, capacitors etc.), and it has a rigid design and hence needs to be tuned to each power level, cannot be programmed in the factory and certainly can not be altered in the field. And further, the long-term stability as well as thermal effects and thermal stability are inferior to those of the digital circuits. And yet, the analog solution has its undisputed merits: it is less expensive than the digital approach and in contrast to common intuition; it is more accurate than the digital approach. This is because it does not suffer from sampling errors, delays, and duty cycle resolution problems. Given infinite computing power, zero power dissipation, vast software engineering support and a price tag comparable to the analog solution, the digital controller will surely be preferred. In reality, the digital controller solution is presently more expensive than the analog one making it less attractive in price sensitive applications such as low to mid power range AC-DC front ends.

A cursory cost analysis of the digital controller solution immediately reveals that the higher cost is associated with parts that are involved in the feedback loop. To achieve a wide bandwidth for the feedback loop requires fast A/D converters and a high frequency clock that are expensive and have high power dissipation. It stands to reason, therefore, that an optimal design of controllers for SMPS can be achieved by using the best of the two worlds, analog and digital.

Previous attempts to combine analog and digital control [1] suffer from a number of drawbacks. The first is the reliance on conventional analog parts that still require many external components. Another problem is the inefficient interfaces between the analog and digital parts (for example: using averaged PWM signals as a D/A). It is thus evident that a pre-requisite for reaching an optimal mixed-signal solution, is an innovative analog part that must have some key features the will streamline the marrying the two technologies. One of them is universality. That is, the ability to function as-is over a wide range of power levels without the need to change peripheral components such as resistors and capacitors of the phase compensation network. Another requirement is circuit

simplicity and compatibility with mainstream, low-cost microcontroller VLSI technologies so that a single chip realization is a viable possibility.

The Mixed-Mode Front-End Controller (MMFEC) described in this paper was designed along the above guidelines. The objective was to develop a complete front-end solution that includes the control of a PFC stage and inrush current, housekeeping, optional interfaces to the subsequent stages, and digital communication for control, telemetry and management purposes. The analog part of the MMFEC is based on a novel PFC approach to be discussed first.

II. The PFC control method

Conventional embodiments of CCM APFC systems [2] include a controller that senses the input voltage and the line current (Fig.1).

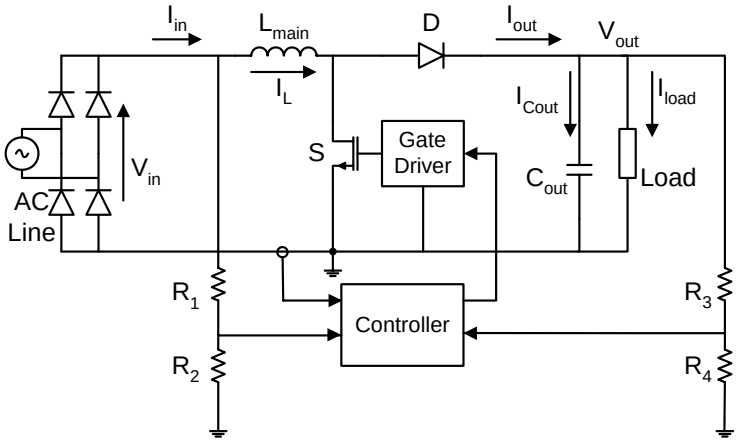


Figure 1: Conventional CCM APFC approach.

The shape of the rectified power line voltage, obtained from the input voltage V_{in} via the divider R_1 and R_2, is used as the reference for the desired shape of the input current. The controller also receives a signal that is proportional to the input current. The current level is adjusted for any given load by monitoring output voltage V_{out} via the divider R_3 and R_4, and multiplying the reference signal of the current control loop by the deviation from the desired output voltage level, so as to trim the effective reference signal to the load.

A drawback of this conventional implementation is the need to sense the input voltage, namely the line voltage after rectification. Due to switching effects, the input voltage is normally noisy and is susceptible to interference pick-up that may distort the reference signal and hence the input current. Experienced engineers have learnt the hard way; designing an APFC system to operate over a wide range of power levels using a conventional controller is no easy task. Making the inner (current) loop stable is tricky and fighting the ground loops is exhausting.

Thus, the conventional PFC control method is unsuitable as the analog part of the MMFEC, since one of the basic requirements is that there will be no need for re-adjusting the controller for each power level or power stage design.

An alternative solution for APFC control is to operate a Boost topology in Discontinuous Conduction Mode (DCM). In this case the input current of the converter will track the average input voltage - when the power stage is driven by a constant duty cycle during the power line period [3, 4]. Consequently, sensing of the input voltage in such cases is not required. Unfortunately, the high ripple of the inductor current, and hence, the high RMS current of the switch, limits DCM to low power applications. It is generally recognized that CCM mode of operation is the practical solution for medium and high power levels. Other solutions utilizing a "voltage follower" approach in different topologies [5] are also restricted to low power levels only.

Since the analysis of our PFC control concept that was found suitable for the MMFEC, has been published earlier [6-8], for the sake of brevity, we repeat here only the essentials. The APFC method is based on the Boost topology operating in the CCM. The system (Fig. 2) includes a power stage and a control scheme that senses the input current and produces a D_{off} duty cycle proportional to the average value of this current.

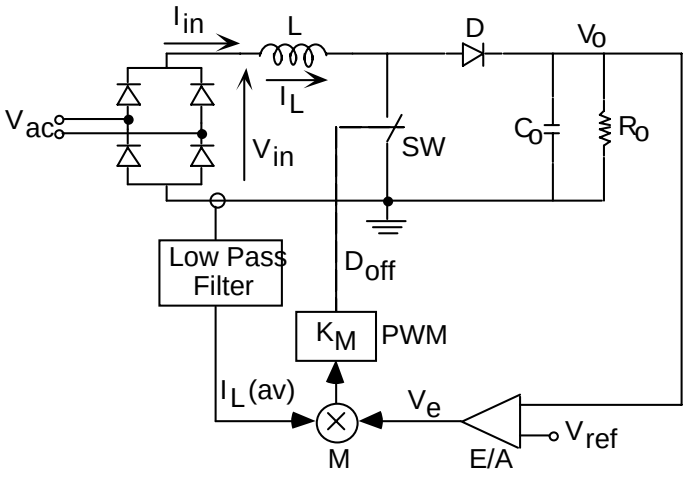
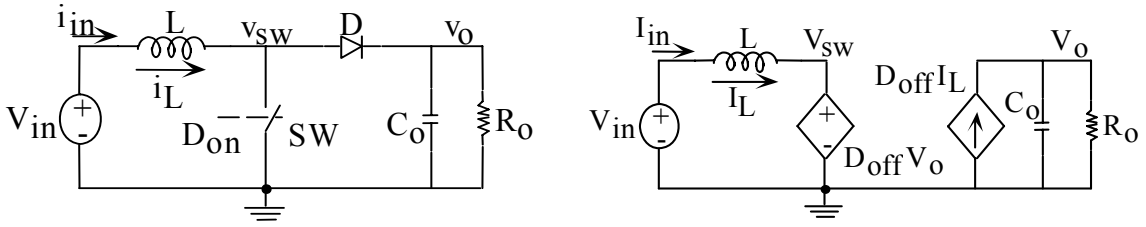


Figure 2: Implementation of an APFC control scheme with no sensing of input voltage.

The outer loop is used to trim the proportionality constant (between the input current and D_{off}) to accommodate any given load. The principle of operation can be understood by considering the average model of Fig. 3 that represents the power stage (Fig. 3a) and its average model (Fig. 3b).



(a) (b)

Figure 3: The Boost converter (a) and its behavioral average model (b) ([9, 10]).

Assuming the circuit is stable (as will be shown below), this implies (Fig. 3b):

$$V_{in}(av) = D_{off} V_o(av) \qquad (1)$$

where, D_{off} is (1-D_{on}), D_{on} is the duty cycle, $V_{in}(av)$ is the average input voltage and $V_o(av)$ is the average output voltage. Averaging is over one switching cycle under the assumption that the switching frequency is much higher than the bandwidth of V_{in} and of V_o.

Since the average input current $I_{in}(av)$ is equal to the average inductor current $I_L(av)$, equation (1) can be manipulated to the form:

$$\frac{V_{in}(av)}{I_{in}(av)} = \frac{D_{off} V_o(av)}{I_L(av)} \qquad (2)$$

To make the input resistive with an input resistance R_e, we require:

$$\frac{V_{in}(av)}{I_{in}(av)} = R_e = \frac{D_{off} V_o(av)}{I_L(av)} \qquad (3)$$

That is, a resistive input will be observed if D_{off} is programmed according to the rule:

$$D_{off} = \left(\frac{R_e}{V_o(av)} \right) I_L(av) \qquad 0 < D_{off} < 1 \qquad (4)$$

The stability of the circuit can be appreciated by considering the simplified block diagram of Fig. 4.

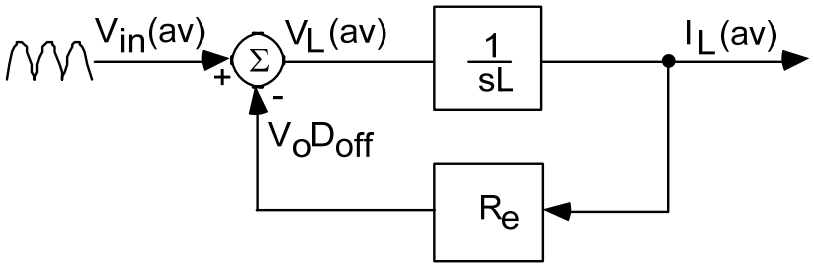


Figure 4: Simplified block diagram of current control loop.

In this control scheme the voltage imposed on the inductor (V_L) is equal to the input voltage minus the average voltage at the switch (Fig. 3b). The summing junction reconstructs the total voltage imposed on the inductor (L) while the feedback path represents the D_{off} programming according to (4). This block diagram representation assumes that the output voltage (V_o) is constant with negligible ripple and that R_e is set to a given constant value. Under these conditions, the system (Fig. 3) is linear and the loop-gain (βA) is found to be:

$$\beta A = (R_e)(\frac{1}{sL}) = \frac{R_e}{sL} \qquad (5)$$

which represents a bandwidth of $R_e/2\pi L$ and a phase margin of 90^0. This implies that the 'inner' current feedback loop is unconditionally stable for any input or output voltages - under the assumption that V_o is constant. But, as further analysis provided below shows, this conclusion is also valid for practical cases.

The closed loop response (input current as a function of input voltage) is clearly:

$$\frac{I_L(av)}{V_{in}(av)} = \frac{1}{R_e}\frac{1}{1+s\frac{L}{R_e}} \qquad (6)$$

where $I_L(av)$ and $V_{in}(av)$ are the low frequency component of the inductor (and input) current and the low frequency component of the input voltage respectively. This result implies that the tracking bandwidth is $R_e/2\pi L$ as would be expected from (5).

In practical APFC applications for 50/60 Hz power line, the tracking bandwidth (BW_{Iin}) should be at least 1kHz [11] or, in general:

$$\frac{R_e}{2\pi L} = (BW_{I_{in}}) \qquad (7)$$

This constraint can now be checked against other design considerations and in particular, the size of the inductor required to keep the current ripple within reasonable limits.

Maximum ripple is reached at $D_{on} = 0.5$ that is when $V_{in}(av) = 1/2\ V_o(av)$. The ripple ($\Delta I$) at this point will be:

$$(\Delta I)_{D_{on}=0.5} = \frac{V_{in}(av)}{2 f_s L} \qquad (8)$$

where f_S is the switching frequency.

The ripple ratio ($\Delta I/I_{in}(av)$) will be:

$$\left(\frac{\Delta I}{I_{in}(av)}\right)_{D_{on}=0.5} = \frac{\frac{V_{in}(av)}{2 f_s L}}{\frac{V_{in}(av)}{R_e}} = \frac{R_e}{2 f_s L} \quad (9)$$

Combining (7) and (9) we obtain:

$$\left(\frac{\Delta I}{I_{in}(av)}\right)_{D_{on}=0.5} = \frac{\pi}{f_s}(BW_{I_{in}}) \qquad (10)$$

or:

$$(BW_{I_{in}}) = \frac{1}{\pi} f_s \left(\frac{\Delta I}{I_{in}(av)}\right)_{D_{on}=0.5} \qquad (11)$$

which implies that for a design of say $\left(\frac{\Delta I}{I_{in}(av)}\right)_{D_{on}=0.5} = 0.1$ (that is, maximum current ripple is 10% of the nominal current value), the tracking bandwidth will be about $f_S/30$. This is obviously more than enough for modern switch mode systems in which f_S>50kHz. For higher ripple ratios the bandwidth will be even larger.

The dynamics of the control scheme was thoroughly studied earlier [8]. It was found that the expression for the inner (current) loop is:

$$\beta A = \frac{sC_o R_o R_e + R_e + D_{off}^2 R_o}{s^2 L C_o R_o + sLR + D_{off}^2 R_o} \qquad (12)$$

and, for practical values (C_o=1mF; L=1mH, R_o= 140Ω) it is well behaved (Fig. 5).

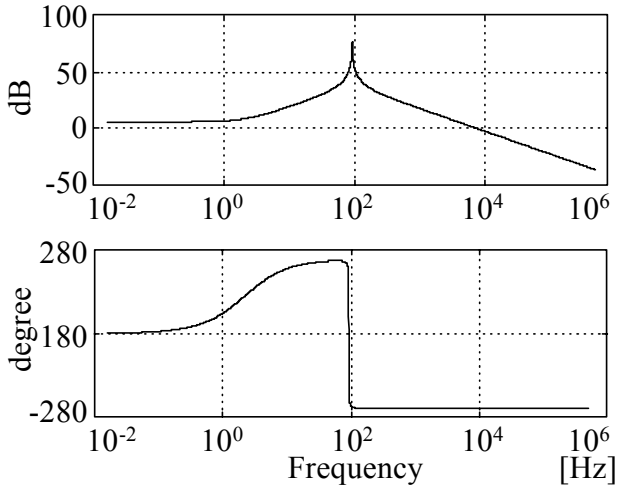


Figure 5: Loop gain of the current control loop.

Consequently, good current tracking is obtained over the required frequency range (Fig. 6).

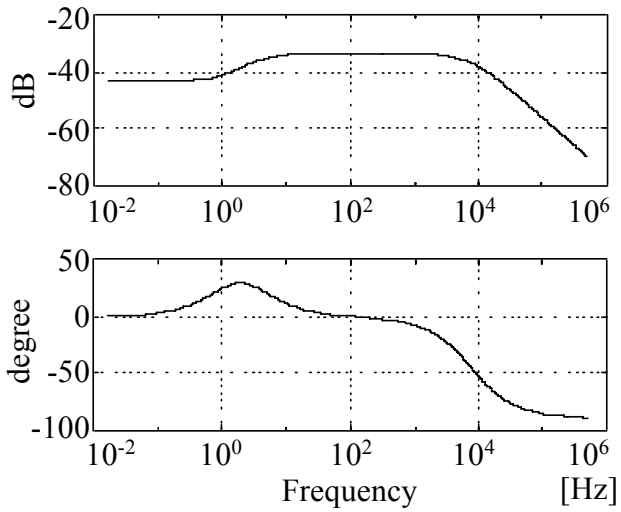


Figure 6: Transfer function of the current control loop.

To further explore the salient differences between our approach and the 'classical' CCM implementation we compare the two when represented by control-type block diagrams (Fig. 7). Only the parts associated with the current tracking are depicted. In each case there would be a need for an outer loop amplifier to keep the output voltage constant under variable operating conditions.

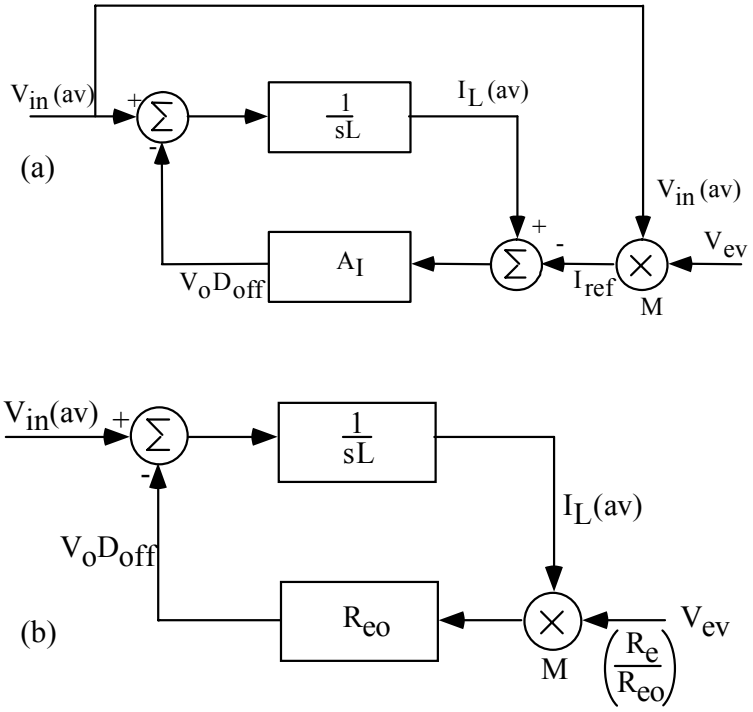


Figure 7: Block diagram of a conventional (a) and our solution for (b) power factor correction control.

The output of that error amplifier (V_{ev}) is used to drive the inner current loop. The two block diagrams are approximate. Both assume that the output voltage has no ripple component. We will also neglect here the ripple on V_{ev} and possible feedforward circuits [12, 13]. In the conventional control scheme shown in Fig. 7a, we recognize an inner current loop and a multiplier that generates the reference to the inner loop. The feedback loop is composed of two parts: the inductor that sees two opposing voltages, $V_{in}(av)$ and V_oD_{off} [9, 10] and a current error amplifier A_I. The latter is taken to include the modulator transfer function, sensing resistor and amplifier gain. The drive signal of this inner loop is a reference current I_{ref} which is generated by multiplying the rectified input voltage by the output of the outer loop error amplifier (V_{ev}). On the other hand, the proposed control scheme uses the input voltage $V_{in}(av)$ as the excitation signal of the inner current loop (Fig. 7b). In this case, the output of the outer loop operational amplifier (V_{ev}) modulates the effective input resistance (R_e). Nominal value is assumed to be R_{eo} and for any other operating condition V_{ev} will change the input resistance so as to keep V_o at the desired level. For the conventional control scheme (Fig. 7a) $V_{in}(av)$ is in fact a disturbance.

However, due to the high loop gain provided by A_I, which is built around an operational amplifier, the conventional current loop can suppress this disturbance as well as that caused by the output ripple. In our control scheme (Fig. 7b), the magnitude of loop gain is evidently smaller (6), but if the interaction between the inductor L and output capacitor Co is taken into account (Fig. 5) one finds that the increase in the loop gain due to the passive components is rather significant. As it happens, practical value of L and C_o will have a resonant frequency around the low frequency range. A theoretical analysis of this question is beyond the scope of this paper.

But examination of practical examples clearly show that the resonant range is as pointed out. For example, a normal engineering choice is 1mF for a 1kW APFC while the inductor will be in the range 0.5mH to 1mH for this power range (depending on the switching frequency). This will result in resonant frequency of 160 Hz. Damping will move the resonant frequency somewhat but it is still expected to be in the right range.

The high loop gain due to the passive resonant phenomena explains the excellent tracking and the rejection of the disturbance due to the output ripple. In the conventional case, the rejection is due to the high loop gain provided by A_I (Fig. 7a). But the high gain of the operational amplifier plus the extra phase shifts of the phase compensation network may deteriorate the phase margin. Furthermore, the introduction of a very high gain operational amplifier may render the system sensitive to switching noise. In the light of the above, it appears that the lack of an operational amplifier in the inner current loop is a significant advantage.

III. The analog circuit

As discussed in Section II, a resistive behavior at the input of a Boost converter will be observed if D_{off} is made proportional to the average input current (4). One possible way to achieve this under closed (outer loop) conditions is shown in Fig. 2. This solution requires a multiplier (M) to adjust R_e as a function of the load voltage V_o.

However, circuit implementation of analog multiplier is relatively complex and expensive since it calls for transistors matching and may require trimming. An alternative innovative circuit shown below can realize the PFC control scheme under consideration without an analog multiplier by making the ramp of the PWM modulator variable and dependent on the output voltage error signal [6, 14]. Such possible realization of a controller without a multiplier is depicted in Fig. 8. In this circuit, D_{off} is generated by comparing a signal that is proportional to the average input current ($I_L(av)R_S$), to a ramp voltage that is generated by charging the capacitor C_{ch} by a depended current source (G_1). The output of the current source (I_{ch}) is proportional to the output (V_e) of the voltage error amplifier (A_2):

$$I_{ch} = G_m \cdot V_e \quad (23)$$

where G_m is the transconductance of A_2.

Thus, the voltage ramp that is applied to the positive input (V+) terminal of the comparator can be described by:

$$V_+ = \frac{I_{ch}}{C_{ch}} t = \frac{G_m \cdot V_e}{C_{ch}} t \quad (24)$$

where t is time.

The voltage at the negative input of the comparator is proportional to the average input current that is obtained by sensing the current across the sense resistor R_S. The low frequency average of the sensed voltage is extracted by passing the signal through a low pass filter (R_f, C_f). Consequently, the signal at the negative input terminal of the comparator (V-) will be:

$$V_- = I_L(av) \cdot R_S \quad (25)$$

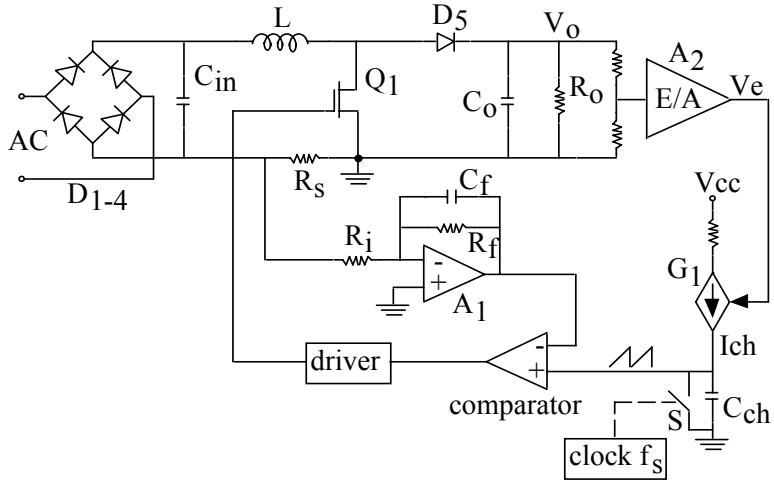


Figure 8: Realization of the multiplier action by a controllable slope.

As long as V+ is smaller then V-, the comparator's output voltage will be held in its low state ("off" part of the switching period). This period terminates when V+ reaches the magnitude of the signal at a V- . This will determine the duration of T_{off}, i.e. at $t=T_{off}$, V+ and V- will be equal. Equating (24) and (25) we find:

$$\frac{G_m V_e}{C_{ch}} T_{off} = I_L(av) R_S \quad (26)$$

The switching frequency (f_S) is determined by resetting the capacitor C_{ch} every T_S seconds by a switch (S). Since $D_{off}=T_{off}/T_S$, we find:

$$D_{off} = \frac{I_L(av)}{V_e}\frac{R_S \cdot C_{ch}}{G_m \cdot T_S} \quad (27)$$

Applying (3) , R_e is given by:

$$R_e = \frac{V_o(av)}{V_e}\frac{R_s \cdot C_{ch}}{G_m \cdot T_s} \quad (28)$$

Hence, a load change that will tend to vary the output voltage V_o, will cause a change in V_e such that R_e will be modified according to (28) and the output voltage will be stabilized. The magnitude of the V_o change due to a load variation will depend on the overall gain of the voltage feedback loop.

IV. The mixed mode controller concept

The PFC control concept and circuitry described above match the requirements set forth for the MMFEC very well. The analog circuit is simple, compatible as-is with a wide range of power levels, does not need any external components (except for the sense resistor), and does not require any special micro-electronics fabrication technology. Thus, the general concept of the mixed-mode controller includes analog and digital sections as shown schematically in Fig. 9. Also shown in the figure is a simple inrush current control (relay based) that is practically a free byproduct of the mixed signal capability. Fig. 10 provides a better insight into the circuitry realization of the digital-analog assembly and the interconnection thereof. Shown in this case is a Power MOSFET based inrush control.

The required analog part (Fig. 10) includes a 'current amplifier' A_i to amplify the voltage across the sense resistor R_s, a ramp capacitor C_{ramp} and discharge switch Q_{ramp}, a comparator $COMP_1$, and current source I_s which is in fact a part of an A/D converter. Also included in the analog circuit is a second comparator $COMP_2$, used for over current protection. The circuit is simple and inexpensive to implement on a chip.

Since the analog section takes care of the inner current loop, the micro-controller only needs to handle the outer voltage loop, which has a narrow bandwidth and hence, does not require fast sampling rates.

The objective of an optimal design is that the digital control algorithm should not just mimic and be 'as good as' the analog controller but should (as implemented in the NGPower chip) have better performance by applying logic based non-linear control. Thus, the MMFEC achieves performance superior to what is possible with analog control. For example, the output voltage transients due to load and input voltage steps can be reduced dramatically.

A 'free' bonus of the mixed mode controller is the capability to handle inrush current. This can be achieved in many different ways to fit any particular application. To this end, divider R_a, R_b. is used to sense the input voltage, aside from the output voltage needed also for the PFC control. Fig. 9 shows a relay-based implementation while Fig. 10 demonstrates a PWM based solution. Upon turn on, series switch Q_4 is driven by a slowly increasing duty cycle to limit the magnitude of the inrush current. Another example is a thyristor based inrush control that can also be easily implemented as shown in Fig. 11.

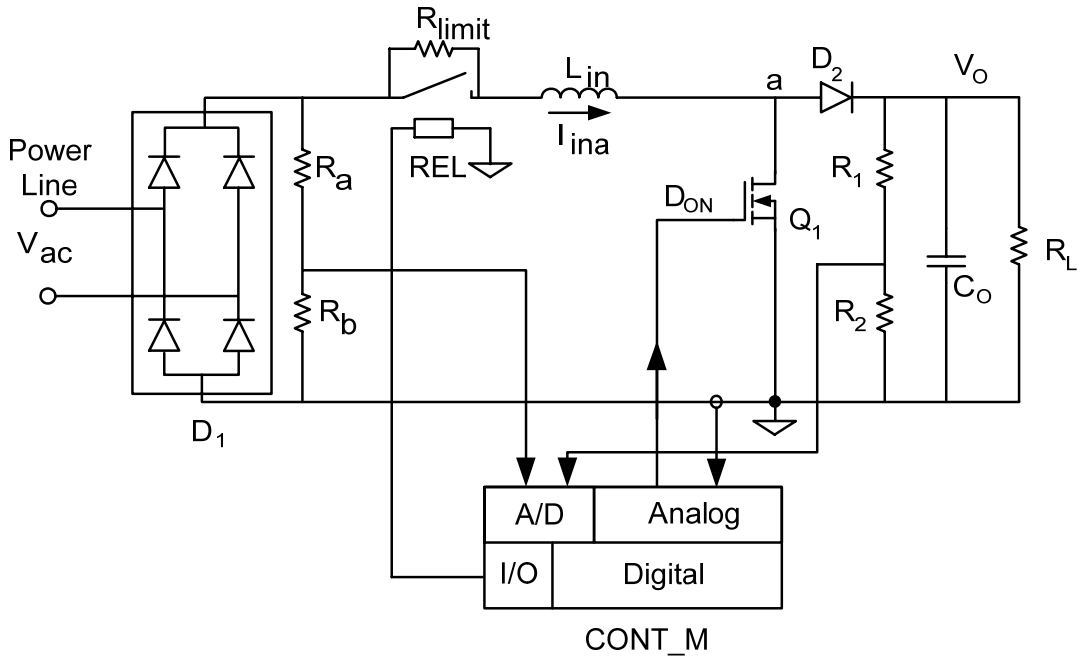


Figure 9: Relay-based implementation of inrush current

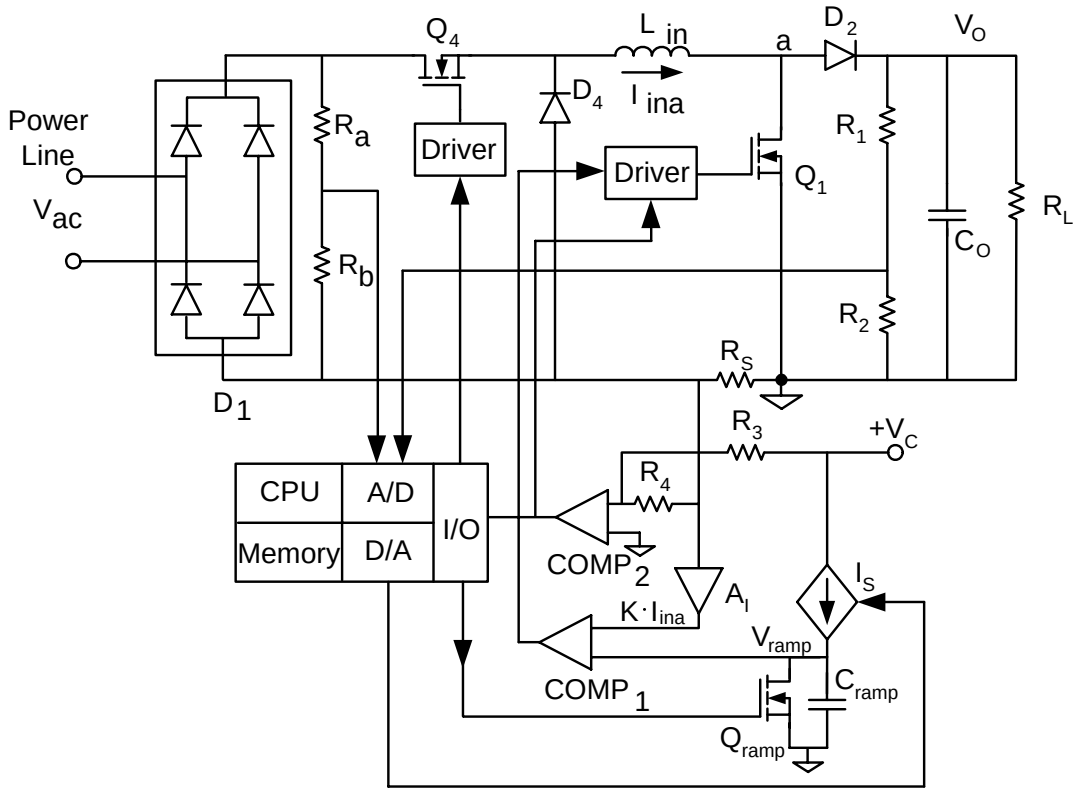


Figure 10: PWM-based implementation of inrush current

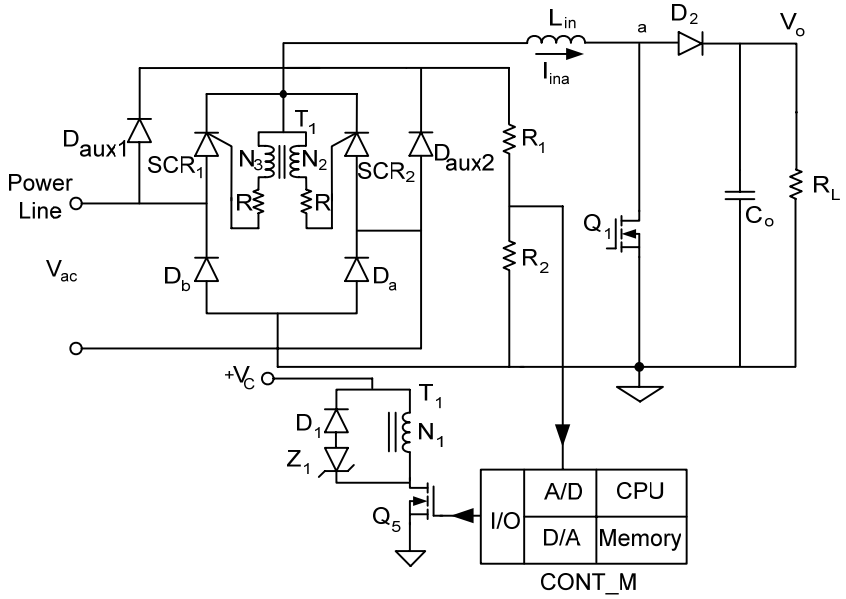


Figure 11: Thyristor-based implementation of inrush current

V. Experimental Results

As reported earlier [7, 8, 15], the analog part of our PFC control method is proven to have extremely good performance. When using this method a good THD value is obtained down to 4% at full load for universal line system as shown in figures 12-17. The experiments described below were aimed to test the symbiosis of the analog and digital parts.

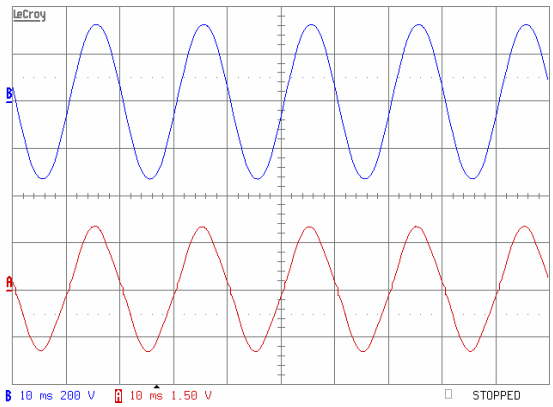


Figure 12: Input behavior. Pout≈300W. Upper trace: Input voltage 230Vrms. Lower trace: Input current 1.5A/div. Horizontal scale: 10ms/div.

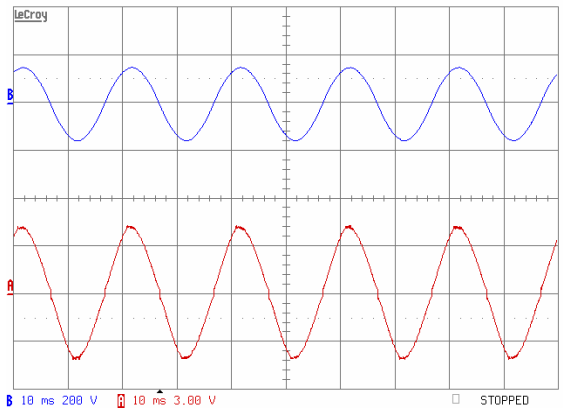


Figure13: Input behavior. Pout≈300W. Upper trace: Input voltage 110Vrms. Lower trace: Input current 3A/div. Horizontal scale: 10ms/div.

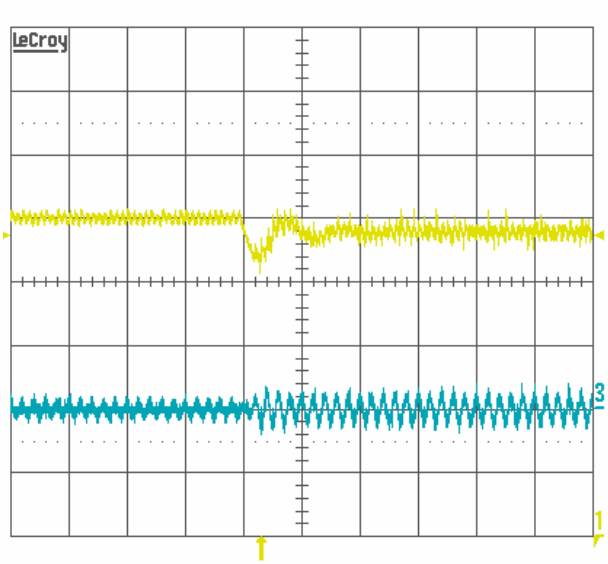


Figure 14: Input voltage step. Pout=50W; Vin=265Vac -> 85Vac; Upper trace: output voltage – 10V/div; Lower trace: input current – 5A/div; Horizontal scale: 0.1s/div

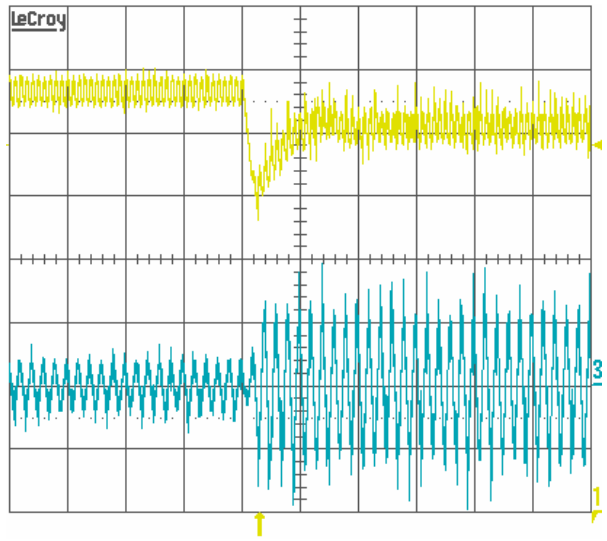


Figure 15: Input voltage step. Pout=300W; Vin=265Vac -> 85Vac; Upper trace: output voltage – 20V/div; Lower trace: input current – 5A/div; Horizontal scale: 0.1s/div

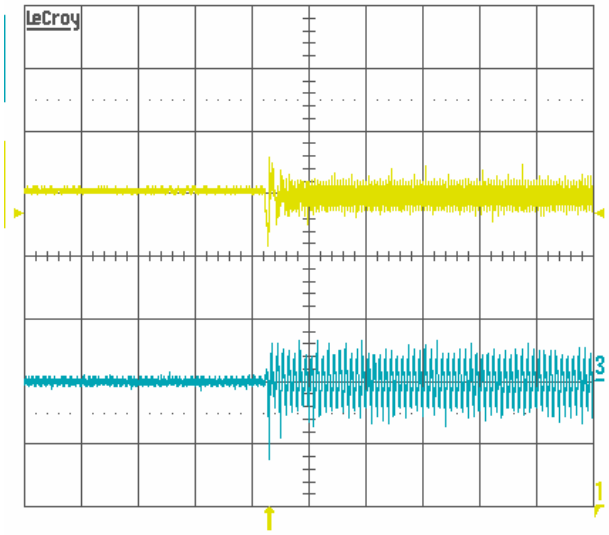


Figure 16: Load step. Vin=230Vac; Load=15W -> 300W; Upper trace: output voltage – 20V/div; Lower trace: input current – 5A/div; Horizontal scale: 0.2s/div

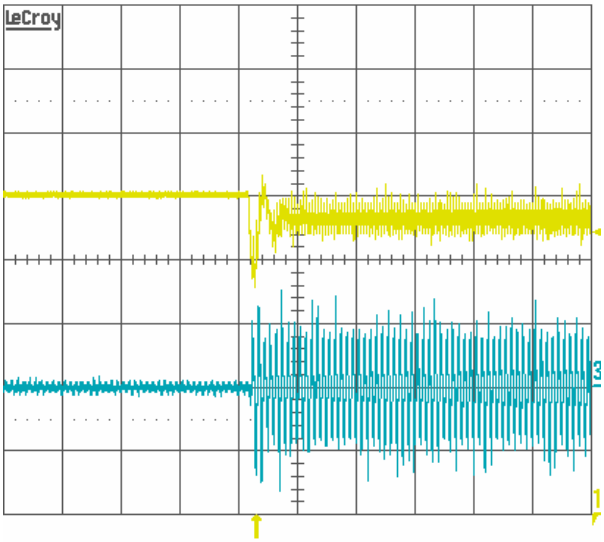


Figure 17: Load step. Vin=110Vac; Load=15W -> 300W; Upper trace: output voltage – 20V/div; Lower trace: input current – 5A/div; Horizontal scale: 0.2s/div

A test setup (emulator) was built using an off-the-shelf microcontroller (PIC16F876) and the GPT1105A analog PFC controller. Two experiments were carried out to demonstrate and test the concept of our MMFEC under moderate power levels (up to 1kW). The first: an implementation of a 1KW PFC stage and the second: an electronic ballast for fluorescent lamps.

The experimental setup of the emulator-based 1kW PFC stage (Fig. 18) included a 1mH inductor, and 1mF output capacitor, a single Power MOSFET switch (IRFP460) operating at 75kHz switching frequency.

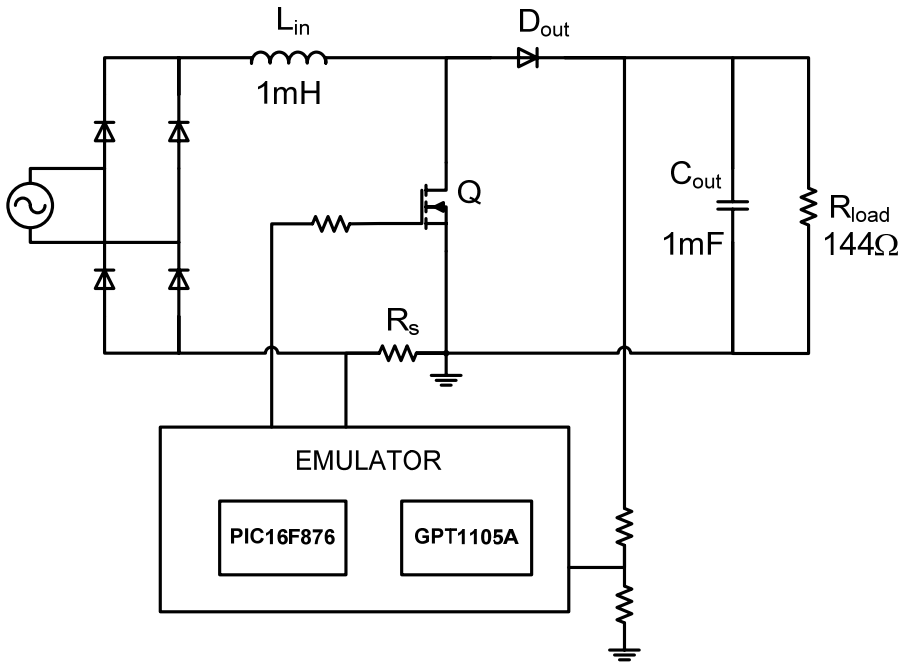


Figure 18: Experimental setup of 1kW PFC stage.

The system was operated from AC source. Output voltage was 385V. Typical input voltage and current (Fig. 20) demonstrate the excellent performance of the system. THD was measured to be about 5%, far below the Line Harmonics Limits standard (EN61000-3-2).

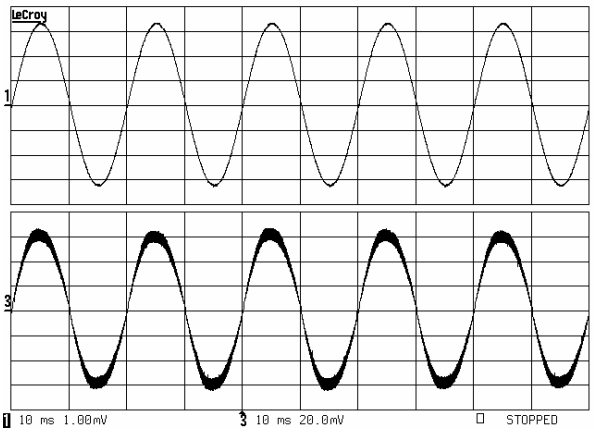


Figure 19: Input behavior of the system shown in Fig. 19. Upper trace: input current 2A/div. Lower trace: input voltage 230VAC.Horizontal scale: 10mS/div.Vout=385V. Pin=975W

The second test of our MMFEC was implementing the emulator as a controller for two dimmable ballasts, each for two serially connected fluorescent lamps (Fig. 20).

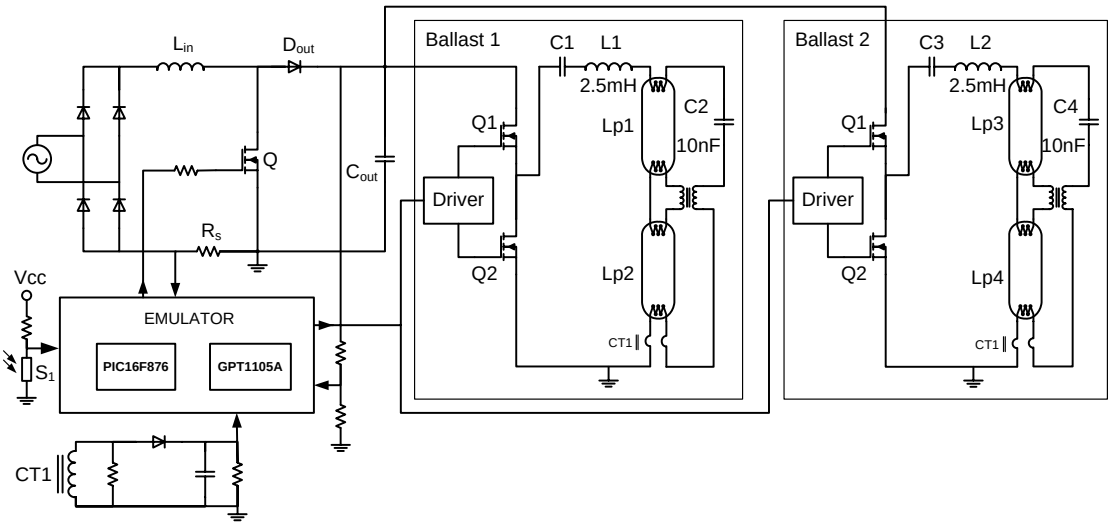
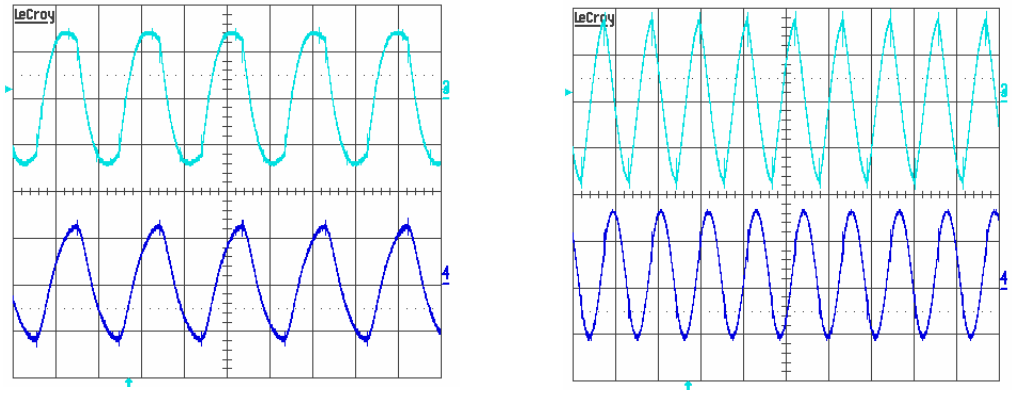


Figure 20: Experimental setup of digital PFC stage driving 2 lamp ballasts.

Ballast 1 and Ballast 2 in Fig. 20 were identical. The lamps used were LEUCIA LP2500 (36W).

The emulator's firmware was modified to generate two independent signals; one for driving the power factor section and the other for running the ballast. Dimming was accomplished by varying the drive frequency of the ballasts. The lamps were ignited by driving the ballast with the switching frequency close to resonant frequency of C1 and L1. The end of the ignition phase was recognized by sampling the lamps' current via the current transformer CT. In case the lamps failed to ignite, the ignition algorithm was repeated until the ignition succeeded or maximum (predefined) number of ignition cycles reached. In the latter case the drivers shut off. The information obtained from sampling the lamps current was further used to dim the lamps in response to the changes in the environmental lighting. The latter was measured by a photoresistor S_1.

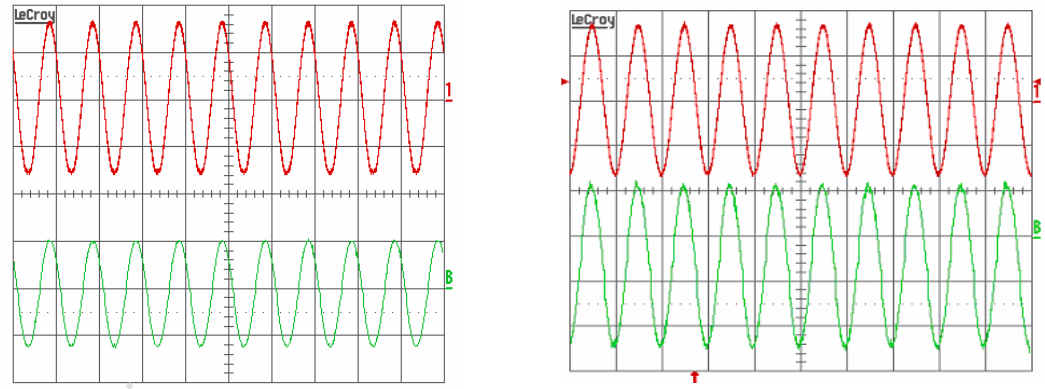
Lamps' voltage and current (one branch) at different power levels are presented in Fig. 21.



(a) (b)

Figure 21: Lamps' voltage and current (one branch). (a) Full load (Pin=187W). Upper trace: lamps' current 0.5A/div; Lower trace: lamps' voltage 200V/div; (b) Dimmed lamps (Pin=59W). Upper trace: lamps' current 0.25A/div; Lower trace: lamps' voltage 200V/div. Horizontal scale: 20μs/div.

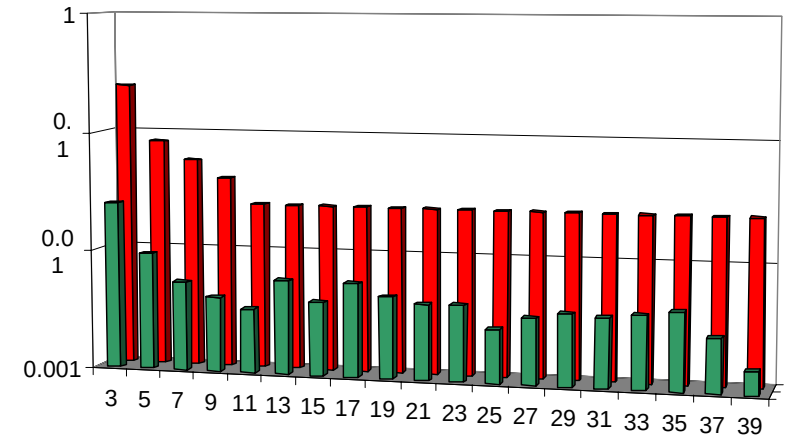
The input behavior of the system of Fig. 21 at the two power levels is depicted in Fig. 22.



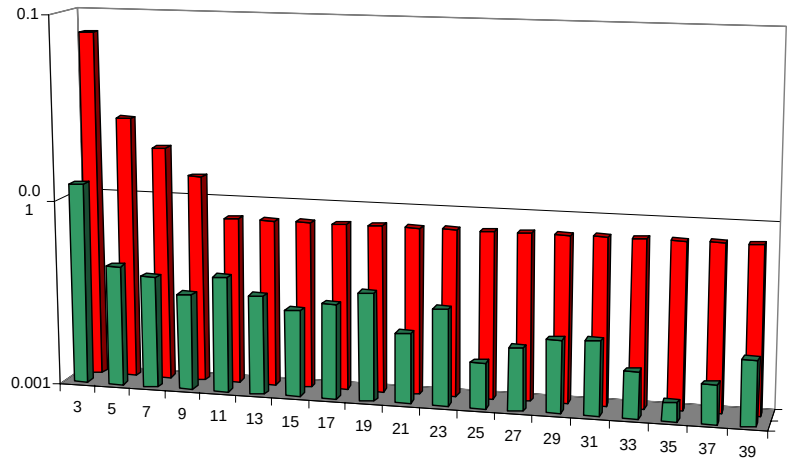
(a) (b)

Figure 22: Input behavior of the front-end of Fig. 21. (a) Full load (Pin=187W). Upper trace: input voltage (230Vac); lower trace: input current 1A/div. (b) Dimmed lamps (Pin=59W). Upper trace: input voltage (230Vac); lower trace: input current 0.2A/div. Horizontal scale 10ms/div.

Fig. 23 shows good tracking of the input current to the input voltage for the high and low power levels with exceptionally good compliance to Class C limits of the EN61000-3-2 standard. It should be noticed that the Y axis is logarithmic. It is quite clear that the system passes the standard with very high margins.



(a)



(b)

Figure 24: Compliance of the ballast of Fig. 21 to EN61000-3-2 standard (Class C). Red (toll) bars: standard limits. Green (short) bars: measured current harmonics. (a) Full load (187W); (b) Light load (57W).

VI. The NGPower NGPD4102

The MMFEC presented in this paper is being implemented in a low cost IC; the NGPD4102.

This device offers the benefits of digital power control without exceeding the price constraints of the application. The integrated device is designed to handle all the typical functions associated with the front end of a power supply as summarized in the following table:

Function	NGPD4102
APFC algorithm	CCM
Inrush current control	Yes
Soft start	Programmable
DC/DC control	Yes
Smart protections	Over-voltage Over-current Over-temperature Brown-out
Driver capabilities	Yes
Monitoring	Yes
Communication	PMBus, UART

Table 1: NGPD4102 Functions Summary

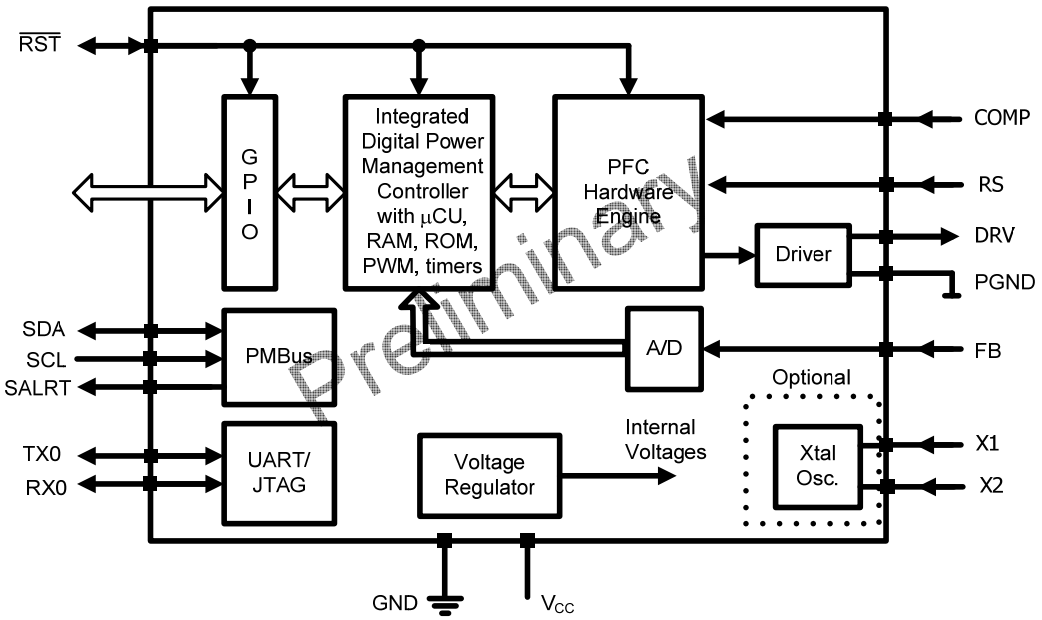


Figure 25: NGPD4102 Functional Block Diagram

The major blocks include the digital part - the Integrated Digital Power Management (IDPM) Controller and the analog PFC Hardware Engine. The IDPM is built around a micro-controller that executes the output voltage loop control algorithms and supervises the PFC Hardware Engine. The output voltage is sensed by an A/D converter of moderate speed. The IDPM Controller also performs and controls the peripheral functions such as soft start and inrush current control. The latter is facilitated by connecting current limiting devices such as SCRs or a relay to the programmable IO interface. The digital section can be clocked either by the internal oscillator or an external timing network or resonator. The device also includes a 1.5 Amp gate driver, making it possible to realize up to a 1kW front- end system without an external driver. The NGPD4102 includes a boot-ROM that initializes the device and executes the basic routines and the PFC operation so that there is NO NEED to tune the internal or external phase compensation loops., Flash memory is provided for storing user programs, application-specific parameters, and monitored data. Additional PWM outputs are provided to drive external DC-DC circuitry if required.

It is possible to communicate with the device either via a standard PMBus interface or via a UART (RS-232). The micro-controller is accessed via the UART or the JTAG interface. This allows in-circuit debugging, and direct code download during user program development phases.

The device is packaged in either 24-pin SOIC or 24-pin DIP; making it suitable for rugged SMPS applications (see Fig. 26). The power supply range for the device is 12V-30V for proper operation. Gate voltage is limited to 15V

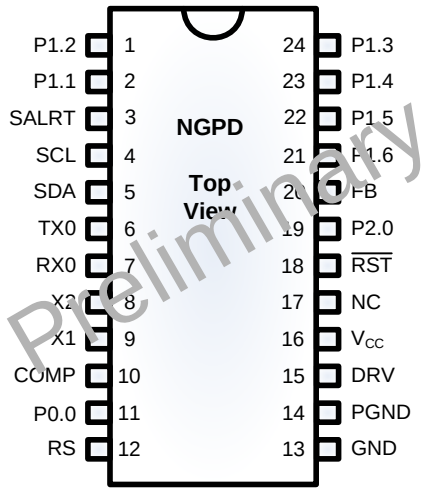


Figure 26: Preliminary pinout of NGPower's NGPD4102

VII. Evaluation Board (EVB)

The device is supplied with basic application firmware so that the designer can start using it without any development overhead. For cases that customization and adaptation to specific requirements are required, a convenient evaluation and development tool is available. The block diagram of the EVB is shown in Fig. 27 below:

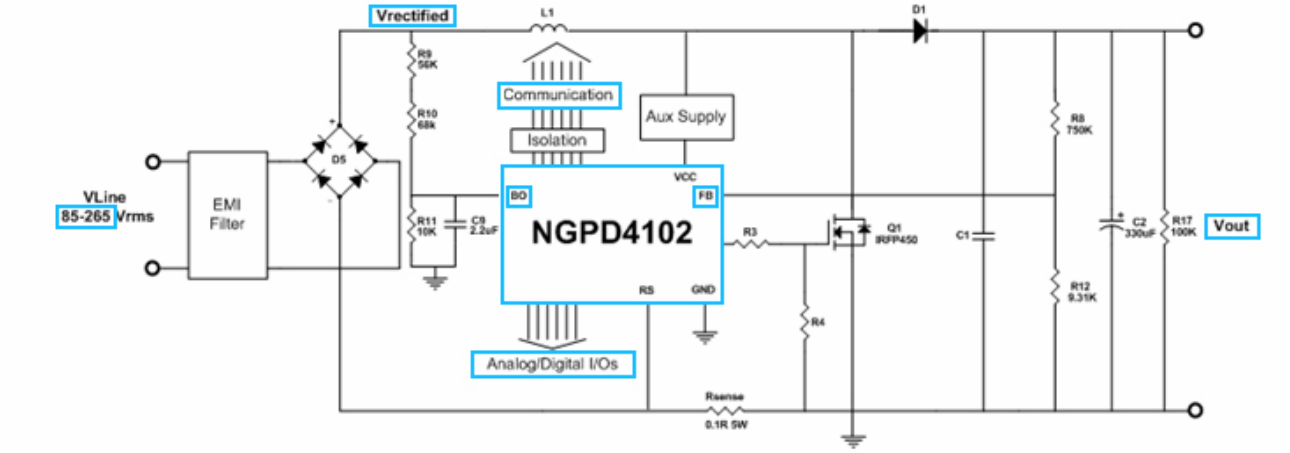


Figure 27: NGPD4102 Evaluation Board Functional Block Diagram

The EVB is a 300W APFC pre-converter built around the NGPD4102 AC-DC front-end Power Manager and Controller. The board is designed for universal power lines from 85VAC to 265VAC and produces a regulated 380VDC output.

This tool provides the user with

- Hands-on evaluation of all NGPD4102 functions
- Complete development environment
- Application Builder for generating C-code
- Kernel micro-code supplied for core functions
- APFC
- PS Housekeeping functions
- Real-time monitoring and control
- Isolated communications interface to PC

The EVB demonstrates the overall functionality of the NGPD4102 controller, and shows the advantages resulting from the combination of digital flexibility with the high performance and excellent response inherent in analog circuits, namely: high level of performance, fast response, extended flexibility and scalability.

The addition of digital functionality does not adversely impact circuit complexity or PCB size. There is also no need to modify traditional analog APFC stage design rules.

The board is self powered. The internal circuitry of the board is powered from the on-board auxiliary power supply tapped off the mains input.

Fig. 28 below shows a photograph of the working EVB, using the NGPD4102 emulator - housed in a 24-pin DIP package. The emulator is constructed from discrete components on a standard PCB, and encapsulated in an epoxy housing.

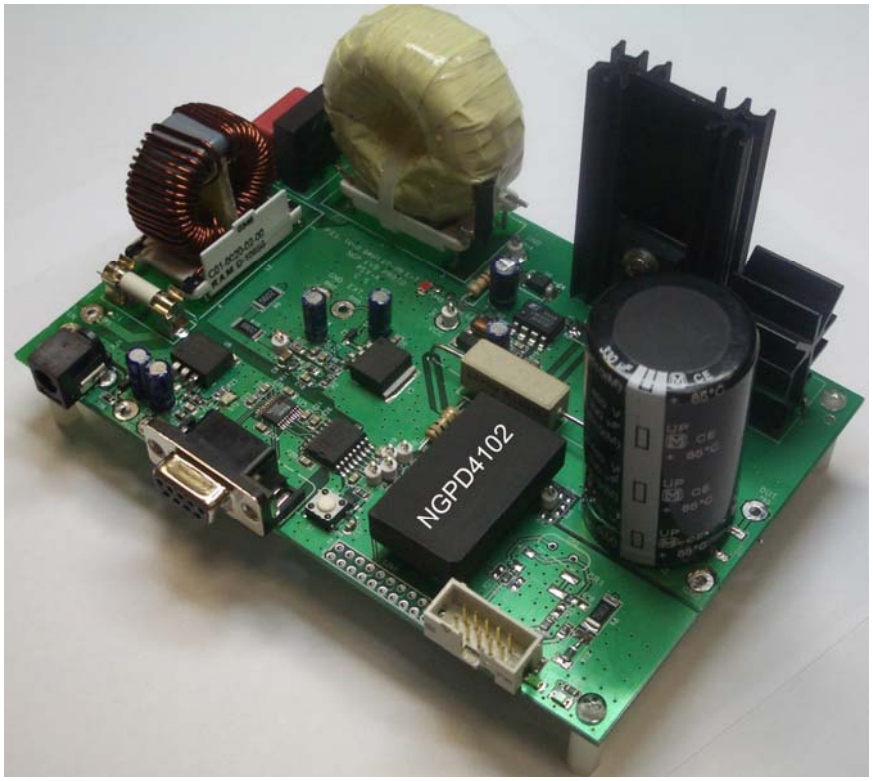


Figure 28: The NGPower EVB using the NGPD4102 emulator

Analog/digital I/Os are provided to allow connection of additional sensors or other devices to the board. This enables the user to test these functions together with the NGPD4102 and easily extend the control capabilities of the power supply.

The board communicates with the computer through an RS232 interface, optically isolated from the power stage. All RS232 circuitry is driven by the on-board powered externally by a separate voltage adaptor for isolation.

All configurable housekeeping functions such as soft-start, brown-out, over-voltage protection, etc. can be tested on the board and fine-tuned via the Graphic User Interface (GUI). The GUI also provides real-time monitoring of the board .

Selected GUI screens are shown in Fig.'s 29 – 30. The GUI interface provides a convenient and simple way to configure and monitor the EVB operation.

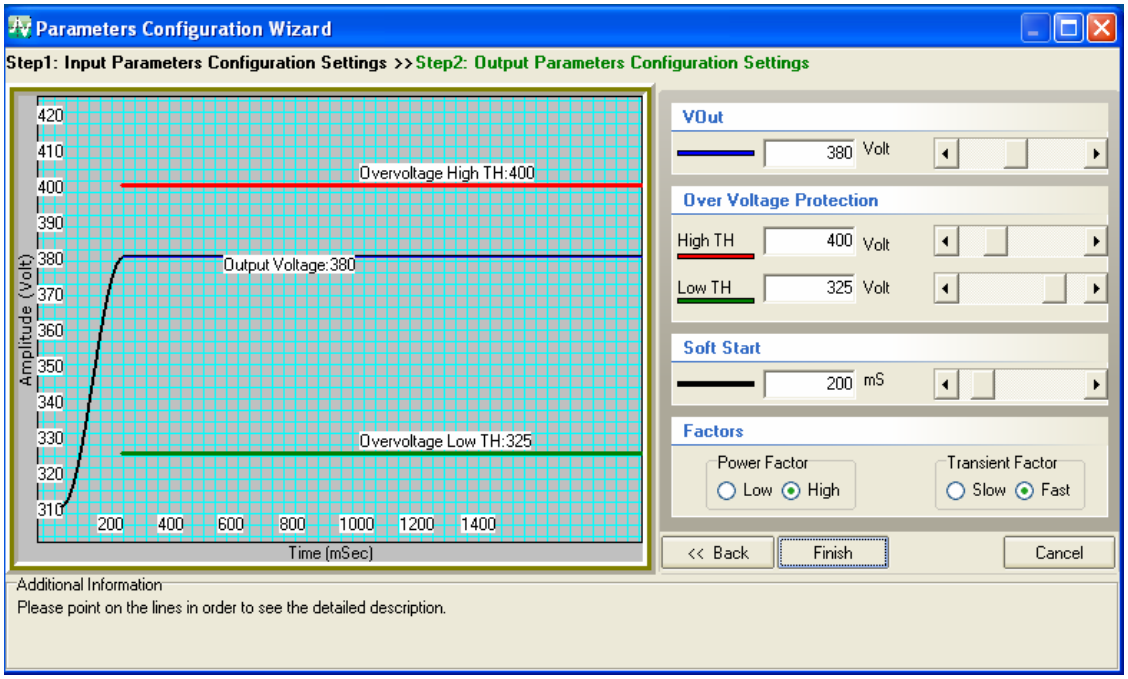


Figure 29: EVB GUI: Input parameters' settings

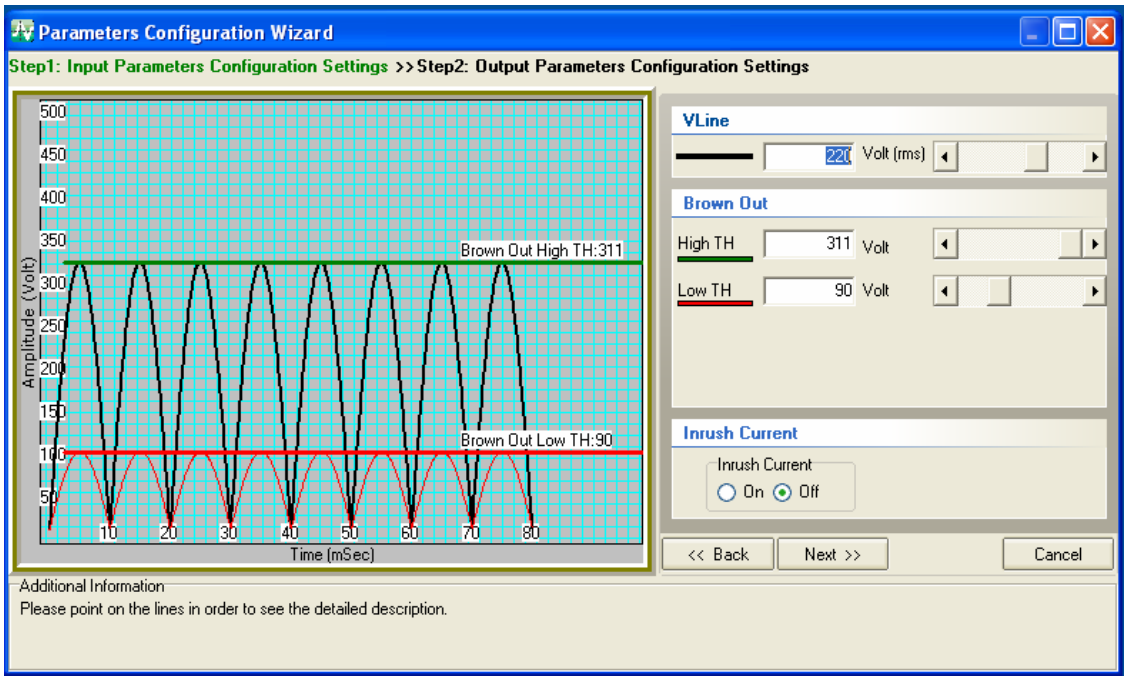


Figure 30: EVB GUI: Output parameters' settings

The process of adapting the basic software to the end-user's application is very straight-forward with the Wizard option of the GUI . Using the Wizard the end-user sets the input parameters (input voltage range, brown-out threshold and inrush current control scheme) and output parameters (output voltage, soft-start and over-voltage threshold). This is done in a 2 step process and the results of the parameter changes are displayed (Fig. 31-32).

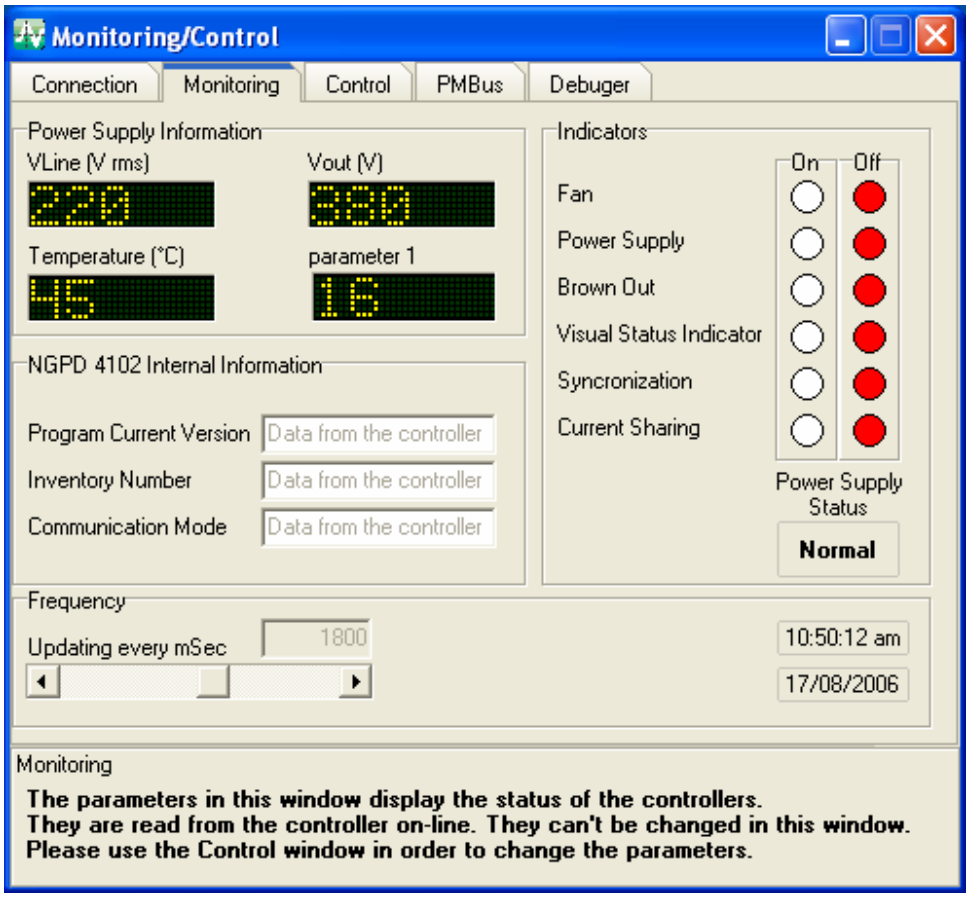


Figure 31: EVB GUI: Real-time parameter monitoring

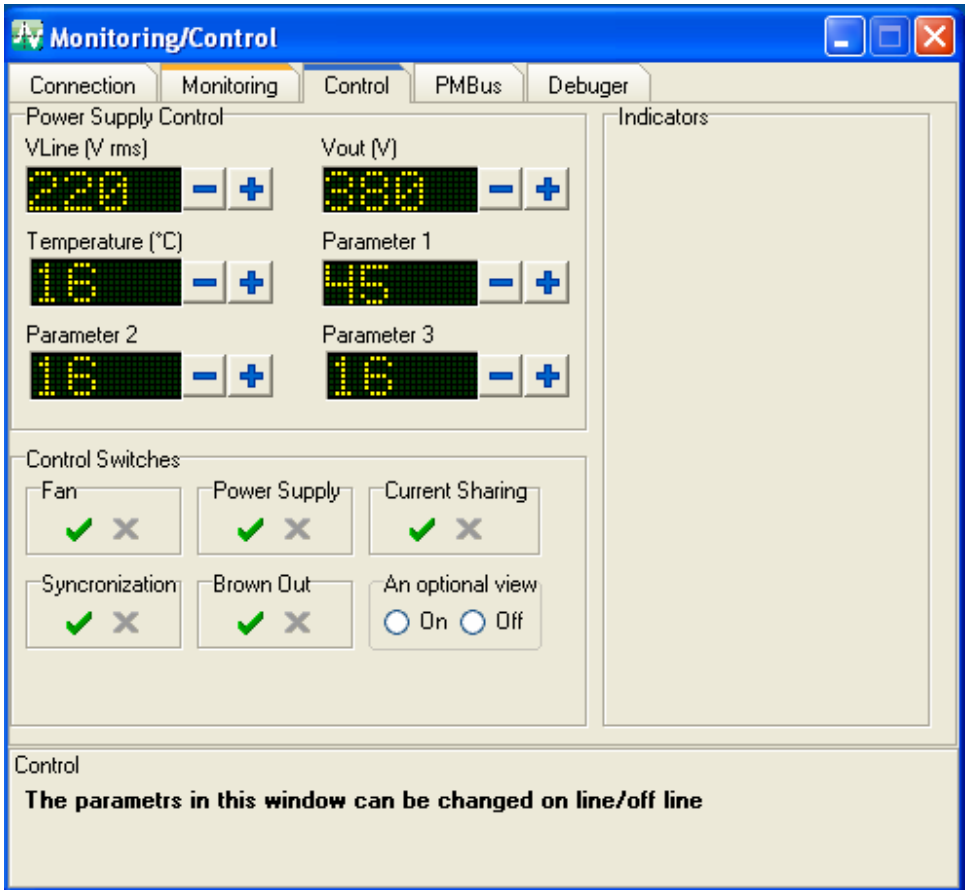
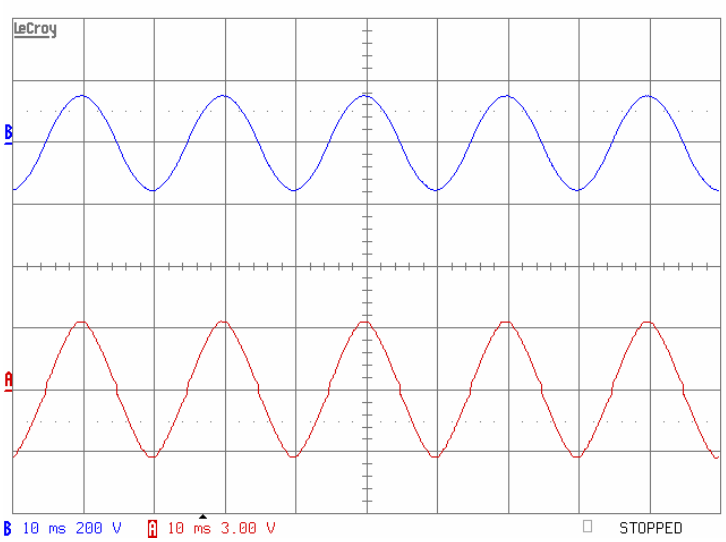


Figure 32: EVB GUI: Real-time parameter control

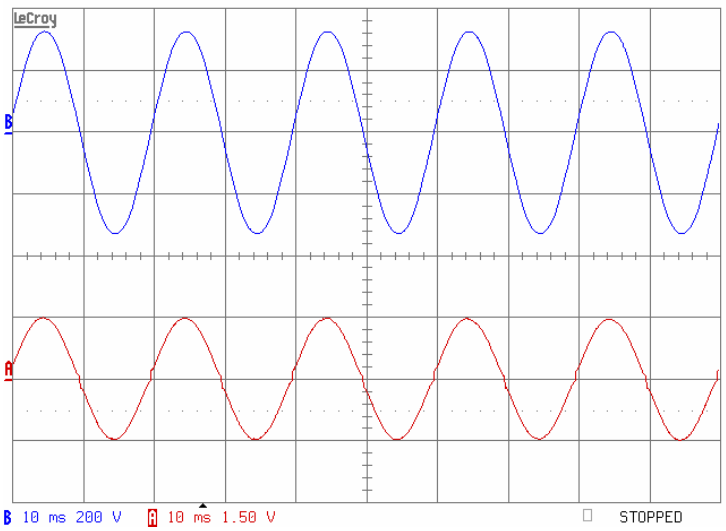
EVB was tested at nominal power levels. Measurements were taken at 110VAC and 230VAC. The plots below show that the input current follows the line voltage almost ideally.

THD of 4.17% and efficiency of 96% was measured when the board was loaded by a 290W load with 230VAC supplied at the input. All these measurements were taken when the board was using the firmware control algorithm.



Upper trace – Line Voltage
Lower trace – Input Current

(a)



Upper trace – Line Voltage
Lower trace – Input Current

(b)

Figure 33: EVB waveforms measured at (a) 110VAC and (b) 230VAC

VI. Discussion and Conclusions

This paper discusses the motivation for developing the NGPower front-end controller NGPD4102, outlines the theory behind the novel PFC control method that is implemented in the IC, and presents test results that were obtained by a hardware emulator. It also presents the NGPower hardware and software tools specially developed to minimize the design effort when using the NGPD4102.

The primary objective of the NGPower mixed mode controller is to provide a comprehensive, high quality and yet economically feasible solution, for the control of the front end of moderate power (150W-1KW) power supplies. This is achieved by applying a novel analog circuit for the inner loop while leaving the outer loop control as well as the housekeeping and communications chores to a simple, low-cost, digital core. A unique feature of the NGPower solution is that the PFC control loop algorithm is supplied as firmware suitable for a wide range of power levels as-is. No additional software development is required for implementation of a fully operational system. Since the analog section of the device performs the major computational effort, considerable computing power is left for additional functions, such as soft-start, inrush current, communications, as well as complete control of specific applications. This was demonstrated by using the device to control an electronic ballast for four fluorescent lamps and the associated PFC circuit.

Test results presented in this paper, confirm the conjecture that a mixed mode solution is the optimal approach to power converters' control. By utilizing the strength of the analog part (PWM generation and current control) the requirements of the digital part are simplified considerably - making the complete solution comparable in cost to pure analog solutions. However, achieving this requires innovative circuits that cannot be obtained by simply combining conventional analog and digital circuits. In fact, such a strategy may lead to the worse of the two worlds, rather than the better.

🕮 References:

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