Control by Emulation: APF Borderline Controller Example

Sam Ben-Yaakov[1] and Ilya Zeltser[2],
Dept. of Electrical and Computer Engineering
Ben-Gurion University of the Negev
Beer-Sheva 84105, ISRAEL

[1] sby@ee.bgu.ac.il , [2] ilyaz@ee.bgu.ac.il
http://www.ee.bgu.ac.il/~pel

ABSTRACT

The Borderline Current Mode (BCM) Active Power Factor Controller (APFC) developed in this study applies a capacitor to emulate the inductor of the power stage and hence the capacitor voltage replicates continuously the inductor current. By this, the instantaneous current of the inductor is available to the controller circuitry without actually measuring it at any given instance. The emulating network is synchronized to the real power system by a zero-crossing signal of the (physical) inductor current. The controller does not include a precision analog multiplier (as some APF BCM controllers do) and does not need to sense the input voltage. An interesting and useful attribute of the proposed controller is its ability to be transformed - by a simple circuit reconfiguration - into a Continuous Current Mode (CCM) APFC controller that also functions without sensing the input voltage.

The paper covers the theoretical aspects of the new controllers family, presents a pre-ASIC discrete-circuit implementation, simulation, and experimental results. The pros and cons of the new controller concept are discussed and possible ways for digital implementation of the new controller concept are suggested.

1. Introduction

Borderline Current Mode (BCM) is considered a favorable solution for Active Power Factor Correction (APFC) [1, 2] in low to medium power applications. This is due to the higher efficiency that can be achieved in comparison to Continuous Conduction Mode, CCM, and Discontinuous Conduction mode, DCM. The higher efficiency is a result of (1) the lower rms current (as compared to DCM) and (2) the negligible diode reverse recovery losses (as comparing to CCM) stemming from the fact that the inductor and diode currents reach zero just before turn-on of the switch.

BCM-APFC control can be achieved in a number of alternative approaches. Some require sensing of input voltage and a precision multiplier [3] while others accomplish the APFC control task without the need to sense the input voltage [4, 5]. Methods that get-by without the sensing of the input voltage are more robust since they are not sensitive to noise that is superimposed on the input voltage (due to switching effects). Methods that do not require a precision multiplier have the advantage of being more economical. This paper presents a new BCM-APFC controller that does not require the sensing of the input voltage, nor does it apply a precision analog multiplier. In addition to presenting an alternative control approach, the study developed a new emulation based concept that might be useful in other power electronics applications.

Control of switch mode systems normally entails the measurement of pertinent system's variables (e.g. output voltage, inductor current) and producing a control signal (such as a duty cycle) to keep the system within the desired operational boundaries. In some cases, direct measurement of a key variable is either impossible or undesirable. This can be overcome by emulating the behavior of the desired variable and estimating its value by sensing the emulating network.

The new APFC-BCM controller developed in this study applies a capacitor to emulate the behavior of the inductor and hence the capacitor voltage replicates continuously the inductor's current. By this, the instantaneous current of the inductor is available to the controller circuitry without actually measuring it at each given instance.

The paper covers the theoretical aspects of the new controllers family, presents a pre-ASIC discrete-circuit implementation, simulation, and experimental results. The pros and cons of the new controller concept are discussed and possible ways for digital implementation of the new controller concept are suggested.

2. Inductor Current Emulation

It has been shown, and implemented in fact in commercial products [6], that one can obtain by emulation the inductor current over the full switching cycle, by measuring the inductor current during the 'on' time only. The inductor current during the 'off' duration can then be replicated by discharging a capacitor. In this case, the capacitor emulates the inductor during the 'off' state and the voltage across it is equal, within a transformation constant, to the inductor current.

Inductor emulation by a capacitor is possible because the state equations of inductors and capacitor have a similar form:

$$\frac{dI_L}{dt} = \frac{V_L}{L} \qquad (1)$$

$$\frac{dV_C}{dt} = \frac{I_C}{C} \qquad (2)$$

where I_L is the inductor current, V_L is the voltage across the inductor, L is the inductance, C is the capacitance, V_C is the voltage across the capacitor and I_C is the current of the capacitor.

Equations (1), (2) imply that an analogy exists between the behavior of the inductor and the capacitor when one interchanges voltage for current and vice versa. In particular, the capacitor's voltage will mimic the inductor's current if, at any given time, the current of the capacitor will be made proportional to the voltage across the inductor. This relationship is illustrated in Fig. 1. Here the capacitor C is fed by a current source I_C, the value of which follows the voltage V_L across the inductor L. In this case the voltage across the capacitor will follow within a proportionality constant the current of the inductor I_L.

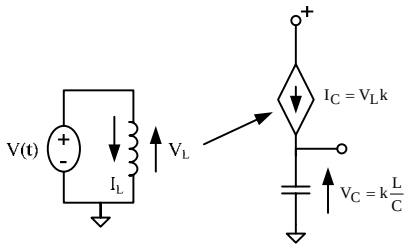

Fig. 1. Inductor and capacitor duality.

Figure 2 illustrates possible a application of this I_L-V_C emulation power. The objective in this case is to emulate the solenoid's L current driven by the switch FET_1. To this end, transistor Q_1 and resistor R are used to convert the voltage across the solenoid to a current, the current is then mirrored by Q_2 and Q_3 and fed to capacitor C.

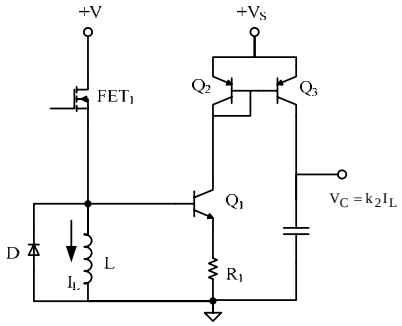

Fig. 2. Emulating an inductor current by voltage across a capacitor.

Consequently, the voltage across the capacitor will be proportional to the current of the inductor. Obviously, one would need to take care of initial conditions. That is, to zero the voltage of the capacitor when the inductor current is zero. A simple circuit that also illustrates the emulation concept for this example is shown in Fig. 3. The voltage across the capacitor will emulate the inductor current if the measurement duration is much shorter than the time constant R_CC.

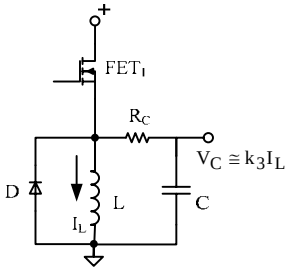

Fig. 3. Emulation concept example.

Aside from the direct I_L to V_C emulation illustrated earlier, one can consider indirect approaches. In the example of Fig. 4, the current of the inductor is emulated by the capacitor's voltage. This is accomplished by subjecting the capacitor to two current sources, corresponding to the voltages of each of the inductor's terminal. One is representing the input voltage and the other the output voltage that appears only during the off duty cycle D'. If this Boost power stage is used as an APFC, then the average input current to the stage, $\langle I_L \rangle$, is proportional to the input voltage V_{in}:

$$I_{in} = \frac{V_{in}}{R_e} \qquad (3)$$

where R_e is the input resistance of the stage. Hence, in this case, the discharging current source I_d (Fig. 4) can be made proportional to the average input current $\langle I_L \rangle$ instead to the input voltage. This is the underlining design concept used in this work.

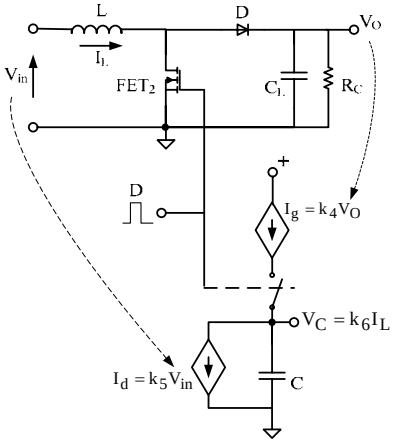

Fig. 4. Converter control by emulation

3. **Method description**

The presented method of BCM APFC borderline control by emulation is based on the APFC control strategy that does not require sensing of the input voltage [7, 8]. For the sake of clarity, the basic relationships of this APFC control method are briefly repeated here. Fig. 5 depicts an arrangement of the APFC converter with no sensing of the input voltage.

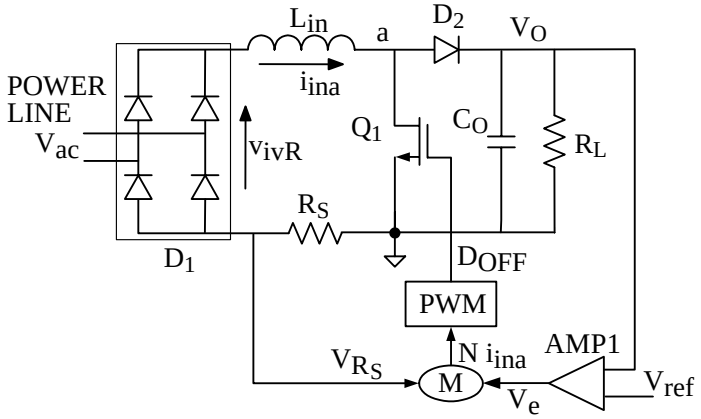

Fig. 5. APFC controller with no sensing of input voltage.

The voltage seen at point 'a' (V_a) is a pulsating voltage of maximum amplitude V_O and duration of T_{OFF} (Fig. 6).

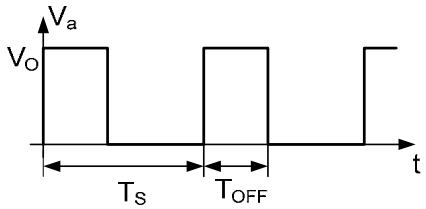

Fig. 6. Instantaneous voltage at the drain of the Q1 (point 'a') of Fig. 5

Consequently, the average voltage at point 'a' (V_a) will be:

$$v_{av} = \frac{V_o \cdot T_{OFF}}{T_S} \qquad (4)$$

where T_S is the PWM switching period and T_{OFF} is a time interval when Q_1 is not conducting.
Or:

$$v_a = V_o D_{OFF} \qquad (5)$$

where

$$D_{OFF} = \frac{T_{OFF}}{T_S} \qquad (6)$$

The 'on' duty cycle D_{ON}, when Q_1 is conducting (During "T_{ON}"), is similarly defined as:

$$D_{ON} = \frac{T_{ON}}{T_S} \qquad (7)$$

The input voltage fed to the Boost converter (V_{ivR}), is assumed to be of low frequency (rectified line voltage) as compared to the switching frequency ($f_S = \frac{1}{T_S}$) and hence can be considered constant over one or several switching periods (T_S). Assuming that the power converter is properly controlled, the average low frequency voltage across L_{in} is close to zero (otherwise the current will run away). This implies:

$$v_{ivR} = v_{av} \qquad (8)$$

where V_{ivR} is the instantaneous low frequency component of V_{ivR}.
Or, from (4)

$$v_{ivR} = V_o D_{OFF} \qquad (9)$$

If D_{OFF} is programmed according to the rule:

$$D_{OFF} = N i_{ina} \qquad (10)$$

where N is a constant and i_{ina} is the low frequency component of the input current (i_{ina}), then:

$$v_{ivR} = V_o N i_{ina} \qquad (11)$$

or:

$$i_{ina} = \frac{v_{ivR}}{V_o N} = \frac{v_{av}}{V_o N} \qquad (12)$$

Assuming that C_O is sufficiently large so that the ripple of V_O can be neglected, equation (12) implies that the input current will follow the input voltage. That is, the converter will look resistive with an apparent input resistance (R_e):

$$R_e = N V_o \qquad (13)$$

which implies that N controls the input resistance R_e:

$$N = \frac{R_e}{V_o} \qquad (14)$$

The value of the input resistance and hence the input current can thus be controlled by varying N. In practical applications, V_O needs to be maintained constant even if the load (R_L) varies. In this control scheme, the output voltage can be maintained constant by closing a feedback loop on N.

Fig. 5 schematically illustrates the control of the duty cycle of the power switch Q_1. Here the voltage that is proportional to the input current (V_{R_S}) as sensed by the resistor R_S is multiplied (M) by the output of an error amplifier (V_e). which is proportional to the deviation of the output voltage V_O from a reference voltage V_{ref}. The output of the multiplier, which is proportional to i_{ina} by a given factor N is fed to a PWM modulator that generates D_{OFF} according to (10). In the circuit of Fig. 5 the PWM modulator is driven by a constant frequency oscillator. Consequently, this method, in its basic form, cannot be utilized for operation in BCM mode.

In the borderline case, the duration T_{OFF} (Fig. 7) is the time it takes the inductor current to drop to zero. Therefore, this period should not be controlled or modified as described above in connection with basic APFC controller with no sensing the input voltage.

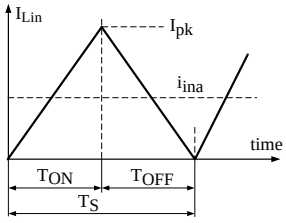

Fig. 7. Inductor current in Borderline Conduction Mode (BCM).

However, D_{OFF} as defined by (6) can still be programmed according to Eq. (10) by adjusting D_{ON}.

One possible way to determine the T_{ON} and T_{OFF} time interval is to predict the time instance when the inductor's current approaches its peak value. This is accomplished in present design by emulating the inductor current waveform by a

capacitor as shown in Fig. 8. Notice that in this case, due to circuit realization considerations that are discussed below, the waveform of the capacitor's voltage is inverted with respect to the inductor's current.

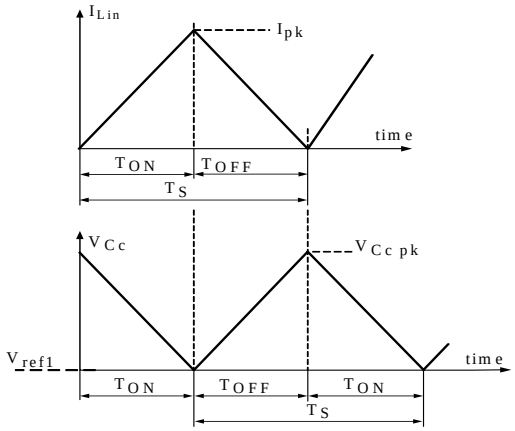

Fig. 8. The current of the inductor of APFC converter (I_{Lin}) and replicated signal with inverted slopes (V_{Cc}).

Hence, the slopes of the lower capacitor's waveform (V_{Cc}) of Fig. 8 are inversely proportional to the slopes of the current of the main inductor (I_{Lin}). As a result, the minimum of V_{Cc} occurs at the peak of I_{Lin}. Assuming that the minimum value of V_{Cc} is known (predefined by the design) the end of the T_{OFF} interval can be set by detecting the instance when the inductor's current reaches zero whereas the end of T_{ON} time interval will be recognized by comparing the inductor's replicated signal V_{Cc} to a predetermined level. In this scheme, the inductor's current is replicated by using the duality between the inductor and the capacitor behavior as described in Section 2. That is, by making the current charging a capacitor C_c to be proportional to the voltage applied to the main inductor, the slope of the voltage across the C_c will be proportional to the slope of the current through the inductor. This is demonstrated in Fig. 9a. It is assumed here that the current source I_{ch} of Fig. 9a is proportional to V_{in} and the current source I_{dch} is proportional to $V_{out.}$ During the "on" time interval the voltage applied across the inductor L_{in} of the boost converter is V_{in}. Similarly, the capacitor C_c in Fig. 9a is charged by the current I_{ch}. During the "off" time the voltage applied to the inductor is (V_{in}-V_{out}) and consequently, the current discharging the capacitor will be I_{ch}-I_{dch}.

In the proposed control method the slopes of the voltage across the emulating capacitor C_c are inversed relative to the slopes of the inductor's current. This can be achieved by switching the charge and discharge current sources of Fig. 9a, as shown on Fig. 9b. That is, during the "on" interval the capacitor C_c is discharged with a slope that is proportional to V_{in} and it is charged with a slope, proportional to (V_{out}-V_{in}) during the "off" interval of the switching cycle. In this way the voltage across the capacitor in Fig. 9b will be similar to the lower trace of Fig. 8. The advantage of this inverse arrangement is that the variable current source ($I_{ch}(V_{in})$)is now referred to ground, which simplifies the circuit implementation as described below.

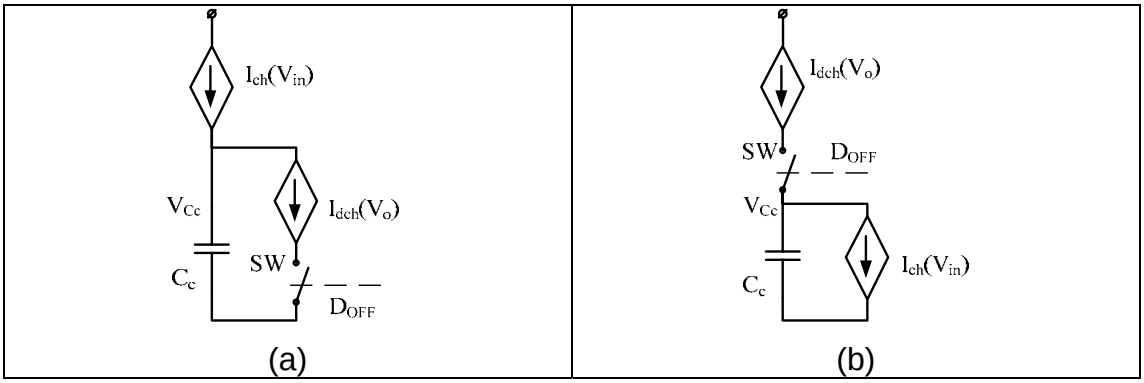

Fig. 9. Replicating the inductor's current.
(a) same slopes and (b) inverted slopes.

The peak voltage of C_C (V_{Cpk}) in Fig. 89b can be calculated from duration T_{OFF} and duration T_{ON}:

$$V_{Cpk} = \frac{\left(I_{dch}(Vout) - I_{ch}(V_{in})\right)}{C_c} \cdot T_{OFF} \qquad (15)$$

$$V_{Cpk} = \frac{I_{ch}(V_{in})}{C_c} \cdot T_{ON} \qquad (16)$$

from which:

$$(T_{OFF} + T_{ON}) \cdot I_{ch}(V_{in}) = T_{OFF} \cdot I_{dch}(V_{out}) \qquad (17)$$

since $T_{OFF} + T_{ON} = T_S$ (18)

one finds:

$$D_{OFF} = \left(\frac{1}{I_{dch}(V_{out})}\right) I_{ch}(V_{in}) \qquad (19)$$

In a given operating conditions the output voltage V_{out} remains constant and hence the $I_{dch}(V_{out})$ will be constant. Assuming that the converter of Fig. 5 is operated as APF stage, its input average current i_{ina} follows the input voltage V_{in}, and therefore the current source $I_{ch}(V_{in})$ can be made to be proportional to i_{ina}, that is:

$I_{ch}(V_{in}) = k \cdot i_{ina}$ (20)

Equation (19) can therefore be rewritten as follows:

$$D_{OFF} = \left(\frac{k}{I_{dch}(V_{out})}\right) \cdot i_{ina} \qquad (21)$$

Comparing Eq. (21) to Eq. (10), it is evident that the control circuitry of Fig. 9b follows the programming rule determined by Eq. (10).

4. Implementation

a. Analog approach

The converter of Fig. 10 illustrates one possible practical way to apply the control concept of Fig. 9b to the borderline APFC stage.

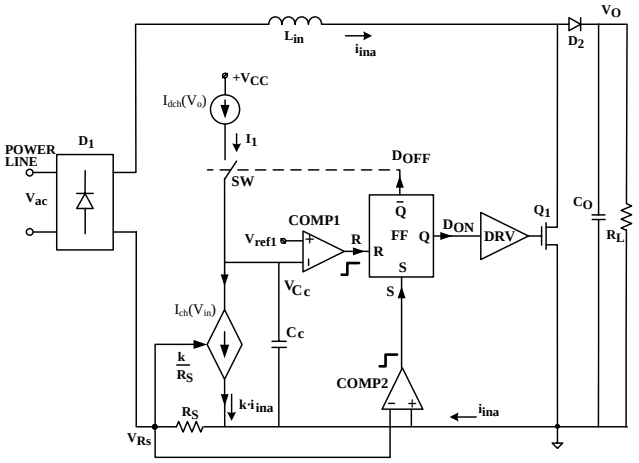

Fig. 10. Application of indirect inductor current emulation in BCM APFC stage.

The circuit includes two current sources that feed a capacitor C_C: an independent current source $I_{dch}(V_{out})$ that produces a current I_1 and a dependent current source $I_{ch}(V_{in})$ that produces a current that is proportional to the average of the input current i_{ina} (i.e. $k \cdot i_{ina}$). The dependent current source $I_{ch}(V_{in})$ is controlled by the voltage across the sense resistor R_S of i_{ina}. The current source $I_{dch}(V_{out})$ is connected to the capacitor via a switch SW that is conducting during the period T_{OFF}. The signal Doff for the duration T_{OFF}, as well as the complementary signal D_{ON}, are produced by a flip-flop FF whose Q state corresponds to D_{ON} while $\overline{Q}$ corresponds to Doff. The FF is set and reset by two comparators. Comparator Comp1 produces a reset signal whenever the capacitor voltage (V_{C_C}) drops below a reference voltage (V_{ref1}). The FF is set when the input current drops to zero. The set signal for the FF is generated by comparator Comp2 when the voltage across the sense resistor R_S drops to zero. Under normal operating conditions, the capacitor C_C is charged from level V_{ref1} by a current ($I_1 - k \cdot i_{ina}$) and discharged by $k \cdot i_{ina}$ to return to V_{ref1}.

The relationship between the voltage across C_C (V_{C_C}) and the inductor current (i_{ina}) is as depicted in Fig. 8.

Duration T_{OFF} is triggered whenever the voltage of C_C drops to the level of Vref1, while duration T_{ON} is triggered whenever the inductor's current drops to zero. Since the power switch is turned on only after the inductor current drops to zero, the operation is in BCM.

In a practical application, the input resistance of the APFC converter (Re) needs to be adjusted so as to comply with the power requirement of the load. This can be done by controlling the proportionality constant N of (10). From (10), (13) and (17) we find:

$$\frac{k}{I_1} = \frac{R_e}{V_o} \qquad (22)$$

Namely:

$$R_e = \frac{k}{I_1} V_o \qquad (23)$$

Equation (23) implies that either controlling k or I_1 can adjust the input resistance (Re).

Fig. 11 illustrates a possible solution for controlling variable 'k'. This is accomplished by applying an error amplifier AMP1 that produces a signal that is proportional to the deviation of the output voltage (as measured via the divider R1, R2) from a reference voltage V_{ref3}.

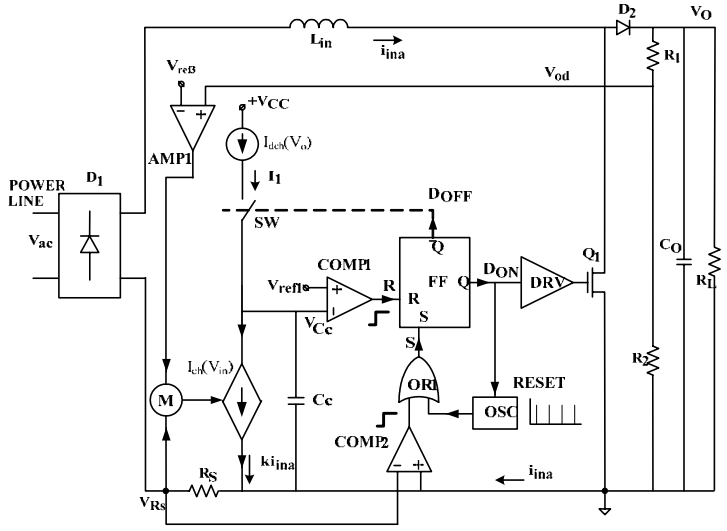

Fig. 11. Changing the input impedance of the APFC stage by varying the 'k' coefficient.

The amplified error signal is fed to one input of an analog multiplier M, while VRs, being proportional to i_{ina}, is fed to another input of this analog multiplier. This allows to control the coefficient 'k' of the dependent current source $I_{ch}(V_{in})$ which changes so as to keep the output voltage (V_O) constant, i.e., to balance the input and output power. It is of significance out that the multiplier that controls the coefficient 'k' is placed in the feedback control loop that is responsible for keeping the output voltage at some predefined nominal value. If, by any reason, the value of 'k' will not be as expected the output voltage will depart from its nominal value. In this case the error in the output voltage will be recognized by the error amplifier AMP1 and 'k' will be corrected accordingly. This implies that the precision and the linearity of the multiplier M are of no importance and consequently even a very simple and low cost analog multiplier can be chosen for this application.

Although the above description discusses a BCM APF operation, it equally applies to a CCM APFC stage - also without sensing the input voltage – as shown in Fig. 12.

In this case the zero inductor-current detection circuitry is replaced by a constant frequency oscillator.

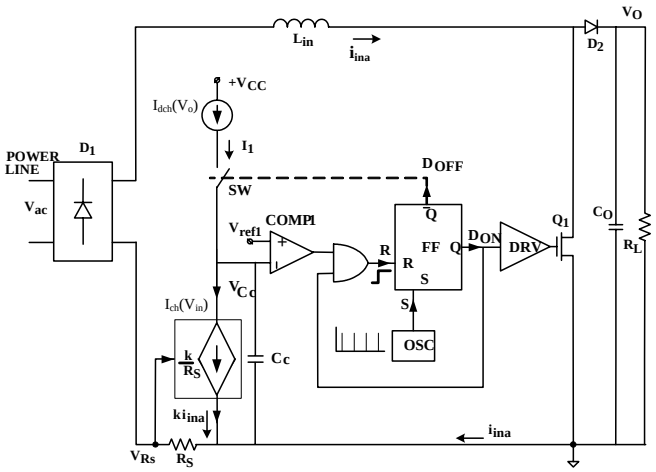

Fig. 12. Implementation of the proposed control technique in the realization of a CCM APF stage.

Since Eq. (21) still holds, the converter of Fig. 12 functions as an APFC even if the inductance of L_{in} is large, forcing the converter to operate in CCM mode. In this case, the flip-flop FF is set to the 'High' state (i.e. Q='High') at constant intervals as determined by the Clock of a constant frequency oscillator OSC, of which frequency is so predetermined as to force the converter to operate in CCM mode.

It is thus clear that essentially the same electronic circuit elements can be utilized for either operating the converter in CCM mode or in BCM mode. Switching between these two modes could be implemented by a minor hardware change and/or by proper software and/or by configuring the oscillator OSC according to the desired mode of operation.

In practical realization of the CCM scheme, one may need to introduce slope compensation to overcome the possible onset of sub-harmonic oscillations. The slope compensation could be formed by adding, for example, a triangular waveform to the voltage V_{ref1} in Fig. 12.

b. Digital Implementation

According to the proposed control scheme, the implementation of APFC converter requires the use of a capacitor C_C that is sequentially charged and discharged in each switching cycle. The size of this capacitor is a function of the charging current magnitude and the available dynamic range, i.e., the voltage range that can be handled in a given system. In some cases, the required value of the capacitor may be too large for implementation on an electronic chip, thus becoming a limitation whenever a microelectronics solution is desired. Another practical problem that may deteriorate the performance of an APFC system built according to the suggested analog control scheme is the typical inherent interference of a switch mode system due to spikes. The spikes may cause false triggering of the comparators used in the analog implementation described above.

An alternative approach to realize a capacitor behavior is by a digital counter. In this case counting up will represent charging and counting down, discharging and digital comparators will replace the analog comparators. This will overcome the problem of analog comparators sensitivity to noise.

Fig. 13 illustrates schematically a general functioning and layout of a power factor correction circuit that utilizes a digital controller.

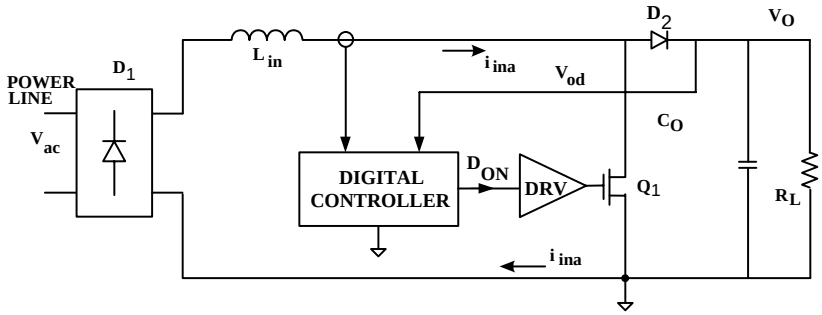

Fig. 13. A general functioning and layout of a digital APFC controller.

The Digital Controller receives signals that are proportional to the input current (i_{ina}) and output voltage (V_O), and generates the required gate signals for the switch Q_1. The algorithm utilized by the digital controller emulates the charge and discharge comparison scheme relating to the analog embodiments.

It should be pointed out that the suggested control methodology is inherently compatible with microelectronic technology. Digital implementation is advantageous, since several housekeeping circuits which are normally required in a power supply, such as overload protection, shortening or disconnecting the outputs, softstart etc. can be easily implemented in the digital controller.

5. Simulation model and simulation results

A simulation model of an APFC converter controlled according to the proposed control technique was developed (Fig. 15).

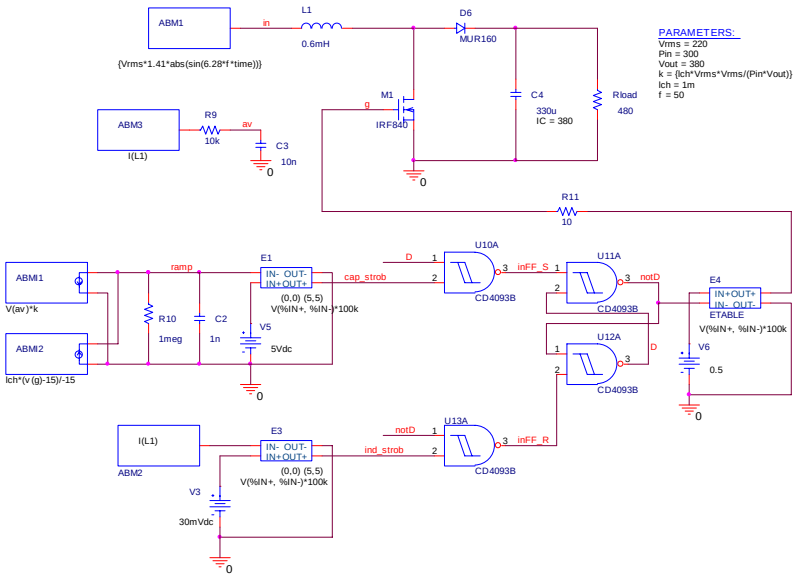

Fig. 15. Cycle-by-cycle simulation model of BCM APF stage.

The rectified line voltage is generated in this simulation model by the behavioral voltage source ABM1. The current of the main inductor L1 is smoothed by the low pass filter R9, C3 to reconstruct its low frequency component (node "av"). This signal is further used by dependent current source ABMI1 that discharges the emulating

capacitor C2. The capacitor C2 is charged by the current source ABMI2. The voltage across the capacitor is compared to the reference of 5V (V5) by the behavioral voltage source E1 that serves as a comparator. This comparator generates the "set" signal that is provided to a flip-flop based on two "NAND" gates U11A and U12A. The reset signal for this flip-flop is generated by the comparator E3 that senses the current of the main inductor and compares it to the reference that is very close to zero (about 30mA). The output of the flip-flop is provided to the gate of the main transistor M1 through the level shifting driver implemented on behavioral voltage source E4.
Fig. 24 illustrates the simulated input voltage, input current and average input current of the simulation model of Fig. 15.

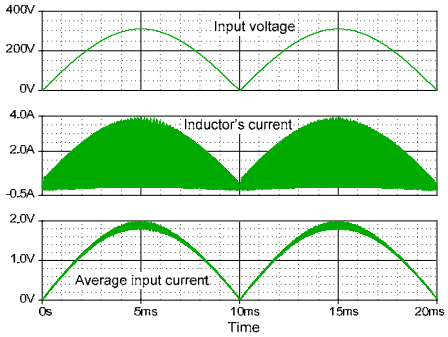

Fig. 16. Simulated input voltage, input current and average input current.

As clearly observed in Fig. 16, the low frequency component of the input current follows the input voltage in time and amplitude proportionality, assuring thereby a unity power factor.

6. Experimental setup and results

The proposed BCM APFC control methodology (Fig. 17) was implemented as shown in Fig. 17.

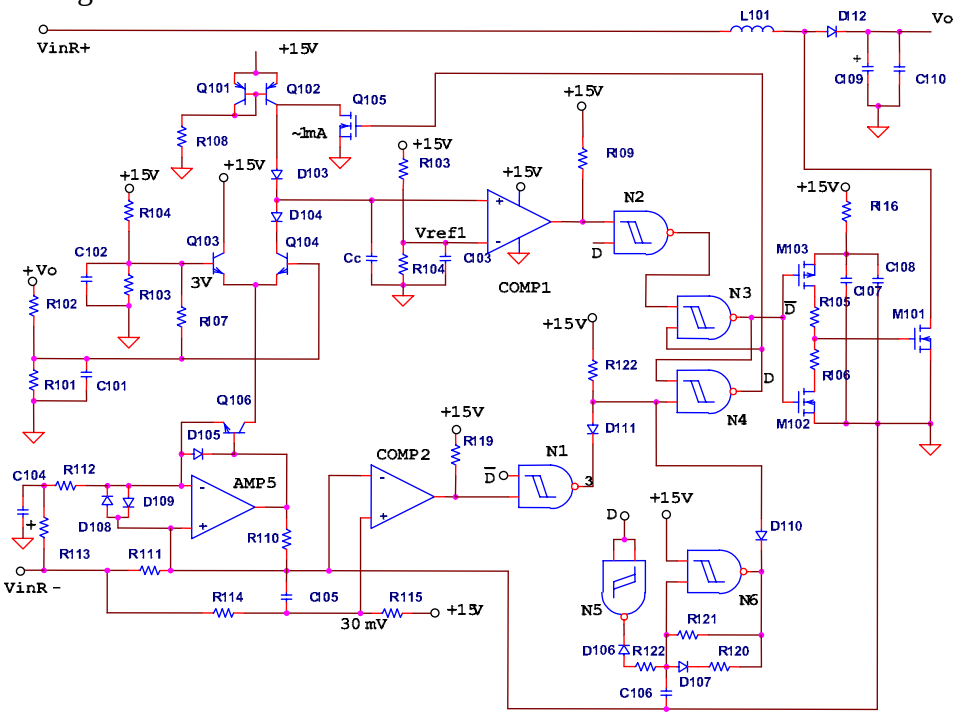

Fig. 17. Experimental circuit implementation of the proposed BCM APFC control method.

The circuit follows the concept of controlling variable ‘k’ as demonstrated in Fig. 11. The input current is sensed by R111, filtered out by R113, C104 and translated to the collector of Q106. The pair Q103, Q104 and Q106 form a low cost two quadrant multiplier such that the current at the collector of Q104 is controlled by the error signal formed by subtracting from a voltage proportional to the out Vo, the reference voltage at the junction of R103, R104. Thus the collector current of Q104 is controlled by the deviation of V_O from desired level. The I_1 source is generated by the current mirror pair Q101, Q102. The current I_1 forced by Q102 is switched by Q105 such that during D_{ON} I_1 is shorted to ground and it does not charge C_C. C_C is thus charged and discharged according to the programming rule (15, 16). The triggers for the FF are obtained by comparators COMP1 and COMP2 (LM393) that detect when C_C discharge reaches V_{ref1} and by COMP2 that detects when the input current drops to zero. In order to reduce the risk of false triggering due to the switching noise, the voltage across the sense resistor R111 is filtered out by R114 and C105 and a small offset of about 30mV (equivalent to about 60mA of the inductor's current) was added to the positive terminal of the comparator. The FF is formed by two NAND gates N3, N4.

An independent oscillator that is build around the gate N6 is utilized to initiate and/or trigger the circuit at start-up or in a case of deadlock (i.e., resuming normal operation). The frequency of the oscillator is designed to be below the range of operating frequencies of the converter. If the converter is operating properly the capacitor C106 of the oscillator is discharged by the gate N5 at every switching cycle so the oscillator is inoperative under normal operating conditions.

The rest of the circuit: gate drivers M102, M103, etc., follow the standard design practice.

The circuit of Fig. 17 was operated form an AC voltage source at 300W power level. The input voltage was 230Vrms and the output voltage was about 380V. The main inductor (L101) and the output capacitor (C109) were 0.6mH and 220 μF respectively.

Figs. 18 and 19 present the drain voltage of the main transistor M101, the high frequency current of the main inductor L101 and the voltage across the emulating capacitor C_C.

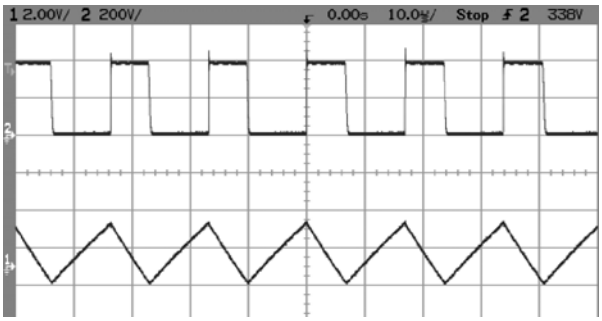

Fig. 18. Drain voltage and inductor’s current of the presented APFC stage.
Vin=230Vrms; Vout=386V; Pout=300W
Upper trace: Drain voltage: 200V/div
Lower trace: Input current: 2A/div
Horizontal scale: 10µS/div

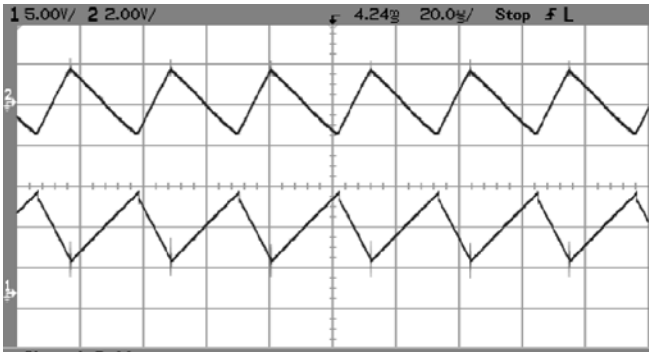

Fig. 19. Inductor's current vs. the voltage across the emulating capacitor.
Upper trace: input current (2A/div)
Lower trace: voltage on the emulating capacitor (5V/div)
Horizontal scale: 20μS/div

The input behavior of the proposed converter is shown in Fig. 20.

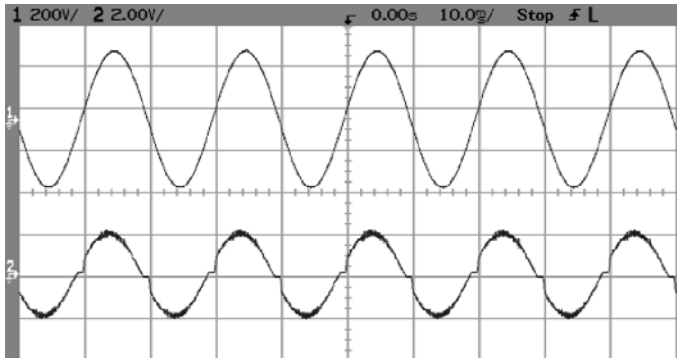

Fig. 20. Input behavior of the stage
Vin=230Vrms; Vout=386V; Pout=300W
Upper trace: input voltage – 230Vrms
Lower trace: input current 2A/div
Horizontal scale: 10mS/div

7. Conclusions

A new BCM APFC controller was developed, theoretically analyzed, simulated and tested experimentally. The unique features of the controller are that it applies inductor-capacitor emulation to reconstruct the inductor's temporal current waveform and that it does not require the sensing of the input voltage. Another important and practical attribute of the controller is the ability to also operate in CCM. Toggling between BCM and CCM can be implemented by a minor hardware change. This makes it possible to operate an APFC stage in dual mode: BCM at low power levels and CCM at higher power levels. The advantage of this adaptable operation would be an increase of overall efficiency. BCM has higher efficiency at lower power levels due to the lower losses at turn on. This advantage is overridden at high power levels by the high rms losses. This is why at higher power levels CCM is preferred. Hence, the ability of the controller to operate in an adaptive mode would increase the efficiency over an extended power level.

The experimental controller demonstrates the simplicity of the circuit that is compatible with both analog and digital implementations. Furthermore, the fact that

the circuit does not call for sophisticated module, such as a precision multiplier, attest to the fact that ASIC realization would lead to a low cost IC.

References

[1] Petreus, D., Ciocan, I., and Farcas, C., "Average current mode control versus borderline current mode control on power factor correction circuits," *29th International Spring Seminar on Electronics Tchnology, ISSE'06*, 2006, pp. 262-267.

[2] Abramovitz, A., "Effect of the Ripple Current on Power Factor of CRM Boost APFC," *CES/IEEE 5th International Conference on Power Electronics and Motion Control,. IPEMC '06.* 2006 Vol. 2, pp. 1-4.

[3] ON Semiconductor, "MC33232: Power factor controller," *ONSeimconductor*, 2007. [Online]. Available: http://www.onsemi.com/pub/Collateral/MC33232-D.PDF. [Accessed: Aug. 20, 2007].

[4] Texas Instruments, "UC1852: High power-factor preregulator," *Texas Instruments*, 1999. [Online]. Available: http://focus.ti.com/lit/ds/symlink/uc1852.pdf. [Accessed: Aug. 20, 2007].

[5] ON Semiconductor, "MC33260: GreenLine CompactPower Factor Controller: Innovative Circuit for Cost Effective Solutions," *ON Semiconductor*, 2007. [Online]. Available: http://www.onsemi.com/pub/Collateral/MC33260-D.PDF. [Accessed: Aug. 20, 2007].

[6] Texas Instruments, "UC2849: Secondary side average current mode controller," *Texas Instruments*, 1995. [Online]. Available: http://focus.ti.com/lit/ds/symlink/uc2849.pdf. [Accessed: Aug. 20, 2007].

[7] Ben-Yaakov, S., and Zeltser, I., "The dynamics of a PWM boost converter with resistive input," *IEEE Trans. Industrial Electronics*, 1999, vol. 46, pp. 613-619.

[8] Ben-Yaakov, S., and Zeltser, I., "PWM converters with resistive input," *Power Conversion and Intelligent Motion, PCIM-98*, 1998, pp. 87-95.