Generic and Unified Model of Switched Capacitor Converters

Sam Ben-Yaakov
Senior member, IEEE

Michael Evzelman
Student member, IEEE

Power Electronics Laboratory
Department of Electrical and Computer Engineering
Ben-Gurion Univ. of the Negev
P.O. Box 653, Beer-Sheva, 84105 Israel
sby@ee.bgu.ac.il; evzelman@ee.bgu.ac.il
Website: www.ee.bgu.ac.il/~pel/

Abstract -- A generic modeling methodology that analyzes the losses in Switched Capacitors Converters (SCC) was developed and verified by simulation and experiments. The proposed analytical approach is unified, covering both hard and soft switched SCC topologies. The major advantage of the proposed model is that it expresses the losses as a function of the currents passing through each flying capacitor. Since these currents are linearly proportional to the output current, the model is also applicable to SCC with multiple capacitors. The proposed model provides an insight into the expected losses in SCC and the effects of their operational conditions such as duty cycle. As such, the model can help in the optimization of SCC systems and their control to achieve desired regulations.

I. Introduction

Switched Capacitor Converters (SCC) suffer from a fundamental power loss deficiency which makes their use in some applications prohibitive. The power loss is due to the inherent energy dissipation when a capacitor is charged or discharged by a voltage source or another capacitor [1, 2]. Two types of SCC have been considered in the literature, hard and soft switched SCC. The soft switched SCC employ a series inductor to achieve zero current switching [3, 4]. Previous studies that analyze losses in SCC covered separately the hard switching case [1, 2, 5-7], or the soft switching case [3]. A comparison between the two was carried out in [4]. However, in [4] the analysis for the soft switched SCC was carried out under the first harmonics approximation while in this study we present a closed form solution of the losses both for the hard switched and the soft switching case. This paper presents a generic model that applies to both hard and soft switched SCC. The major advantage of the model presented here is that it expresses the losses as a function of the current passing through each flying capacitor. Since these currents are linearly proportional to the output current, the proposed model can be applied to derive the losses of SCC with multiple capacitors.

II. Inherent Switched Capacitors Losses: Hard Switching Case

For the sake of clarity we consider first the case of a 1:1 SCC depicted in Fig. 1. The analysis is made under the assumption that the input voltage, V_{in}, and output voltage, V_o, are constant over a switching cycle, the switches S_1 and S_2 have "on" resistances of R_{S1} and R_{S2} respectively, the capacitor, C, has a series loss component R_{ESR} and that the switches connect the capacitor C to V_{in} and V_o during the times t_1 and t_2 respectively. The switching frequency is f_s and the switching period $T_s = 1/f_s$. Note that due to possible dead time between switch transitions the total duration $t_1 + t_2$ may be smaller than T_s. The generic charge/discharge process can be represented by the basic equivalent circuit of Fig. 2, in which ΔV is the initial voltage difference between the capacitor and the corresponding voltage source (V_{in} or V_o) and R is the total resistance of the loop (switch resistance and capacitor's ESR).

The energy loss E_R during the time t_1 will be:

$$E_R = \frac{\Delta V^2 \cdot C}{2} \cdot (1 - e^{-2\beta}) \quad (1)$$

where $\beta = t_1/RC$. The charge Q transferred during t_1 is calculated to be:

$$Q = \Delta V \cdot C \cdot [1 - e^{-\beta}] \quad (2)$$

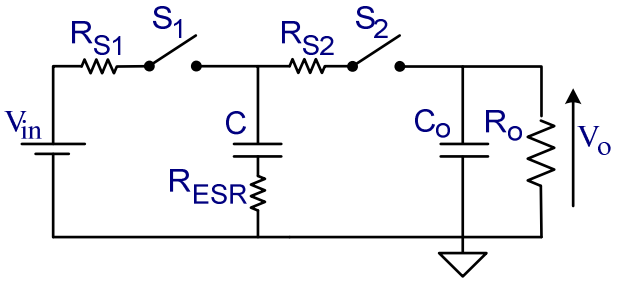


Fig. 1: Hard switched 1:1 SCC.

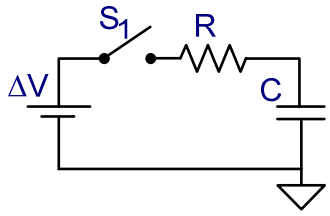


Fig. 2: Equivalent circuit of charge/discharge process.

Relating these results to the SCC of Fig. 1 the energy loss during t_1, E_1, and during t_2, E_2, will be:

$$E_1 = \frac{\Delta V_1^2 \cdot C}{2} \cdot (1 - e^{-2\beta_1}) \quad (3)$$

$$E_2 = \frac{\Delta V_2^2 \cdot C}{2} \cdot (1 - e^{-2\beta_2}) \quad (4)$$

where ΔV_1, ΔV_2 are the initial voltage differences during the time periods t_1 and t_2 respectively and β_1, β_2 are the relevant exponents for each case.

In steady state, the charge Q, transferred by each switch is identical and equal to:

$$Q = \Delta V_1 \cdot C \cdot [1 - e^{-\beta_1}] = \Delta V_2 \cdot C \cdot [1 - e^{-\beta_2}] \quad (5)$$

For switching frequency f_s the (identical) average capacitor currents, I_{Cav} transferred through each switch are:

$$I_{Cav} = f_S Q = f_S \Delta V_1 \cdot C \cdot [1 - e^{-\beta_1}] = f_S \Delta V_2 \cdot C \cdot [1 - e^{-\beta_2}] \quad (6)$$

The initial voltage differences ΔV_1, ΔV_2 can now be expressed as a function of the average current:

$$\Delta V_1 = \frac{I_{Cav}}{f_S C \cdot [1 - e^{-\beta_1}]} \quad (7)$$

$$\Delta V_2 = \frac{I_{Cav}}{f_S C \cdot [1 - e^{-\beta_2}]} \quad (8)$$

Replacing ΔV_1 and ΔV_2 in (3) and (4) by (7) and (8) and adding them up yields:

$$E_R = E_1 + E_2 = \left(\frac{I_{Cav}}{f_S C}\right)^2 \cdot \frac{C}{2} \cdot \left[\frac{(1 + e^{-\beta_1})}{(1 - e^{-\beta_1})} + \frac{(1 + e^{-\beta_2})}{(1 - e^{-\beta_2})}\right] \quad (9)$$

The total power loss of the circuit P_T can now be calculated from the total energy loss (E_1+E_2) by multiplying it by f_s:

$$P_T = (I_{Cav})^2 \cdot \left\{\frac{1}{2 f_S C} \cdot \left[\frac{(1 + e^{-\beta_1})}{(1 - e^{-\beta_1})} + \frac{(1 + e^{-\beta_2})}{(1 - e^{-\beta_2})}\right]\right\} \quad (10)$$

The above expression is valid for a SCC with two charge/discharge phases. Multi phase cases are discussed in section 5.

III. Inherent Switched Capacitors Losses: Soft Switching Case

We commence the examination of the soft switched SCC by considering again the simple 1:1 converter case of Fig. 3, which reduces to the generic network of Fig. 4. In this case we find:

$$E_R = \frac{\Delta V^2 \cdot C}{2} \cdot \left(1 - e^{-2\pi \frac{\alpha}{\omega_d}}\right) \quad (11)$$

where:

$$\omega_0 = \sqrt{\frac{1}{LC}}, \alpha = \frac{R}{2L}, \omega_d = \sqrt{\omega_0^2 - \alpha^2}, R = R_{ind} + R_{ESR} + R_S, \text{(Fig.3)}$$

Since the analysis is focused on soft switching operation, it is assumed that the switching period is longer than half of circuit's damped oscillation period, and that the quality factor of the effective RLC circuit is higher than 1/2. In this case, the charge, Q_C, transferred to and from the capacitor during both charging and discharging phases of the SCC, is found to be:

$$Q_c = \Delta V_{1,2} \cdot C \cdot (1 + e^{-\pi \frac{\alpha}{\omega_{d(1,2)}}}) \quad (12)$$

Where subscripts 1 and 2 denote the two phases. The charge Q_c, which is transferred to the capacitor from the source, is then transferred by the capacitor to the load, so the current to the load, I_O, will be the average charge during either charging or discharging half cycle of converter's operation. Applying the relationship $Q_C \cdot f_S = I_{C(avg)}$, ΔV can be expressed as:

$$\Delta V_{1,2} = \frac{I_{C(avg)}}{f_S C \cdot (1 + e^{-\pi \frac{\alpha}{\omega_{d(1,2)}}})} \quad (13)$$

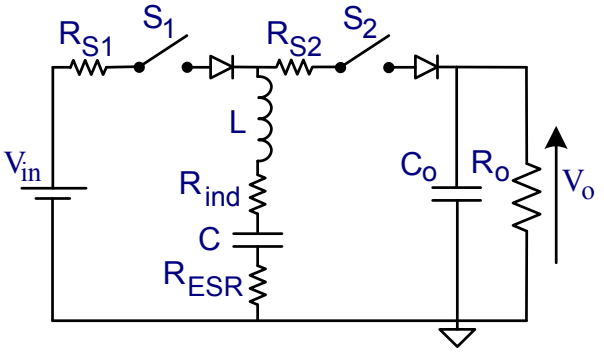


Fig. 3: Soft switched 1:1 SCC.

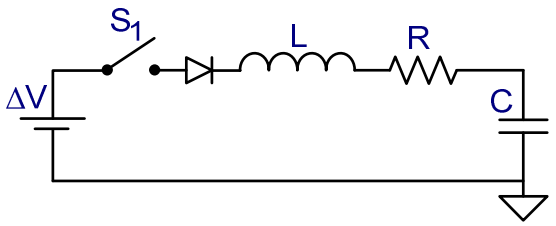


Fig. 4: Equivalent circuit of resonant charge/discharge process.

Substituting the value of voltage ripple (13) into energy dissipation equation (11) results in:

$$E_{R(1,2)} = \left(\frac{I_{C(avg)}}{f_S C}\right)^2 \cdot \frac{C}{2} \cdot \frac{(1 - e^{-\pi \frac{\alpha}{\omega_{d(1,2)}}})}{(1 + e^{-\pi \frac{\alpha}{\omega_{d(1,2)}}})} \quad (14)$$

Combining the energy dissipated during charging – $E_{R(1)}$ and discharging – $E_{R(2)}$ periods, and multiplying them by the switching frequency, yields the total power dissipation due to the conduction losses of the resonant, or soft switching converter – $P_{T(res)}$:

$$P_{T(res)} = I_{Cav}^2 \cdot \left\{\frac{1}{2Cf_S} \cdot \left[\frac{(1 - e^{-\pi\zeta_{d(1)}})}{(1 + e^{-\pi\zeta_{d(1)}})} + \frac{(1 - e^{-\pi\zeta_{d(2)}})}{(1 + e^{-\pi\zeta_{d(2)}})}\right]\right\} \quad (15)$$

where: $\zeta_{d(1)} = \frac{R_1}{2\omega_{d(1)}L}$; $\zeta_{d(2)} = \frac{R_2}{2\omega_{d(2)}L}$

The above expression assumes that the switching time in each phase is equal or larger than the sum of the dead time and the interval π / ω_d (half of the circuit damped period).

IV. The Generic Equivalent Circuit Model

Examination of the power loss in the hard and soft switching cases (10, 15) reveals that they can be expressed as a resistor loss, as shown in previous publications for the hard switching case [5-8]. Since the load current is supplied by the flying capacitors, it is inevitable that the relationship between the charges passing through a capacitor during each switching stage, and the output current will be linear. Consequently in SCC systems the average flying capacitors' current I_{Cav} is linearly proportional to the output current I_o:

$$I_{C_{av}} = k \cdot I_o \quad (16)$$

This implies that the losses could be modeled as the losses of an equivalent resistor R_e connected in series with the output, as shown in Fig. 5. The value of the equivalent voltage source V_e is the open circuit voltage of the SCC. That is, the no load output voltage, often referred to as the "target voltage" of the converter. The value of the equivalent resistance for the hard switched 1:1 case (for which k=1) derived form (10) will be:

$$R_e = k^2 \cdot \frac{1}{2Cf_S} \cdot \left[\frac{(1 + e^{-\beta_1})}{(1 - e^{-\beta_1})} + \frac{(1 + e^{-\beta_2})}{(1 - e^{-\beta_2})}\right] = \frac{1}{2f_S C} \cdot \left[\coth\left(\frac{\beta_1}{2}\right) + \coth\left(\frac{\beta_2}{2}\right)\right] \quad (17)$$

and for the soft switched 1:1 case derived from (15) is:

$$R_{e(res)} = k^2 \cdot \frac{1}{2Cf_S} \cdot \left[\frac{(1 - e^{-\pi\zeta_{d(1)}})}{(1 + e^{-\pi\zeta_{d(1)}})} + \frac{(1 - e^{-\pi\zeta_{d(2)}})}{(1 + e^{-\pi\zeta_{d(2)}})}\right] = \frac{1}{Cf_S} \cdot \left[\tanh\left(\frac{\pi\zeta_{d(1)}}{2}\right) + \tanh\left(\frac{\pi\zeta_{d(2)}}{2}\right)\right] \quad (18)$$

For the 1:1 SCC, k = 1 and $V_e = V_{in}$.

It should be noted, that the equivalent resistance and generic model derived here, reflect the conduction losses only. The models do not include additional losses like: switching losses during turn 'on' and 'off', possible shoot through, and charge/discharge of the input capacitances of the switches [6]. In the soft switching case, switching losses can normally be ignored.

V. Extension to Higher Order Cases

The extension is demonstrated by considering a step down 3:1 converter that also includes two phases as shown in Fig. 6. In this case the average current through each capacitor is one third of the output current - I_o, (k = 1/3) as can be derived from Kirchhoff's Current Law (KCL) [5, 6].

It is assumed for simplicity that R_{ds_on} of all the switches is equal (denoted R_s), all the capacitances of switched capacitors are equal (C) and their ESRs are also equal (ESR). Inspecting phases A and B of the SCC operation, one can conclude that 1/3 of the output current is supplied by the source during phase A and 2/3 of the output current is delivered during phase B. This conclusion hinges on the fact that the average current of each capacitor must be the same in each of the two switching phases (A & B) to maintain charge balance.

The total equivalent capacitances for the Phase A and B are:

$$C_{T(A)} = \frac{C \cdot C_o}{2 \cdot C_o + C}; C_{T(B)} = \frac{2 \cdot C_o \cdot C}{C_o + 2 \cdot C} \quad (19)$$

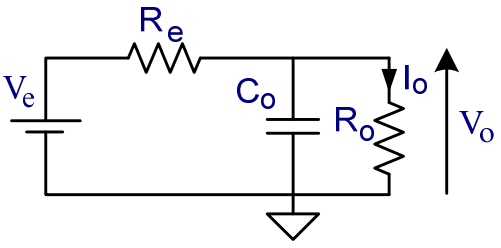


Fig. 5: SCC generic equivalent circuit.

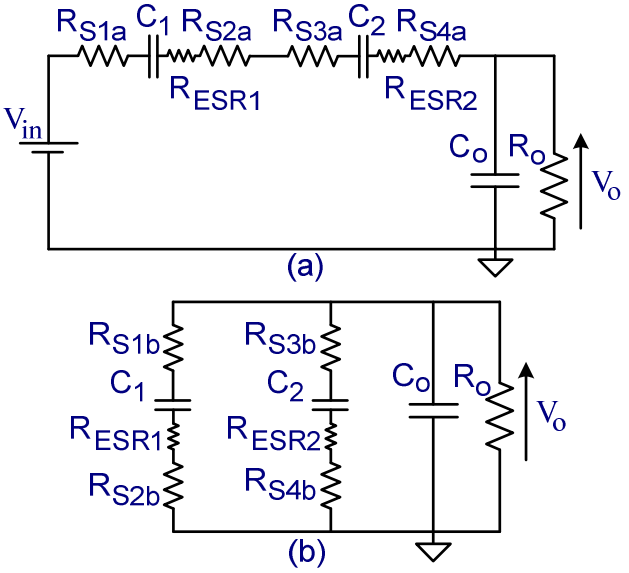


Fig. 6: Step down 3:1 SCC operation phases: (a) Phase "A", (b) Phase "B".

The total equivalent resistances are: $R_{T(A)} = 4R_S + 2ESR + ESR_O$ and $R_{T(B)} = R_S + ESR/2 + ESR_O$. Defining t_1 as the duration of the phase A, $\beta_{(A)}$ is expressed as:

$$\beta_{(A)} = \frac{t_1}{R_{T(A)}C_{T(A)}} = \frac{t_1}{(4R_S + 2ESR + ESR_O)\cdot\left(\frac{C\cdot C_O}{2\cdot C_O + C}\right)} \quad (20)$$

Applying the expression for energy dissipation in the resistor for RC circuit (9), we can express the energy loss in the resistors due to the phase A operation of the SCC:

$$E_{R(1)} = \frac{1}{9}\cdot\frac{I_O^2}{2f_S^2\cdot C\cdot C_O}\cdot(2\cdot C_O + C)\cdot\coth\left(\frac{\beta_{(B)}}{2}\right) \quad (21)$$

Defining t_2 as the duration of phase B, $\beta_{(B)}$ is expressed as:

$$\beta_{(B)} = \frac{t_2}{R_{T(B)}C_{T(B)}} = \frac{t_2}{(R_S + ESR/2 + ESR_O)\cdot\left(\frac{2\cdot C_O\cdot C}{C_O + 2\cdot C}\right)} \quad (22)$$

and the energy loss in the resistors during phase B of the SCC operation is:

$$E_{R(B)} = \frac{4}{9}\cdot\frac{I_O^2}{2f_S^2\cdot C\cdot C_O}\cdot\frac{C_O + 2\cdot C}{2}\cdot\coth\left(\frac{\beta_{(B)}}{2}\right) \quad (23)$$

Combining the two dissipation components and multiplying them by the switching frequency results in total average power dissipation, which can be directly used to express the equivalent resistance:

$$R_e = \frac{1}{18f_S C C_O}\left[(2C_O + C)\coth\left(\frac{\beta_{(A)}}{2}\right) + 2(C_O + 2C)\coth\left(\frac{\beta_{(B)}}{2}\right)\right] \quad (24)$$

For equal switching time periods ($t_1 = t_2 = T_s/2$) and identical flying capacitors $C_1 = C_2 = C$, $R_{ESR1}=R_{ESR2}=R_{ESR}$, identical switch resistances R_S, and infinite output capacitor C_O with no ESR, the β's of each of the phases are equal despite the fact that the capacitors are connected in series and then in parallel. Under these assumptions the equivalent resistance R_e is reduced to:

$$R_e = \frac{2}{9}\left\{\frac{1}{f_S C}\cdot\frac{(1+e^{-\beta})}{(1-e^{-\beta})}\right\} \quad (25)$$

where $\beta = \frac{T_S}{2}\cdot\frac{1}{(2\cdot R_S + R_{ESR})\cdot C}$

Being a 3:1 step-down converter, the equivalent source V_e is in this case: $V_e = V_{in} / 3$.

The derivation of the equivalent resistance model for the soft switching case is demonstrated on a step-up 1:3 converter that includes two phases as shown in Fig. 7. As in the previous analysis, it is assumed again that C_O is infinitely large and that its ESR can be neglected, $C_{1a}=C_{1b}=C_2=C$ and $ESR_{1a}=ESR_{1b}=ESR_2=ESR$. In the first phase of the analysis the diode losses (Dxx in Fig. 7) are neglected. The resistor R_1 represents the switch resistance and the parasitic resistance of the inductor. The analysis of phases "A" (Fig. 7a) and "B" (Fig. 7b) of the SCC operation is carried out on stand-alone, four separate sub-circuits 1-4 (Fig. 8). It should be noted, though, that this separation is only an approximation since it neglects the fact that all the currents of the sub-circuits of a given phase pass through R_1 simultaneously.

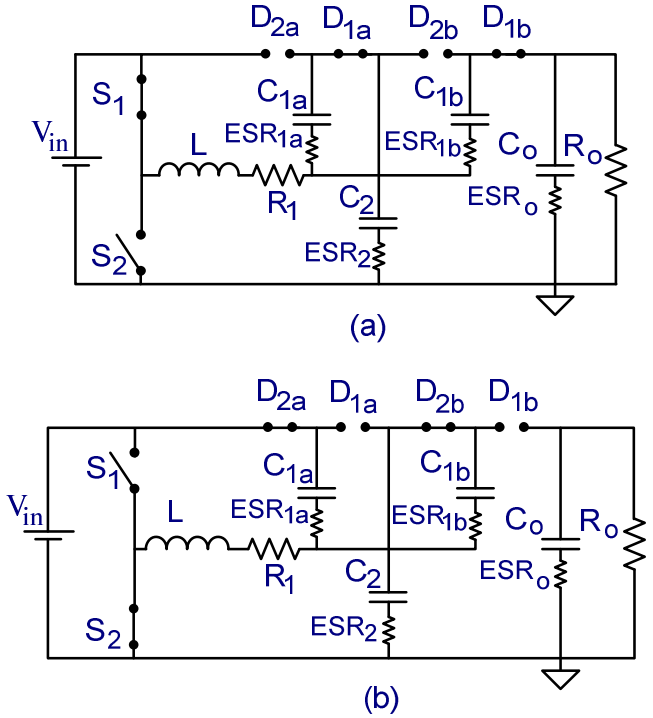


Fig. 7: Step up 1:3 SCC operation phases: (a) Phase "A", (b) Phase "B".

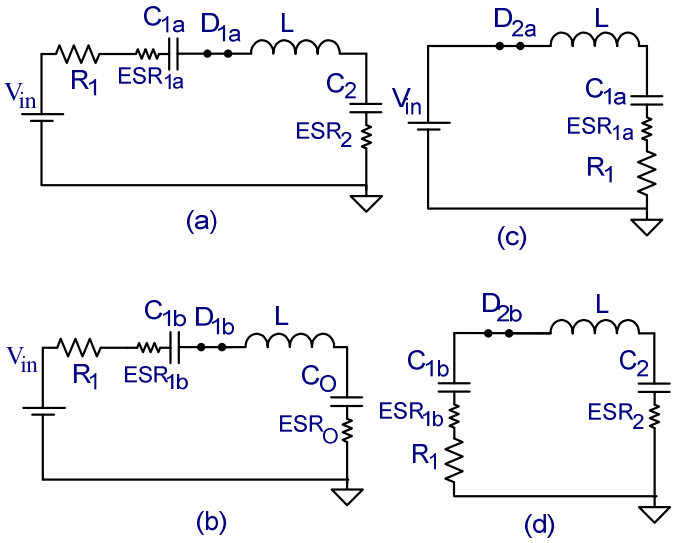


Fig. 8: Sub-circuits of phases A (a, b) and B (c, d).

The decoupling assumption is acceptable if R_1 is smaller than the other resistance in the circuit. As is evident from the simulation and experimental results given below, this assumption is acceptable in practical circuits that will normally be designed with a small R_1 (low $R_{ds(on)}$ and high Q inductor). If the decoupling is unwarranted, the analysis becomes complex and as such is beyond the scope of this paper.

Examination of Fig. 8 reveals that the same charge is transferred by each of the capacitors during each switching phase (A&B) and that the average current through the capacitors is equal to the output current I_o (i.e. k=1). This could be inferred as follows: The charge to the output is supplied by C_{1b} (Fig. 8b) while this charge is supplied to C_{1b} by C_2, (Fig. 8d). In the same manner, C_2 is charged by C_{1a} (Fig. 8a). And finally, this charge is supplied to C_{1a} by the source V_{in} (Fig. 8c). Considering the fact that all charges are identical and equal to the output current (for any given switching cycle in steady state), we find that k=1. As a side note one can observe that the average current coming off the input V_{in} is three times the output current as would be expected from power balance considerations, considering the fact that this is a step up (1:3) converter. This current ratio occurs because V_{in} supplies the said charge three times: in sub circuits shown in Figs. 8a, 8b and 8c.

The equivalent capacitor in each subcircuit is calculated to be:

$$C_{T(1,4)}=\frac{C}{2};\quad C_{T(2)}=\frac{C_o\cdot C}{C_o+C};\quad C_{T(3)}=C; \tag{26}$$

The total equivalent resistances are: $R_{T(1,4)}=R_1 + 2ESR$; $R_{T(2)}=R_1 + ESR + ESR_O$; $R_{T(3)}=R_1 + ESR$;

Using the expression for energy dissipation in the resistor for the soft switching case (14), the energy loss in the resistors of the sub-circuits can be expressed as:

$$E_{R(1,4)}=\frac{I_o^2}{2f_s^2C/2}\cdot\tanh\left(\frac{\pi\zeta_{(1,4)}}{2}\right)$$
$$E_{R(2)}=\frac{I_o^2}{2f_s^2\left(\frac{C_o\cdot C}{C_o+C}\right)}\cdot\tanh\left(\frac{\pi\zeta_{(2)}}{2}\right) \tag{27}$$
$$E_{R(3)}=\frac{I_o^2}{2f_s^2C}\cdot\tanh\left(\frac{\pi\zeta_{(3)}}{2}\right)$$

The average power is obtained by combining all the energy dissipation components and multiplying them by the switching frequency which leads to the expression of the equivalent resistance:

$$R_e=\frac{1}{2f_SC}\left[\begin{array}{l}2\tanh\left(\frac{\pi\zeta_{(1)}}{2}\right)+\frac{C_o+C}{C_o}\tanh\left(\frac{\pi\zeta_{(2)}}{2}\right)\\ +\tanh\left(\frac{\pi\zeta_{(3)}}{2}\right)+2\tanh\left(\frac{\pi\zeta_{(4)}}{2}\right)\end{array}\right] \tag{28}$$

where $\zeta_{(1)}$, $\zeta_{(2)}$, $\zeta_{(3)}$ and $\zeta_{(4)}$ are:

$$\zeta_{(1,4)}=\frac{R_1+2ESR}{2L\sqrt{\frac{1}{L(C/2)}-\frac{R_1+2ESR}{2L}}}$$
$$\zeta_{(2)}=\frac{R_1+ESR+ESR_o}{2L\sqrt{\frac{1}{L\cdot\frac{C_o\cdot C}{C_o+C}}-\frac{R_1+ESR+ESR_o}{2L}}} \tag{29}$$
$$\zeta_{(3)}=\frac{R_1+ESR}{2L\sqrt{\frac{1}{LC}-\frac{R_1+ESR}{2L}}}$$

Diode conduction losses can be modeled by adding to the generic equivalent circuit a voltage source V_D equal to the sum of the forward voltage drops of all the diodes in the circuit and taking into account the average current through each diode. Since in this SCC all the transferred charges are equal, the average currents are equal and consequently $V_D=4V_1$ where V_1 is the average voltage drop across a single diode. Being a 1:3 step up converter, the equivalent source V_e in this case is: $V_e = 3V_{in}$ (Fig. 9).

Another example of deriving the equivalent resistance model is demonstrated by a step down 1:3/8 Extended Binary (EXB) based SCC.

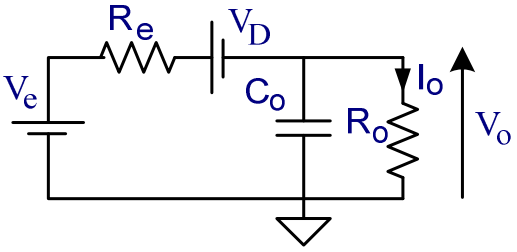


Fig. 9: SCC generic equivalent circuit including diode losses.

This class of converters is based on a novel approach, which makes possible the realization of multi target SCC with binary resolution. In depth description of the approach is presented in [9]. For the 3/8 case there are 4 phases of SCC operation, (Fig. 10).

Following the same concept as before, we apply the following assumptions: that $C_1 = C_2 = C_3 = C$ and that all switch resistances are equal (R). Denoting the average current for each phase Figs. 10a -10d as I_1-I_4 respectively and taking into account that the average current through each capacitor must be zero (in steady state) one can write the following set of equations for each capacitor.

$$\begin{cases} +I_1 - I_2 + I_3 + 0 = 0 \;; C_1 \\ +I_1 + I_2 + 0 - I_4 = 0 \;; C_2 \\ -I_1 - I_2 + I_3 - I_4 = 0 \;; C_3 \\ I_1 + I_2 + I_3 + I_4 = I_o \end{cases} \tag{30}$$

The last equation of (30) states that the sum of the currents of each subcircuit of Fig. 10 equals to the output current (KCL).

$$\sum_{j=1}^{4} \left| I_j \right| = I_O \tag{31}$$

The solution for the system of linear equations (30) is:

$$I_1 = 1/8 \cdot I_o;\; I_2 = 3/8 \cdot I_o;\; I_3 = 1/2 \cdot I_o;\; I_4 = 1/4 \cdot I_o \tag{32}$$

The solution thus defines the k for each phase. Next, one can determine for each SCC phase of operation the total capacitance – C_j, the total resistance – R_j and the parameter – $\beta_j = t_j/(R_j C_j)$. The number of switches used in each SCC operation phase in the experimental setup (Fig. 10) does not change and equals to 4, so the total resistance R is 4 times the switch resistance plus the ESR of the capacitors. Applying the fact that in the EXB based SCC the flying capacitors C_j are always connected serially, one can find the total capacitance – C_j for each SCC operational mode (Fig. 10), [9]. The normalized data required for the equivalent resistor derivation is summarized in Table I.

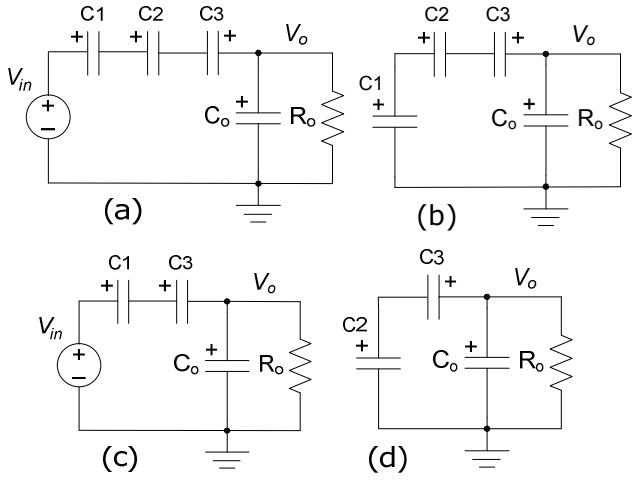


Fig. 10: Capacitors connections that follow the EXB codes of 3/8 and form the 4 phases (a-d) of operation of the EXB based SCC.

TABLE I
NORMALIZED DATA REQUIRED FOR THE EQUIVALENT CIRCUIT MODELING FOR THE SUB-CIRCUITS OF FIG. 10

j	I_j/I_o	C_j/C	β_j/β
1	1/8	1/3	3
2	3/8	1/3	3
3	1/2	1/2	2
4	1/4	1/2	2

Based on Table I, R_e is calculated to be:

$$R_e = \frac{5}{64} \frac{1}{f_S C} \left[3\coth\left(\frac{3\beta}{2}\right) + 4\coth(\beta) \right] \tag{33}$$

VI. SIMULATION AND EXPERIMENTAL VERIFICATIONS

The analytical expressions developed in this study were verified against simulation and experimental results. An example of the excellent agreement between simulation results and the proposed model is given in Fig. 11, which shows the results for a duty cycle of 0.9. Fig. 12a depicts simulation and model derived results of a soft switched 1:1 unity converter. The experimental waveforms for this soft switching case are presented in Fig. 12b. The simulated and model derived output voltage was 21.96V while the measured output voltage in this case was 22V. Fig. 13a presents simulation and model derived results for a step up 1:3 hard switched SCC, experimental results for this converter are presented in Fig. 13b and found to be in good agreement to those obtained by the model and the simulation. Measured output voltage was 62V while the simulation and model derived value was 61.56V. The input voltage in all the experiments was 24V.

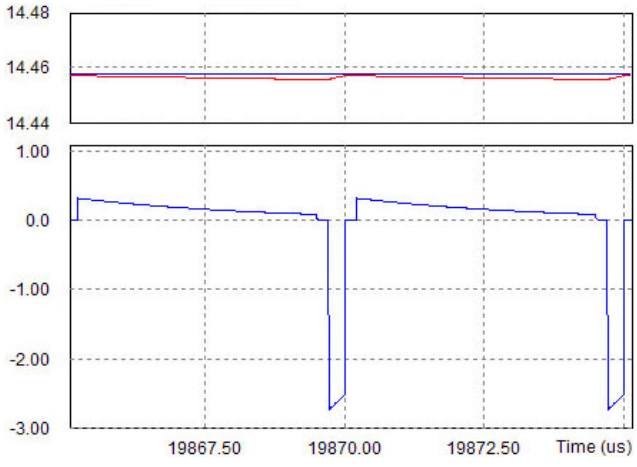
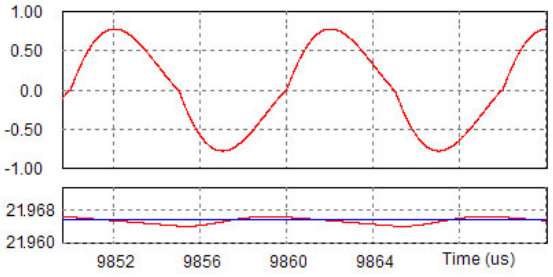
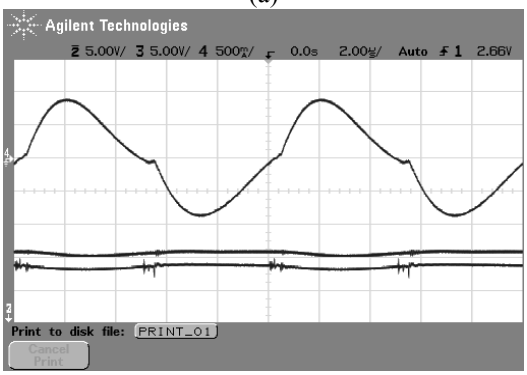


Fig. 11: Simulation and model results for a hard switched 1:1 converter. Upper trace - output voltage (straight line: model). Lower trace - capacitor current. V_{in} = 24V, Duty cycle = 0.9.

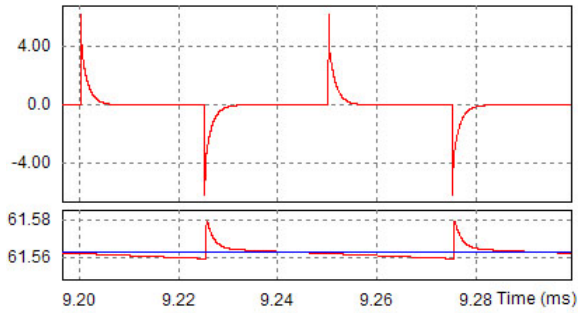


(a)

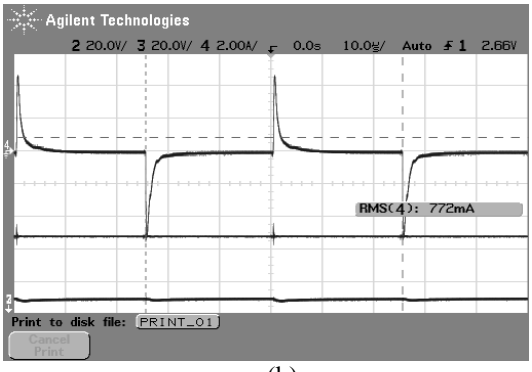


(b)

Fig. 12: Soft switched 1:1 unity converter: (a) Simulation and model: upper plot - capacitor current. Lower plots - output voltage (straight line: model). (b) Experimental: upper line - capacitor current 500mA/div, middle line - output voltage ripple 5V/div, bottom line - capacitor voltage ripple 5V/div. Horizontal scale: 2µs/div. V_{in} = 24V.



(a)



(b)

Fig. 13: Hard switched 1:3 step-up converter:
(a) Simulation and model: upper trace - net capacitors current. Lower plots - output voltage (straight line: model). (b) Experimental: upper line - capacitors current 2A/div, middle line - output voltage ripple 20V/div, bottom line - capacitor voltage ripple, 2V/div. V_{in} = 24V.

The theoretical prediction of (33) was compared to the experimental results by carrying out measurements on the EXB based SCC described in [9]. The experimental setup was built around CMOS bidirectional switches MAX4678 with a nominal 'on' resistance of 1.2Ω, C_1= C_2=C_3= 4.7µF, C_o= 470µF and f_s=100kHz. The control was carried out by a microcontroller PIC18F452. The calculated value of R_{eq} according to (33) was 9.052Ω while the measured value was R_{eq} = 7.35 Ω.

VII. DISCUSSION AND CONCLUSIONS

The modeling approach developed in this study leads to unified model that describes the losses for each flying capacitor in the hard and soft switched cases. For the symmetrical case ($t_1 = t_2$):

$$R_e\Big|_{Hard} = k^2 \cdot \frac{1}{f_S C} \cdot \coth\left(\frac{\theta}{2}\right); \theta = \frac{1}{2f_S \cdot RC} \quad (34)$$

$$R_e\Big|_{Soft} = k^2 \cdot \frac{1}{f_S C} \cdot \tanh\left(\frac{\theta}{2}\right); \theta = \frac{\pi \cdot \zeta_d}{2} \quad (35)$$

Analysis of the loss expressions for the hard switched case reveal that the losses are independent of the switches and ESR resistances when the charge/discharge process ends within each switching period. This is because the coth term in (34) converges to "1" when θ/fs >> 1, Fig. 14a. The losses in this case are equal to $1/2f_sC$. This was also pointed out in [5], and the process was referred to as SSL. The losses are reduced as the switching period becomes shorter and approaches the asymptotic value of 4R when the switching instance is much shorter than the charge/discharge time constants (Fig. 14b). This process was referred to as FSL in [5].

$$R_e\Big|_{Hard} = \left\{\frac{2R}{2f_S CR} \cdot \frac{(1+e^{-\theta})}{(1-e^{-\theta})}\right\} = 2R\theta\frac{(1+e^{-\theta})}{(1-e^{-\theta})}; R_e\Big|_{\theta\to 0} = 4R \quad (36)$$

The lower loss at short switching times is a direct outcome of the fact that in the latter case, the charge/discharge RMS current is smaller than in the exponential case (Fig.15), which prevails in the longer switching time. When the switching time is much shorter than the time constant of the circuit, the current is practically constant during the switching time and hence the RMS value is the lowest possible. For the non symmetrical case, the RMS currents of each phase are not equal and the total equivalent resistance will reach higher values as depicted in Fig. 16. The losses of the soft switched SCC for a high Q case and when the resonant frequency matches the damped oscillation frequency is 5R, higher than the limiting value of the hard switched capacitor (4R). This is because the RMS current of the soft switched SCC is higher than that of the limiting value of the hard switching case (Fig.16). Similar results were derived in [4]. The major difference between the present analysis and the one presented in [4] is the fact that the expression for soft switched SCC equivalent resistance derived in this work is more general, while in [4] it is based on the first harmonic approximation.

This approximation may introduce errors when the equivalent RLC circuits have relatively low quality factor. Furthermore, the model presented in this work is also valid for non-symmetrical operational modes, i.e. when non equal time periods are used in the different SCC phases of operation. Furthermore, since the losses are expressed in this work as a function of the capacitors' current (which is proportional to the output current) the results can be applied to analyze complex multi-phase SCC systems.

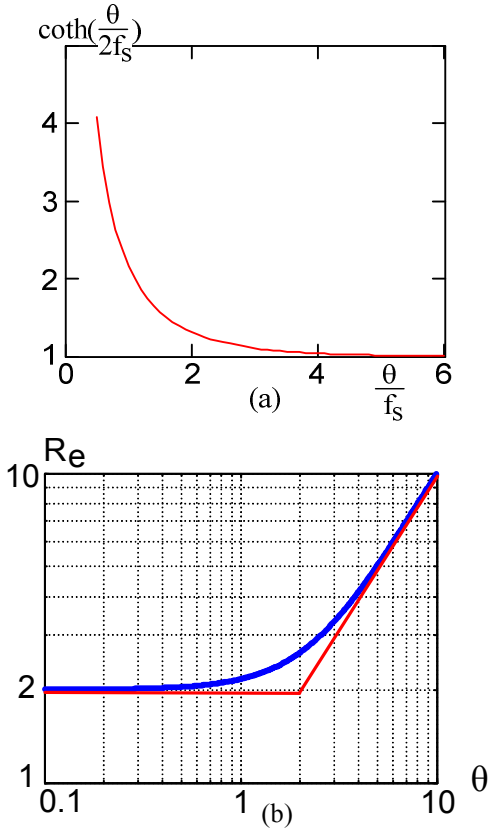


Fig. 14: Hard switching SCC limits: (a) Hyperbolic cotangent as a function of normalized θ (to the switching frequency); (b) Smooth curve - Equivalent resistance as a function of θ, straight lines - asymptotic resistance limits.

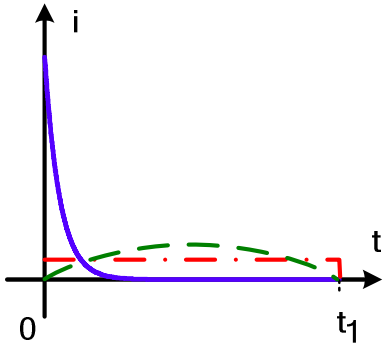


Fig. 15: Current waveforms for different SCC operations: exponential curve - hard switching SCC SSL case; Square – hard switching SCC FSL case; Curved line – soft switching SCC case.

In applications that require a regulated output voltage, the SCC needs to include some means to increase R_e. In most cases it is accomplished by adding resistance to one or more loops. Obviously, the model developed here can be applied to these cases by including in R_e the resistance of the controlling element, such as a MOSFET. Other control techniques, such as variable frequency control and frequency dithering control, could also be evaluated by the proposed approach by extracting the relevant parameters for each operational mode.

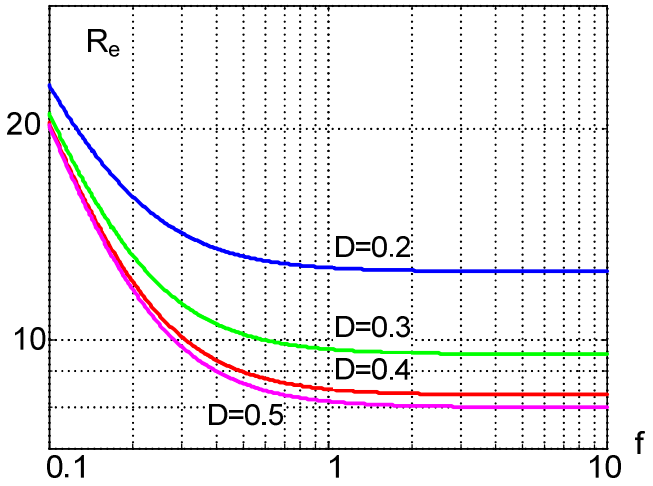


Fig. 16: Dependence of the equivalent resistance on the duty cycle (D) as a function of normalized frequency in hard switched SCC.

REFERENCES

[1] C. K. Tse, S. C. Wong and M. H. L. Chow, "On Lossless Switched-Capacitor Power Converters", *IEEE Transactions on Power Electronics*, Vol. 10, No.3 , 285-261, 1995.

[2] A. Ioinovici, "Switched-capacitor power electronics circuits," *IEEE Circuits and Systems Magazine*, Vol. 1, No. 3, 37-42, 2001.

[3] Y. P. B. Yeung, K. W. E. Cheng, S. L. Ho, K. K. and Law, D. Sutanto, "Unified analysis of switched-capacitor resonant converters ", *IEEE Transactions on Industrial Electronics*, Vol. 51, No. 4, 864 – 873, 2004.

[4] J. W. Kimball, P. T. Krein, "Analysis and Design of Switched Capacitor Converters", *IEEE Applied Power Electronics Conference, APEC- 2005*, vol. 3, 1473 -1477.

[5] M. D. Seeman, S. R. Sanders, "Analysis and Optimization of Switched Capacitor DC-DC Converters", *IEEE Transactions on Power Electronics,* Vol. 23, No. 2, pp. 841-851, March 2008.

[6] B. Arntzen, D. Maksimovic, "Switched-Capacitor DC/DC Converters with Resonant Gate Drive" *IEEE Transactions on Power Electronics,* Vol. 13, No. 5, pp. 892-902, September 1998.

[7] M. S. Makowski, D. Maksimovic, "Performance Limits of Switched-Capacitor DC-DC Converters", *IEEE Power Electronics Specialists Conference, PESC-1995*, vol. 2, 1215 -1221.

[8] I. Oota, N. Hara, F. Ueno, "A General Method for Deriving Output Resistances of Serial Fixed Type Switched-Capacitor Power supplies", *IEEE International Symposium on Circuits and Systems, ISCAS-2000,* vol. 3, 503-506.

[9] S. Ben-Yaakov, A. Kushnerov, " Algebraic Foundation of Self Adjusting Switched Capacitors Converters", *to be published in Proceedings IEEE Energy Conversion and Exposition (ECCE),* San Jose, California, USA, September 20-24, 2009.