A High Gain DC-DC Converter for Energy Harvesting of Thermal Waste by Thermoelectric Generators

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Abstract – **A tapped-inductor boost converter for an input voltage range of 0.3-0.6 V with the output connected to a fixed voltage of 24V for battery charging, was designed, analyzed and tested experimentally. The converter is intended to be used as a harvester for low voltage renewable energy sources such as thermoelectric generators and bio-reactors. The proposed converter is capable of achieving a high boost ratio (40-80) with a reasonable duty-cycle (0.3-0.7). The converter was optimized by selecting low parasitic resistance components and by applying a PCB-based flat magnetic core to reduce the leakage inductance. The operation of the proposed converter was analyzed for continuous and discontinuous inductor current modes and power loss and efficiency expressions were derived. Good agreement was found between circuit simulations, theoretical analysis and experimental results. The experimental unit reached an efficiency of about 86% (gate drive losses included) at an input voltage of 0.5V and output power level of about 1.2W.**

Index Terms- Energy harvesting, high-gain DC-DC converter, boost converter, tapped-inductor, leakage inductance, snubber, thermoelectric generator, TEG.

I. Introduction

The issues of global warming and of the anticipated future shortage of fossil fuels motivate the search for alternative energy sources. Aside from the major energy alternatives, such as solar and wind energy, there is growing interest in the harvesting of small, yet abundant, unexploited energy sources such as wasted thermal energy, kinetic energy and electromagnetic energy. This study focuses on the harvesting of thermal energy that is now dissipated in cars, factories, PV panels and many other places. Thermal energy can be converted into usable electrical energy by thermoelectric devices, which generate a DC voltage as a function of the temperature gradient between the cold and the hot side of the plates. A Thermoelectric Generator (TEG) module is characterized by its high reliability, long life and small size features. Typically, the generated voltage of a single TEG will be lower than 1Volt, while the output power will be in the order of one to several Watts. Hence, there is a need for power conversion between the output of the TEG and the load, which could be a car battery or other loads that normally require higher voltages.

Previous studies have presented various solutions to this basic conversion problem, but none of them is suitable for high efficiency power conversion from sources having a sub-volt output voltage and above 1Watt power level (equivalent to output currents of a few Amperes).

It is important to mention that in a case of very low input voltage together with high input current, not only the circuit design plays an important role, but also choosing the components has a major effect on the circuit's functioning and efficiency. Therefore, different magnetic body forms should be examined.

The objective of this study was to examine the expected losses in high-gain DC-DC converters and to apply the results of the theoretical analysis to the design of a high voltage-gain converter that is suitable for the harvesting of wasted thermal energy by a TEG. The converter was designed to operate at a power level of about 1Watt with an input voltage of 0.3-0.6V, and with the output connected to provide a fixed voltage of 24V for battery charging.

II. Proposed Converter Topology And Operation Analysis

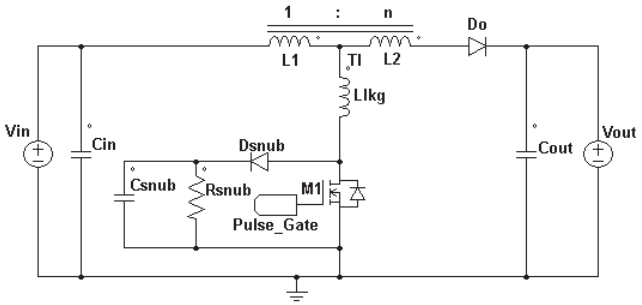


Fig.1. Proposed high tapped-inductor boost ratio DC-DC converter

The basic structure of the proposed converter is shown in Fig.1. C_{in} is the input capacitor which is applied in order to reduce the input ripple; TI is the tapped-inductor with turn ratio 1:n, which is characterized by primary inductance, L_1, secondary inductance, L_2, and the leakage inductance, L_{lkg}, seen at the primary side; M_1 is the MOSFET switch; D_o is the output diode; C_{out} is the output capacitor, which minimizes the output ripple; D_{snub}, R_{snub} and C_{snub} are the diode, resistor and capacitor of the snubber unit, respectively. As discussed below, the snubber is not required in the present application since the voltage overshoot at the MOSFET's drain is minimal thanks to the very low leakage inductance achieved in the experimental unit.

A. Converter Operation

Using a tapped-inductor instead of an ordinary inductor is necessary in order to get a high boost ratio with a reasonable duty-cycle.

The proposed converter operation for one switching cycle comprises two stages. In the first stage, the MOSFET switch, M_1, is on, the primary side and leakage inductance of the tapped-inductor are charged by the input voltage and the output capacitor is charged by the output current. In the second stage, the MOSFET switch is turned off, and the output diode, D_o , is forward-biased. While the energy stored in the magnetizing inductor of the tapped-inductor is being transferred to the load, the energy stored in the leakage inductance is being wasted dissipated. During this time period, the snubber capacitor, C_{snub}, is charged, which clamps the MOSFET's voltage to a safe value (if needed).

B. Theoretical Model

The proposed converter transfer function can be obtained by the flux balance criteria for steady state operation. For continuous inductor current mode, CCM, the transfer function depends only on the duty-cycle, D, and the turns-ratio, n:

$$\left.\frac{V_o}{V_{in}}\right|_{CCM} = \frac{1+nD}{1-D} \quad (1)$$

In contrast, for discontinuous inductor current mode, DCM, the voltage transfer ratio depends not only on the duty-cycle, D, but also on the switching frequency, f_s:

$$\left.\frac{V_o}{V_{in}}\right|_{DCM} = \frac{D(1+n)+D_{off}}{D_{off}} \quad (2)$$

$\left.D_{off}\right|_{DCM}$ is defined as the time ratio that the output diode conducts:

$$\left.D_{off}\right|_{DCM} = \sqrt{\frac{2I_o f_s L_2}{V_o - V_{in}}} \quad (3)$$

Hence, in the DCM mode and for a given voltage transfer ratio, the duty-cycle changes as a function of the switching frequency.

C. Proposed Converter Efficiency: Power Loss Analysis

The main issue in low-input-voltage boost design is that the circuit impedances have to be very low in order to achieve a high level of efficiency.

The loss analysis carried out in this study includes conduction losses (power MOSFET, diode and wires), magnetic losses and gate drive losses. The power losses and efficiency of the proposed topology were calculated both for the CCM and the DCM modes over the frequency range of 10kHz to 100kHz. The loss calculations take into account the forward voltage of the output diode, magnetic core losses, leakage losses, MOSFET gate losses, parasitic resistances, losses of the MOSFET and input and output capacitors (ESR). Equations (3) and (5)-(12) express the differences between the continuous and the discontinuous inductor current mode, CCM and DCM.

For both modes the voltage stress of the MOSFET switch can be calculated by:

$$V_{SM} = \frac{V_{out} - nV_{in}}{n+1} \quad (4)$$

Where V_{SM} is the voltage stress of MOSFET switch.

For CCM:

$$I_{1pk} = \frac{V_{in}}{L_1}\frac{D}{f_s} + I_{in} \quad (5)$$

$$I_{Srms} = \sqrt{D\left[\left(\frac{I_{in}}{D}\right)^2 + \frac{\left(\frac{V_{in}D}{L_1 f_s}\right)^2}{12}\right]} \quad (6)$$

$$I_{2rms} = \sqrt{(1-D)\left[\left(\frac{I_o}{1-D}\right)^2 + \frac{\left(\frac{V_{in}D}{L_1 f_s}\frac{1}{n+1}\right)^2}{12}\right]} \quad (7)$$

$$D_{off} = 1 - D \quad (8)$$

For DCM:

$$I_{1pk} = \frac{2I_{in}}{D} \quad (9)$$

$$I_{Srms} = \frac{2I_{in}}{D}\sqrt{D\,\frac{3D^2+1}{12}} \quad (10)$$

$$I_{2rms} = \frac{2I_O}{D_{off}}\sqrt{D_{off}\,\frac{3(D_{off})^2+1}{12}} \quad (11)$$

where I_{Srms} represents the rms current of the MOSFET switch, I_{2rms} represents the rms current of the secondary winding, I_o is the output average current and I_1 is the current of the primary winding.

Also, for both modes the total rms current of the primary winding, $I_{1rms,tot}$, which is also the converter's input rms current, is:

$$I_{1rms,tot} = I_{in,rms} = \sqrt{(I_{Srms})^2 + (I_{2rms})^2} \quad (12)$$

The following relations (13)-(25) are the results of the power losses and efficiency analyses.

MOSFET's switch loss is composed of conduction and switching losses. The total loss can be expressed by:

$$P_{FET} = r_{DS} I_{S,rms}^2 + \frac{1}{2} f_s C_o (V_{SM})^2 \quad (13)$$

where r_{DS} is the MOSFET drain-source on resistance and C_o is the MOSFET output capacitance.

The overall output diode conduction loss consists of the forward voltage drop loss and the forward resistance loss of the diode. It can be calculated by using the following formula:

$$P_D = V_{FD} I_o + r_{F_D} I_{2,rms}^2 \quad (14)$$

where r_{F_D} is the diode forward resistance and V_{FD} is the forward voltage drop.

Input capacitor (ESR) power loss can be calculated by:

$$P_{C_{in}} = \left[\left(\frac{I_{1pk} - I_{in}}{\sqrt{3}}\right)^2 D + \left(\frac{\frac{I_{1pk}}{n+1} - I_{in}}{\sqrt{3}}\right)^2 D_{off}\right] r_{ESR_{C_{in}}} \quad (15)$$

where $r_{ESR_{C_{in}}}$ is the ESR of the input capacitor, C_{in}.

Output capacitor (ESR) power loss can be calculated by:

$$P_{C_{out}} = \left[\left(\frac{\frac{V_{in}D}{L_1 f_s}\left(\frac{1}{1+n}\right) - I_o}{\sqrt{3}}\right)^2 \frac{V_{in}DL_2}{L_1 V_O (1+n)} + (I_o)^2\left(1 - \frac{V_{in}DL_2}{L_1 V_O (1+n)}\right)\right] r_{ESR_{C_{out}}} \quad (16)$$

where $r_{ESR_{C_{out}}}$ is the ESR of the output capacitor, C_{out}.

The power losses of the magnetic component consist of the copper loss (P_{rL}) and core loss (P_v):

$$P_{rL} = r_{L1}\left(I_{1rms,tot}\right)^2 + r_{L2}(I_{2rms})^2 \quad (17)$$

where r_{L1} and r_{L2} represent the parasitic resistances of the primary and secondary windings of the tapped-inductor, respectively.

Core loss is calculated for a 3F3 ferrite material:

$$P_v = 1.5 \cdot 10^{-6} f^{1.3} (\Delta B)^{2.5} 10^{-3} A_e l_e \quad (18)$$

where ΔB is the change of the magnetic flux density, A_e is the effective cross section of the core and l_e is the core effective magnetic path length.

The power loss due to the leakage inductance is theoretically given by:

$$P_{lkg} = \frac{\left(I_{1pk}\right)^2 L_{lkg} f_s}{2} \quad (19)$$

where L_{lkg} is the leakage inductance reflected to the tap terminal.

However, when an RC snubber is used (Fig. 1), the total power is transferred to the snubber and hence constitutes a power loss that is given by:

$$P_{lkg} = \frac{\left(I_{1pk}\right)^2 L_{lkg} f_s \left(V_{D,snub} + V_{Rsnub}\right)}{2\left(V_{D,snub} + V_{Rsnub} - V_{SM}\right)} \quad (20)$$

This power loss should theoretically be equal to the power dissipated in R_{snub} and D_{snub}:

$$P_{lkg} = \left(V_{Rsnub} + V_{D,snub}\right)\frac{V_{Rsnub}}{R_{snub}} \quad (21)$$

where R_{snub} is the resistance of the snubber unit, V_{Rsnub} is the voltage drop on R_{snub}, $V_{D,snub}$ is the voltage drop on D_{snub} and $I_{D,snub}$ is the D_{snub} average current.

The overall power loss of the above-discussed converter is:

$$P_{loss,tot} = P_{FET} + P_D + P_{rC_{in}} + P_{rC_{out}} + P_{rL_1} + P_{rL_2} + P_v + P_{lkg} \quad (22)$$

The efficiency of this converter can be expressed as:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss,tot}} = \frac{V_o I_o}{V_o I_o + P_{loss,tot}} \quad (23)$$

Finally, the efficiency affected by the gate drive loss is given by:

$$\eta_{tot} = \frac{V_o I_o}{V_{in} I_{in} + P_{Gate}} \quad (24)$$

when:

$$P_{Gate} = Q_G V_{gs} f_s \quad (25)$$

where Q_G is the MOSFET's gate charge and V_{gs} is the MOSFET's gate-source voltage.

III. Flat Magnetics Design

In order to reduce leakage as much as possible, the inductor was designed using flat magnetics, with the primary and secondary windings printed on a PCB. This enables the primary and secondary windings to be printed close to each other using separate thin layers.

PCB copper layers are thin, meaning that in order reduce the resistance of the primary, wide traces need to be used. An E38/8/25 E core and a corresponding PLT 38/25/4 plate core were chosen, having gaps for traces of width of up to $w_p \approx 9mm$. With copper resistance being $\rho \approx 1.68 \cdot 10^{-5}\Omega\cdot$mm, 1oz of copper thickness $h \approx 33 \cdot 10^{-3}$mm and trace length for the selected core $l_p \approx 110$mm, the primary winding's resistance will be $R_p \approx 6.2$mΩ/oz. To reduce the copper resistance to well below 1mΩ, both external layers – top and bottom - were chosen to be used in parallel for the primary winding using 4oz of copper, leading to an estimated resistance of $R_p \approx 0.78$mΩ. In addition, no solder mask was used in the PCB manufacturing process, resulting in an additional tin coating on the primary winding layers and hence further reducing R_P. To eliminate further resistances on the primary side, all the components handling the primary current were mounted on the PCB and fitted closely to the primary winding. The 21 secondary turns were implemented on two internal layers serially connected with 10 windings on one and 11 on the other, resulting in a trace length of $l_s \approx 2270$mm. Considering a PCB of 4oz copper, and the requirements of a minimal etch gap tolerance of 10 mil, the secondary trace width was $w_s \approx 0.381$mm, resulting in estimated secondary resistance of $R_s \approx 0.75\Omega$.

The desired inductance, L, can be achieved using a core with an air gap. The needed air gap length, l_g, can be estimated using (26):

$$l_g \approx \frac{n^2 A_e \mu_0}{L} \quad , \quad l_g > \frac{l_e}{\mu_m} \quad (26)$$

where n is the number of windings, A_e the core's cross-section, μ_0 is the permeability of air and l_e is the core's magnetic length. Equation (26) can be used when considering a core with a basic permeability, μ_m , high enough to satisfy the approximation's condition. The above-mentioned core's geometry has parameters of $A_e = 194\text{mm}^2$ and $l_e = 52.4$mm. For the primary side, considering that $n = 1$ and the desired inductance is $L = 2.2\mu$H, (26) yields $l_g \approx 0.116$mm for core material grades with $\mu_m > 500$.

A magnetic core of grade 3F3 was chosen, with a μ_m of 1720 with magnetic losses of about 1W/Tesla at switching frequencies of about 25kHz for the above-described geometry.

Fig. 2 and Fig.3 show the PCB and its internal windings, as well as the magnetic core. Experimental measurements indicate the following parameters (the resistances include the complete trace and magnetic losses):
$L_p = 2.1\mu H, L_s = 816\mu H, R_p = 1.7m\Omega, R_s = 650m\Omega$, $L_{lkg} = 20\mu H$, measured at the secondary side.

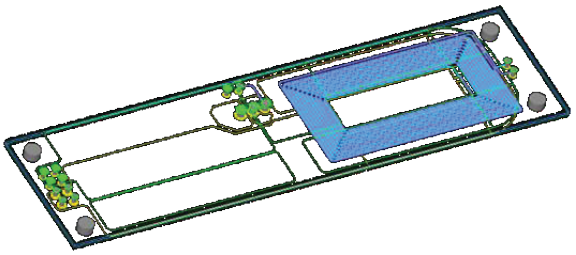


Fig.2. Design of the Flat Magnetics, PCB 2^{nd} layer

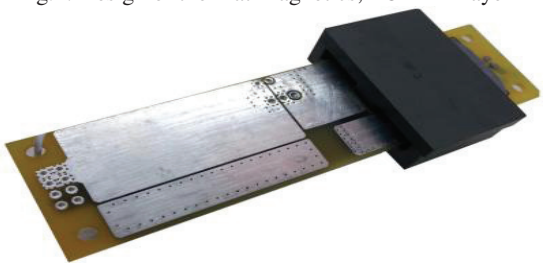


Fig.3. The assembled Flat Magnetics PCB

IV. Experimental Verifications

The design of the tapped-inductor applies a PCB-based flat magnetic element, which contributes to high efficiency due to the low resistance of the PCB windings, low magnetic losses and low leakage.

The proposed converter was tested using PSIM simulations, and validated experimentally.

Table 1 and Table 2 list the design parameters and components selected for the proposed model.

Table 1
Design Parameters

DC output voltage	24V
Input voltage	0.5V
Output power range	$1-1.5$W
Switching frequency range	$10-60$kHz
Duty-cycle range	$0.3-0.7$
Turns ratio, n, of the tapped-inductor	1:21

Table 2
Component Selection

Thermo Electric Cooler	TB-32-2.8-1.5, KRYOTHERM
C_{in}	3×1.5mF/2.5V RR50E152MDN1, NICHICON
Tapped-inductor	E38/8/25, PLT38/25/4, 3F3
M_1	IRF1324PBF
D_1	1N5822
C_{out}	100uF/250V Electrolytic cap

The specifications used in the power loss analysis and the efficiency calculation are given in Table 3.

Table 3
Specifications of the Proposed Converter

Input voltage (V_{in})	0.5V
DC Output voltage (V_{out})	24.34V
Input power (P_{in})	1.1675W
Output power (P_{out})	1.073W
Switching frequency (f_s)	55kHz
Duty − cycle (D)	0.691

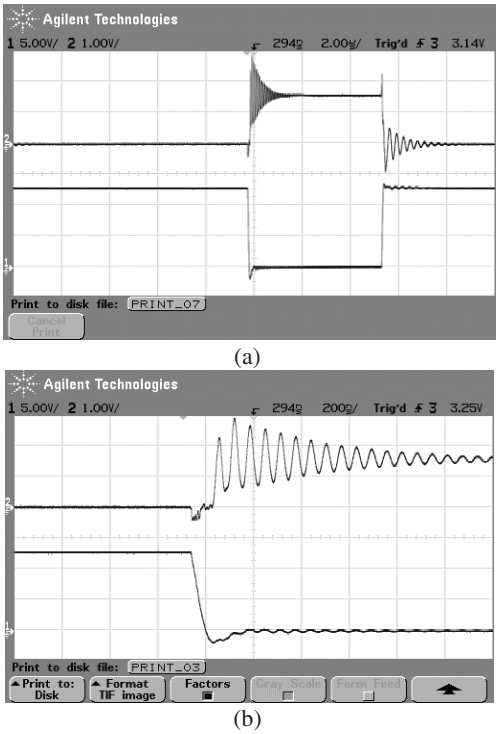
The power loss results (Table 4) were obtained by analyzing the proposed converter with the following parameters: $r_{DS}=1.2$mΩ, $C_o\approx 10{,}000$pF, $r_{F_D}=18.27$mΩ, $r_{ESR_{C_{in}}}=1.666$mΩ, $r_{ESR_{C_{out}}}=245$mΩ, $r_{L1}=1.7$mΩ, $r_{L2}=650$mΩ, $R_{snub}=10$kΩ, $L_{lkg,pri}=0.04535$μH.

Table 4 lists the values of the different calculated power losses.

Comparing the two calculation results of P_{lkg} shows that the result of formula (21) (0.317mW), which is the total power loss of R_{snub} and D_{snub}, is lower than the result of formula (20) (48.314mW), which is the power loss of the leakage inductance itself. This phenomenon can be explained by examining the MOSFET's drain-source voltage. Fig.4 shows the MOSFET's drain-source voltage without the snubber. There are oscillations at f_r=14.7MHz, which are related to the resonant network that is composed of the output capacitor of the MOSFET switch, C_o, and L_{lkg}. Since the output capacitance of the MOSFET is about 10nF, the calculated L_{lkg} from the resonant frequency is 11.7nH, which is about 4 times lower than the measured inductance, 45.35nH. It can thus be concluded that the measured L_{lkg} is a gross over estimate of the real physical value. This could be a result of stray inductances at the primary during measurements. Consequently, the calculated and actual power losses of the leakage inductance will be lower. Further, due to the oscillations and the resulting high frequency current, most of the energy stored in the leakage inductance is absorbed in the parasitic resistances such as the primary and secondary wire resistances and input capacitor ESR. This explains why the energy transferred to the snubber unit is much lower than the energy stored in the leakage inductor. Moreover, not all the snubber unit energy goes to R_{snub} and D_{snub}; there is also a part that is dissipated by the ESR of C_{snub}.

Table 4
Power Losses of the Proposed Converter

P_{FET}	10.2mW
P_D	14.5mW
$P_{C_{in}}$	4.185mW
$P_{C_{out}}$	0.53mW
P_{rL_1}	14.3mW
P_{rL_2}	4.4mW
P_v	16.6mW
P_{lkg}	0.317mW
$P_{loss,tot}$	65mW



(a)

(b)

Fig.4: MOSFET's drain-source voltage (upper, 1V/div.) and gate-source voltage (lower, 5V/div.) without the snubber. (a) Horizontal scale 2μs/div . (b) Horizontal scale 200ns/div.

Fig.5 shows the estimated power loss percentage of the total power loss for the different power loss factors. The largest fraction of the power loss is P_v, followed by P_D and P_{rL1} and then P_{FET}.

Therefore, in order to increase the converter's efficiency, special attention should be taken for reducing the output diode conduction losses. The magnetic component should be considered in terms of the parasitic resistance of the primary winding, R_{L1}, and the core material. Finally, the MOSFET should be chosen with the smallest possible r_{DS}.

Some of the experimental results are presented in Fig.6, which is a plot of the experimentally measured efficiency as a function of switching frequency.

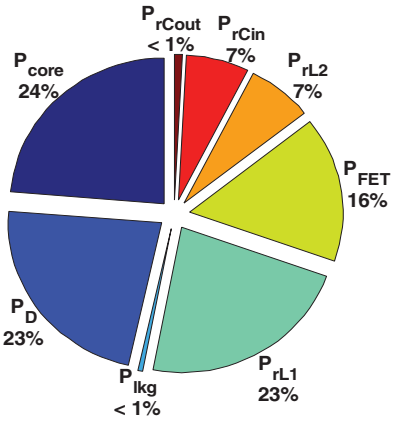


Fig.5: Power loss distribution.

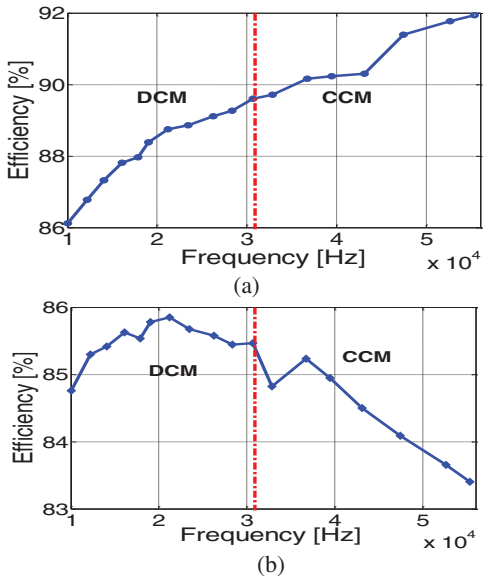


Fig.6: Conversion efficiency of proposed converter as a function of switching frequency for $0.5V$ input voltage and output power of about 1.2W. (a) Without considering gate drive losses. (b) Total efficiency when taking into account gate drive losses.

The theoretical results were compared to the results obtained with the prototype converter.

The specifications used in the power loss analysis and efficiency calculation are given in Table 3. The power loss analysis of the proposed converter is performed with the devices specified in Table 2.

Substituting the specifications of the proposed converter and the components' data from the experimental converter design into the theoretical efficiency formula (without considering gate drive losses) results in:

$$\eta = 94.42\%$$

Experimental results showed efficiency (without considering gate drive losses) of:

$$\eta = 92.943\%$$

When taking into account the gate drive losses in addition, this gives the result:

$$\eta = 83.402\%$$

The good agreement between calculated and measured results was also validated by comparison with different design parameter values.

V. Discussion and Conclusions

In this paper, a tapped-inductor boost converter for extremely low voltage sources, like TEG, was presented and a theoretical analysis for power loss and efficiency was carried out. Simulation and experimental results are shown to verify the theoretical analysis of the proposed converter.

In the proposed application, a Flat Magnetic device is used in order to reduce the leakage inductance. Therefore, the power losses due to the leakage inductance currents are reduced and, also, the snubber is not required.

The suggested analysis can be used to optimize the circuit design and thus can serve as a design guideline tool.

Further research will concentrate on finding an efficient, practical and simple solution for the most dominant power loss factors, which are the output diode conduction loss and the parasitic resistance of the tapped-inductor windings loss.

VI. Acknowledgment

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VII. References

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