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A soft switcher optimized for IGBTs in PWM topologies

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A novel soft switching scheme optimal for IGBTs is described, and investigated theoretically and experimentally. The proposed soft switcher applies an auxiliary IGBT switch which is operated for a short time interval during the turn-off commutation of the main IGBT. The main advantage of the proposed switcher is ZCS of the main and auxiliary IGBTs during both turn-on and turn-off, while all other power devices are also soft switched. The proposed soft switcher can be implemented in various types of PWM topologies. The experimental Boost converter was run at a switching frequency of 100 kHz to power levels of 1 kW. The efficiency was measured to be about 95% at a duty cycle of 0·45 and an output voltage of 300 V.

1. Introduction

Fast and ultra-fast IGBTs (Tsunoda *et al.* 1990) are considered to be a cost-effective choice in medium- to high-power applications. However, the relatively long turn-off time of these devices limits the switching frequency to about 25 kHz. This limitation is especially noticeable in the single-switch active power factor correction circuit, in which the use of an IGBT as the main switch could be highly beneficial. Consequently, the switching frequency limitation hampers the wide use of IGBTs in this class of applications, which are now of great commercial interest. This shortcoming could be corrected by a soft switching strategy that would reduce the switching losses of the IGBT, thereby permitting efficient operation at high switching frequencies.

The ideal arrangement for an IGBT soft switcher is zero current switching (ZCS) or zero voltage switching (ZVS) at turn-on, but ZCS at turn-off (Rangan *et al.* 1989, Chen and Stuart 1992). ZCS at turn-off is highly desirable because it can help to remove the stored charge which otherwise might cause a long current tail. The objective of this study was to explore a possible realization of a soft switcher that ensures soft switching during turn-on and ZCS during turn-off of the IGBTs while maintaining soft switching of all other power devices. The proposed topology applies a soft switches auxiliary IGBT that is operated for a short time interval during the turn-off commutation of the main IGBT. The proposed soft switcher is believed to be optimal for IGBTs because combats the main switching losses of the devices, namely the turn-off losses, while assuring soft switching at turn on. The moderate increase in the average switch current is compatible with the fact that the IGBTs 'on' voltage is practically independent of the current. The IGBT implementation of the soft switcher discussed here is believed to be novel. It shares some common features with a thyristor-based soft switching scheme described earlier (Birznieks 1974) but

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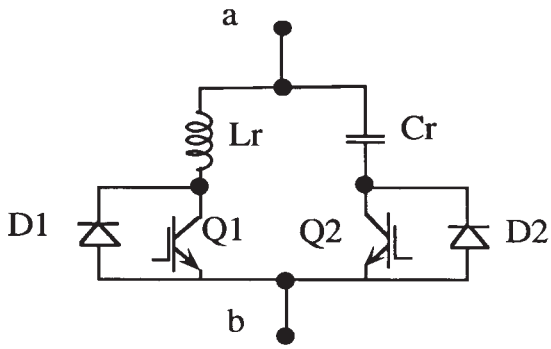

Figure 1. Basic circuit diagram of the proposed soft switcher, Q_1 main switch, Q_2 auxiliary switch.

differs from other proposed ZCS schemes for IGBTs (Hua *et al.* 1993). A similar approach was explored by Wang *et al.* (1994).

This paper presents a thorough theoretical analysis of the proposed switcher, including design guidelines. The paper also gives details of an experimental Boost converter used to test the proposed soft switching scheme and the experimental results that were obtained.

2. The dual switch topology

The dual-switch soft switcher topology (DSSS, Fig. 1) can be implemented in various types of PWM DC–DC converters: Buck, Boost, Buck-Boost, Cuk, Zeta and Sepic. The proposed switcher (Fig. 1) includes two branches connected in parallel. The main switch Q_1, shunted by an anti-parallel diode D_1 and connected in series with a resonant inductor L_r, form the first branch. The second branch comprises the auxiliary switch Q_2, shunted by another anti-parallel diode D_2 and connected in series with a resonant capacitor C_r. The operation of the auxiliary switch Q_2 is synchronized to the main switch Q_1. It is turned on just before the instant that the main switch Q_1 is due to be turned off. This creates a sinusoidal current in the series resonance network (L_r, C_r) which forces a negative current through the branch of the main switch (Q_1, D_1). Consequently, Q_1 current reduces smoothly to zero while the peak resonant current is channelled through the reverse diode D_1. When this diode is conducting, the gate drive of the main switch Q_1 can be removed under zero current conditions, thereby achieving true ZCS. During turn-on of the main switch Q_1, the resonant inductor L_r ensures ZCS by limiting the rate of the current rise. As will be shown below, Q_2 is also turned on and off under soft switching conditions.

3. Theoretical analysis

The analysis was carried out under the following assumptions:

(*a*) the converter elements are ideal

(*b*) the inductance of the main inductor in Buck, Boost and Buck-Boost converters, and the inductances of the two inductors in the Cuk, Zeta and Sepic converters are sufficiently large that their currents are practically constant during one switching cycle

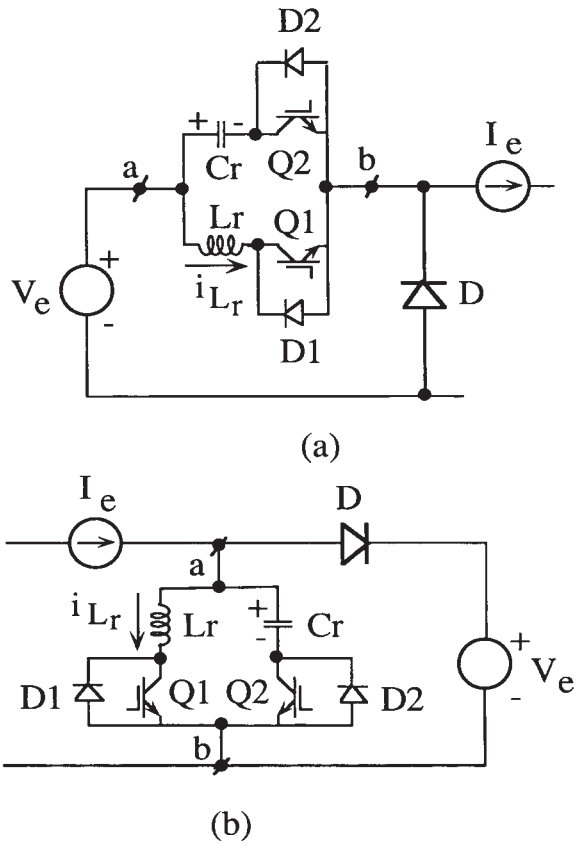

Figure 2. Equivalent circuits of (a) voltage-fed and (b) current-fed PWM converters with DSSS.

(*c*) the capacitance of the output capacitor in all converters and the capacitances of the main capacitors in the Cuk, Zeta and Sepic converters are sufficiently large that the voltages across them can be considered constant during one switching cycle.

These assumptions allow the use of unified equivalent circuits (Fig. 2) for the analysis of the DSSS operation in different types of voltage-fed and current-fed PWM DC–DC converters. Definitions of equivalent current and voltage sources I_e and V_e (Fig. 2) for various PWM topologies are given in Table 1; I_e is the current of the main inductor (I_L) in Buck, Boost and Buck-Boost converters and the sum of the currents of the main inductors (I_{L1}, I_{L2}) in Cuk, Zeta and Sepic converters; V_e is the voltage across the DSSS during the time intervals when both branches of DSSS are not conducting (i.e. when the path between points a and b in Fig. 2 is in the 'off' state). Table 1 also includes V_{sh}, the voltage across the main inductor (represented by I_e in Fig. 2) when the points a and b of the DSSS are shorted. The relationships between I_e and input I_{in} and output I_o currents and the relations between V_e, V_{sh} and input V_{in} and output V_o voltages are found by Kirchhoff's laws (Table 1).

The operation of the DSSS converter will be discussed in relation to the waveforms of Fig. 3 that were obtained by PSPICE (MicroSim Inc.) simulations carried out under the above assumptions. v_{g1} and v_{g2} are the gate voltages of the main Q_1 and auxiliary switch Q_2.

Topology	Buck	Boost	Buck-Boost, Cuk, Zeta, Sepic
I_e	I_o	I_{in}	$I_{in} + I_o$
V_e	V_{in}	V_o	$V_{in} + V_o$
V_{sh}	$V_{in} - V_o$	V_{in}	V_{in}

Table 1. Definitions of I_e, V_e and V_{sh} for various PWM topologies.

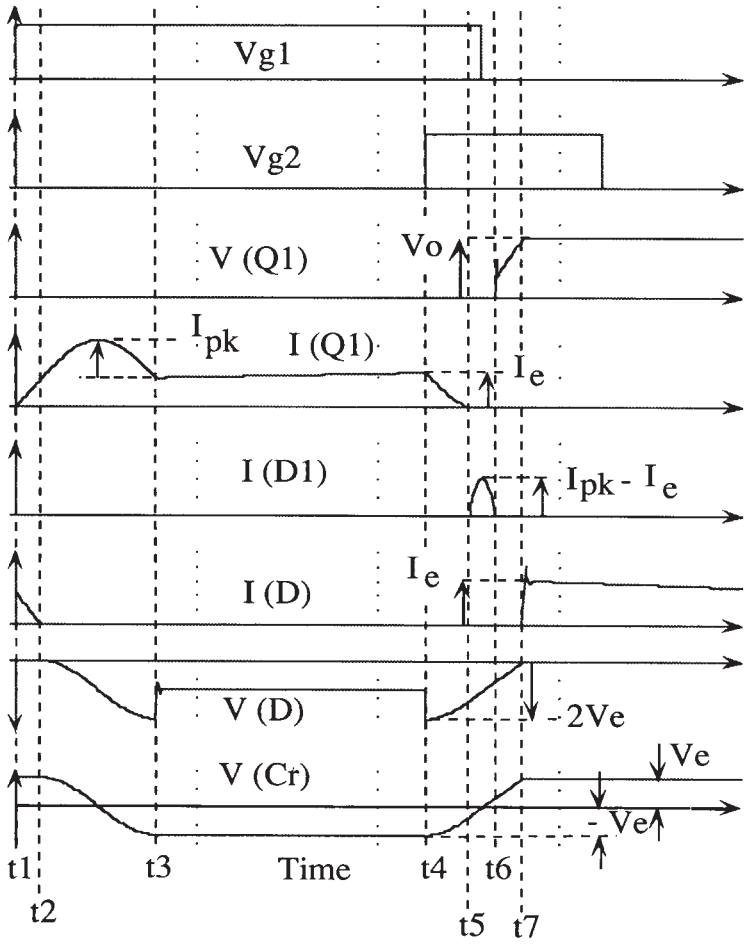

Figure 3. Basic waveforms of the proposed ZCS PWM converter of Fig. 2.

The DSSS switching cycle includes seven stages (Fig. 3):

In the interval that precedes t_1 both transistors of the DSSS are 'off' and the main diode of the converter D is 'on'. The voltage of the main transistor Q_1 and capacitor C_r is V_e. This interval ends when the main transistor Q_1 is driven to turn on.

In the interval $t_1 - t_2$ the main transistor Q_1 and the main diode D are conducting. As the current of Q_1 increases linearly, the current of the diode D decreases at the same rate because the sum of the two is I_e. This commutation interval ends when the current of the main diode D reaches zero and the diode turns off. The duration of the interval $t_1 - t_2$ is found to be

$$t_{1-2} = \frac{I_e L_r}{V_e} \tag{1}$$

Once the clamping effect of D has been removed, the resonant inductor L_r and resonant capacitor C_r are free to resonate. This resonant current will force the anti-parallel diode D_2 into conduction. That is, during the interval $t_2 - t_3$ both the main transistor Q_1 and the anti-parallel diode D_2 of the auxiliary switch are conducting. They close the resonant path of L_r and C_r and carry the sinusoidal current that develops. The magnitude of the resonant current and the capacitor C_r voltage can be expressed as

$$i_r = I_{pk} \sin [\omega_r(t - t_2)] \tag{2}$$

$$v_{C_r} = V_e \cos [\omega_r(t - t_2)] \tag{3}$$

where

$$I_{pk} = V_e \left(\frac{C_r}{L_r}\right)^{1/2} \tag{4}$$

$$\omega_r = \frac{1}{(L_r C_r)^{1/2}} \tag{5}$$

During this interval the current of the main switch i_{Q1} supports two components: the main current I_e and the resonant current i_r:

$$i_{Q1} = I_e + i_r \tag{6}$$

This interval ends when the resonant current i_r reaches zero and the anti-parallel diode D_2 turns off. At this instant, the capacitor C_r voltage is negative and equal, in its absolute magnitude, to the voltage V_e. The voltage on the main diode D at this instant is equal to $2V_e$ (Fig. 3). The duration of the interval $t_2 - t_3$ is found to be

$$t_{2-3} = \pi(L_r C_r)^{1/2} = \frac{T_r}{2} \tag{7}$$

where T_r is the resonant period.

In the interval $t_3 - t_4$ the main transistor Q_1 is conducting while the auxiliary switch Q_2 and all diodes are 'off'. The voltage across the auxiliary switch Q_2 and the main diode D is V_e. This interval ends when the auxiliary switch Q_2 is turned on. The voltage of the main diode D swings at this moment to $2V_e$.

During the interval $t_4 - t_5$ both transistors (Q_1 and Q_2) are conducting. They close the loop on the resonant circuit L_r and C_r, but now the resonant current i_r is in the reverse direction compared with the interval $t_2 - t_3$. Consequently, the current of the inductor L_r and the main switch Q_1 is now the difference between I_e and i_r:

$$i_{Q1} = I_e - i_r \tag{8}$$

To secure ZCS, the peak resonant current I_{pk} of (4) must be larger than I_e. If this condition is fulfilled, i_{Q1} will smoothly reach zero at an instant labelled t_5. At this moment the anti-parallel diode D_1 will turn on. The duration of the interval $t_4 - t_5$ is

$$t_{4-5} = \frac{1}{\omega_r} \sin^{-1}\left(\frac{1}{g}\right) \tag{9}$$

where

$$g = \frac{I_{pk}}{I_e} \tag{10}$$

In interval $t_5 - t_6$ the auxiliary transistor Q_2 and the anti-parallel diode D_1 conduct. The equivalent circuit is the same as in the interval $t_4 - t_5$. This interval ends when the diode D_1 current smoothly reaches zero, turning it off. The duration of the interval $t_5 - t_6$ is

$$t_{5-6} = \frac{2}{\omega_r} \cos^{-1}\left(\frac{1}{g}\right) \tag{11}$$

The gate drive of the main switch Q_1 must be removed during the interval $t_5 - t_6$ and preferably at its beginning. The magnitude of the capacitor C_r voltage in the intervals $t_4 - t_6$ can be expressed as

$$v_{C_r} = -V_e \cos\left[\omega_r(t - t_4)\right] \tag{12}$$

In the final operational stage $t_6 - t_7$, the auxiliary transistor Q_2 is conducting and all diodes are turned off. The capacitor C_r is charged under action of the current I_e. The interval ends when the voltage across the capacitor C_r (v_{C_r})

$$v_{C_r} = \frac{I_e}{C_r}(t - t_6) + V_e \sin\left(\omega_r \frac{t_{5-6}}{2}\right) \tag{13}$$

reaches V_e and the main diode D turns on. The duration of the interval $t_6 - t_7$ is found to be

$$t_{6-7} = \frac{C_r V_e}{I_e}\left[1 - \sin\left(\omega_r \frac{t_{5-6}}{2}\right)\right] \tag{14}$$

The instant t_7 marks the end of the complete switching cycle and the beginning of the next cycle. The gate drive of the auxiliary switch Q_2 must be removed during the interval $t_7 - (t_1 + T_s)$ and preferably at its beginning.

Note that the current and voltage waveforms of the main transistor Q_1 and the anti-parallel diode D_1 (Fig. 3) have the same form as in the isolated DC–DC converter previously described (Ivensky *et al.* 1994).

The results of the above analysis, summarized in Table 2, imply that both IGBTs and all diodes operate under soft-switching conditions. The maximum voltage applied to the main Q_1 and to the auxiliary Q_2 transistor is equal to V_e and the maximum reverse voltage of the main diode D is $2V_e$.

The converter voltage ratio V_o/V_{in} is derived as a function of the apparent duty cycle D_a defined as:

$$D_a = \frac{T_\Delta}{T_s} \tag{15}$$

where $T_\Delta = t_{1-4}$ is the time interval between t_1 when the main switch Q_1 is turned on and t_4 when the auxiliary switch Q_2 is turned on (Fig. 3); T_s is the switching period.

Transistor or diode	Turn-on	Turn-off
Q_1	ZCS	ZCS and ZVS
Q_2	ZCS	ZCS and ZVS
D	ZVS	ZCS and ZVS
D_1	ZCS and ZVS	ZCS
D_2	ZCS and ZVS	ZCS

Table 2. Switching conditions of the transistors and diodes.

The voltage transfer ratio is obtained by applying the assertion that in steady state the average voltage across the main inductor v_L must be zero, i.e.

$$\int_0^{T_s} v_L \, dt = 0 \tag{16}$$

where v_L is the instantaneous value of the voltage across the main inductor of the converter (in Cuk, Zeta and Sepic converters the voltages across both main inductors are equal). Note that in the equivalent circuits of Fig. 2 v_L is the voltage across the current source I_e: in the intervals $t_2 - t_3$ and $t_4 - t_7$

$$v_L = v_C + V_{sh} \tag{17}$$

in the interval $t_3 - t_4$

$$v_L = V_{sh} \tag{18}$$

and in the intervals $t_1 - t_2$ and $t_7 - (t_1 + T_s)$

$$v_L = V_{sh} - V_e \tag{19}$$

We assume that the duration of the interval $t_1 - t_2$ is negligibly small; and the capacitor voltage v_C in the interval $t_6 - t_7$ is described by (12) instead of (13) and therefore the duration of the interval $t_4 - t_7$ is equal to $T_r/2$.

By inserting (17)–(19) in (16) and applying (3), (7), (11), (12) and (15) we find

$$\frac{V_e}{V_{sh}} = \frac{T_s}{T_s - \left(T_\Delta + \dfrac{T_r}{2}\right)} = \frac{1}{1 - D_e} \tag{20}$$

where D_e is the equivalent duty cycle defined by

$$D_e = D_a + \frac{T_r}{2T_s} = \frac{t_{1-4} + \dfrac{T_r}{2}}{T_s} \tag{21}$$

That is, the equivalent duty cycle D_e includes two terms: the first is the apparent duty cycle D_a (t_{1-4}), and the second represents the resonant transition.

The general equation of the DC transfer ratio (20) applies to all PWM converter topologies. By inserting the relevant values of V_e and V_{sh} (from Table 1) we obtain the voltage ratio expressions for Buck:

$$\frac{V_o}{V_{in}} = D_e \tag{22}$$

Boost:

$$\frac{V_o}{V_{in}} = \frac{1}{1 - D_e} \tag{23}$$

Buck-Boost, Cuk, Zeta and Sepic:

$$\frac{V_o}{V_{in}} = \frac{D_e}{1 - D_e} \tag{24}$$

Note that these expressions conform to the corresponding PWM equations for each topology, except that the conventional PWM duty cycle D is replaced by an equivalent duty cycle D_e defined by (21).

The minimal value of the apparent duty cycle $D_{a\,min}$ (for proper operation) corresponds to the case when the auxiliary switch Q_2 is turning on at the same

instant when the anti-parallel diode D_2 turns off, i.e. when $t_{3-4} = 0$. In this case

$$T_\Delta = t_{3-1} \cong t_{3-2} = \frac{T_r}{2}$$

That is, the minimum apparent duty cycle $D_{a\,min}$ is

$$D_{a\,min} = \frac{T_r}{2T_s} \tag{25}$$

and the corresponding minimal value of the equivalent duty cycle is expressed as

$$D_{e\,min} = D_{a\,min} + \frac{T_r}{2T_s} = \frac{T_r}{T_s} = \frac{f_s}{f_r} \tag{26}$$

The maximum value of the equivalent duty cycle will approach unity under the assumption, made above, that the interval $t_1 - t_2$ (Fig. 3) is negligibly small. A more rigorous analysis shows that if $t_1 - t_2$ is considered then the more accurate upper bound to the equivalent duty cycle $D_{e\,max}$ is

$$D_{e\,max} = 1 - \frac{t_{1-2}}{T_s} \tag{27}$$

or, by applying (1), (4), (5), (7) and (10)

$$D_{e\,max} = 1 - \frac{T_r}{2\pi g T_s} = 1 - \frac{f_s}{2\pi g f_r} \tag{28}$$

The maximal value of the apparent duty cycle can be defined from the approximate equation

$$D_{a\,max} = 1 - \frac{T_r}{2T_s} \tag{29}$$

The average current of the main transistor $I_{Q1\,av}$ can be described by the following equation:

$$I_{Q1\,av} = I_e D_a + I_{pk} \frac{T_r}{\pi T_s} + \left[I_e \frac{t_{4-5}}{T_s} - I_{pk} \frac{T_r}{\pi T_s} \sin^2 \left(\frac{\omega_r t_{4-5}}{2} \right) - I_e \frac{t_{1-2}}{2T_s} \right] \tag{30}$$

In practical cases, the expression in the square brackets is negligibly small. Consequently (30) can be approximated by

$$I_{Q1\,av} = I_e D_a + I_{pk} \frac{T_r}{\pi T_s} = I_e D_e + \left(\frac{2}{\pi} I_{pk} - I_e \right) \frac{f_s}{f_r} \tag{31}$$

As would be expected, the average current of the main transistor is higher than in conventional hard switched PWM converters (where $I_{Q1} = DI_e$). However, if T_r (the resonance period) is much shorter than T_s and g (I_{pk}/I_e) is relatively small ($g = 1{\cdot}3, \ldots, 1{\cdot}5$) the penalty paid for ZCS will be rather negligible.

The peak current of the main transistor will be

$$I_{Q1\,max} = I_e + I_{pk} \tag{32}$$

and the average ($I_{Q2\,av}$) and peak ($I_{Q2\,max}$) currents of the auxiliary transistor Q_2 are found to be

$$I_{Q2\,av} = I_{pk}\frac{T_r}{\pi T_s}\sin^2\left(\frac{\omega_r t_{4-6}}{2}\right) + I_e\frac{t_{6-7}}{T_s} \tag{33}$$

$$I_{Q2\,max} = I_{pk} \tag{34}$$

The average and peak current of the anti-parallel diode D_1 have the largest values when the equivalent current of the converter I_e is near zero. In this case

$$I_{D1\,av} = \frac{I_{pk}T_r}{\pi T_s} \tag{35}$$

$$I_{D1\,max} = I_{pk} \tag{36}$$

The current of the anti-parallel diode D_2 is not sensitive to the equivalent current I_e. Its average and peak values are described by (35) and (36):

$$I_{D2\,av} = \frac{I_{pk}T_r}{\pi T_s} \tag{35'}$$

$$I_{D2\,max} = I_{pk} \tag{36'}$$

The average current of the main diode D can be calculated from the equation

$$I_{D\,av} = I_e\left[\frac{T_s - (T_\Delta + t_{4-7})}{T_s} + \frac{t_{1-2}}{2T_s}\right] \tag{37}$$

or approximately

$$I_{D\,av} = I_e(1 - D_e) \tag{37'}$$

The analysis given above describes the operation of an ideal DSSS. However, turn-off processes in practical transistors and diodes may affect the operation of a real DSSS switcher. In particular, a rapid reverse recovery of diode D_1 when it turns off (Fig. 4) will induce a high voltage on the inductor L_r and therefore across the main transistor Q_1. This will initiate parasitic oscillations in the resonant network which includes inductor L_r, the capacitances of the turned-off diode D_1 and the turned-off transistor Q_1. This undesired situation can be corrected by clamping

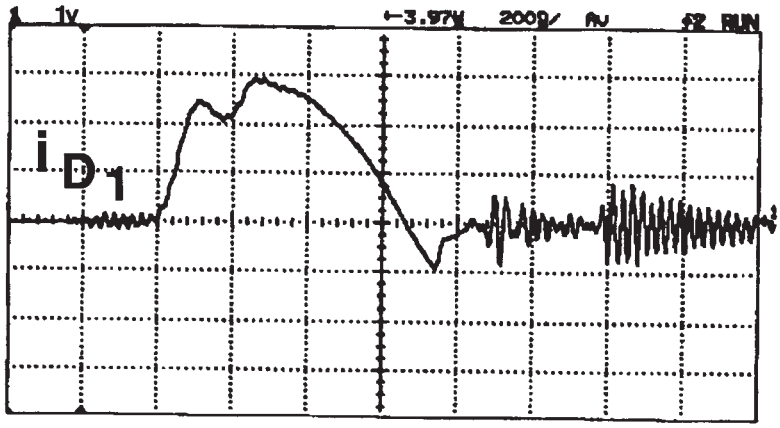

Figure 4. Conduction and reverse recovery of the anti-parallel diode (D1) of the Boost converter; vertical scale 1 A/div., horizontal scale 200 nS/div.

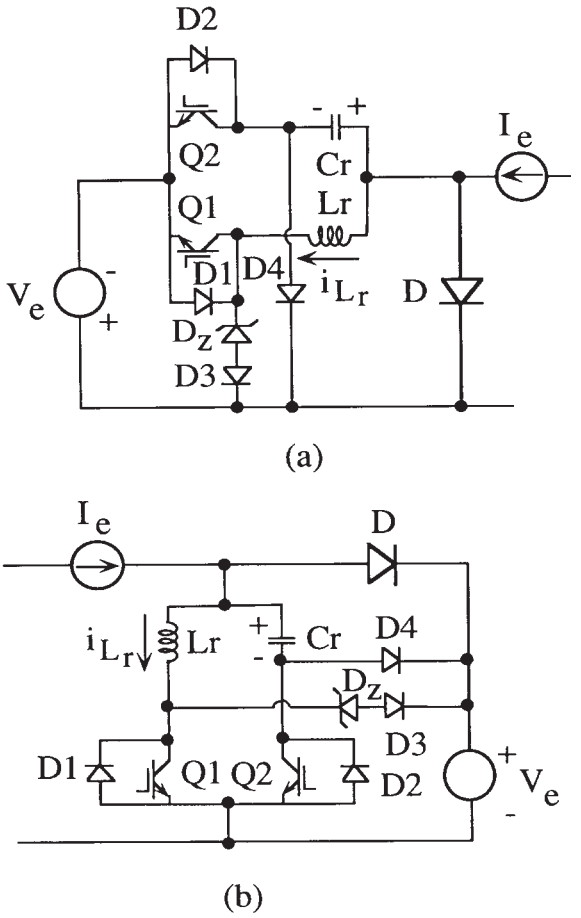

Figure 5. (a) Voltage-fed and (b) current-fed PWM converters with auxiliary protecting circuits.

the common point of the inductor L_r, the main transistor Q_1 and the anti-parallel diode D_1 to voltage source V_e through an auxiliary circuit which includes a Zener diode D_Z and an ordinary diode D_3 (Fig. 5). In this case the transistor voltage v_{Q1} will be limited to $V_e + V_Z$, where V_Z is the breakdown voltage of D_Z. The function of the Zener diode is to help reduce to zero any residual currents in L_r (such as the reverse recovery current of D_1) after the main switch Q_1 is turned off. Without the Zener diode, the current of the inductor L_r will continue to flow through D_3 increasing overall losses and causing hard switching of Q_1 at turn on.

The practical switcher (Fig. 5) includes an additional diode D_4 that clamps the auxiliary transistor Q_2 to the voltage source V_e to protect Q_2 against voltage spikes generated by stray inductances.

4. The experimental circuit

The experimental boost converter (Fig. 6) was operated at a switching frequency of 100 kHz to power levels of 600 W when Q_1 was IRGBC20U, and up to 1 kW when Q_1 was IRGPC50U. The voltage and current waveforms (Fig. 7) were found to be smooth and practically identical to the theoretical waveforms depicted in Fig. 3, except for the trench that follows the peak current of main switch current Q_1. The

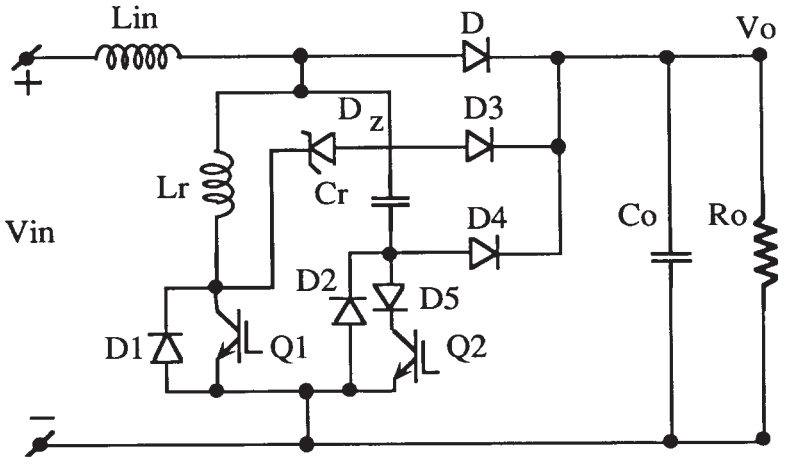

Figure 6. Circuit diagram of the experimental 1 kW converters: L_r 10·3 μH; C_r 17·2 nF; L_{in} 0·45 mH; Q_1 IRGPC50U, Q_2 IRGBC20U; D, D_4 MUR8100; D_1, D_2, D_5 MUR460; D_3 MUR860; D_Z 5 V Zener.

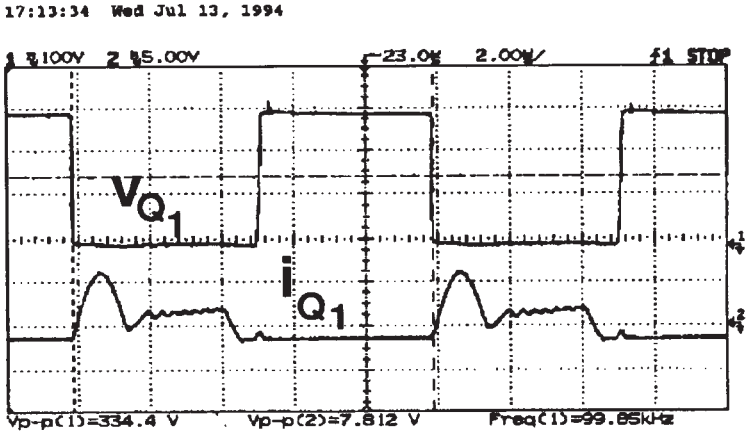

Figure 7. Typical waveforms of the proposed Boost converter; vertical scales 100 V/div. and 5 A/div., horizontal scale 2 μS/div.

trench is attributed to the reverse recovery of the anti-parallel diode D_2. This deviation from the theoretical waveform has only a slight affect on the operation of the switcher; it reduces somewhat the maximum voltage on C_r (by about 10%). This, in turn, reduces the maximum peak current during turn-off commutation.

The experiments also confirmed the conjecture that the proposed topology alleviates the problem associated with the reverse recovery of the main diode (Fig. 8). The efficiency of the experimental prototype was measured to be 94·6% under the following operational conditions: $f_s = 100$ kHz, $V_{in} = 140{\cdot}5$ V, $I_{in} = 7{\cdot}55$ A, $V_o = 261$ V, $P_o = 1004$ W, $D_a = 0{\cdot}45$.

5. Discussion and conclusions

The theoretical and experimental investigation of this study suggest that the proposed soft switching scheme is highly effective in reducing both the turn-on

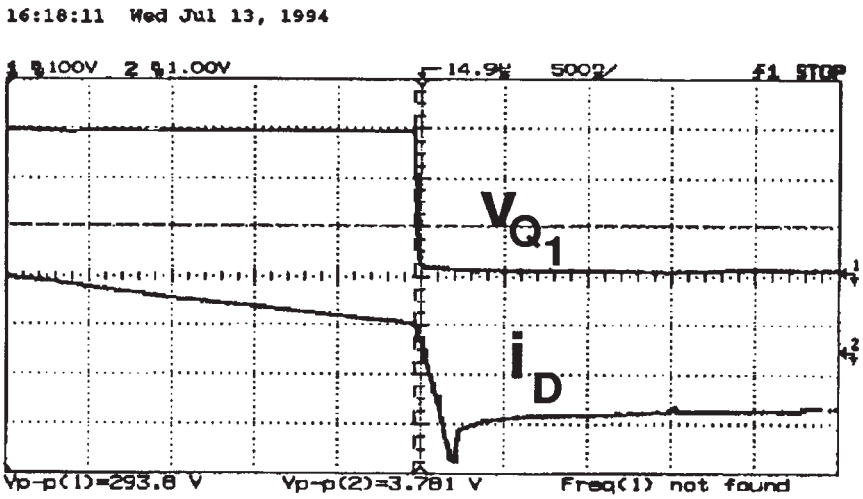

Figure 8. Reverse recovery of the main diode D of the proposed Boost converter; vertical scales 100 V/div. and 1 A/div., horizontal scale 500 nS/div.

and turn-off losses of the main and auxiliary IGBTs. It would thus appear that operation of this IGBT soft switcher in active power factor correction circuits (APFC) at a 100 kHz switching frequency and above becomes practical and rather easy to implement. The experimental results of this study demonstrate that the extra peak current stresses of the proposed ZCS circuit can easily be managed by commercially available IGBTs. The additional losses associated with these stresses are rather low due to the fact that they represent only a moderate increase in the average currents which are the dominant source of losses for the main and auxiliary IGBTs. Furthermore, because the main Q_1 and auxiliary Q_2 transistors are soft switched, both can be IGBTs. This in turn reduces the losses of the auxiliary switch even when a smaller IGBT is used. The only concern would be to select an IGBT that can withstand the expected peak resonance current.

Aside from the larger component count, the main penalty of the DSSS topology is the higher voltage stresses of the main diode D; twice that of the corresponding hard switched topology. The need to use a diode with a higher breakdown voltage will, in practice, increase the conduction losses of the diode due to the larger voltage drop of a higher voltage diode (or a combination of two diodes in series). This drawback is compensated for to a large extent by the fact that the diode is now soft switched (Fig. 8). Consequently, both the reverse recovery losses and EMI emission associated with the turn-off of this diode are considerably smaller.

Notwithstanding the ZCS at turn-off, the main as well as the auxiliary IGBTs need to be fast units if switching frequency is high. This is a consequence of the fact that the transistors must be fast enough to cope with the fast, albeit soft, turn-on and turn-off transitions and short delays available for recovery. The experimental results of this study suggest that the proposed DSSS provides a speed-up factor of about three. That is, an IGBT that is limited by hard switching losses to a given switching frequency, can be switched three times faster if the DSSS is applied. Under these conditions the switching losses will be about the same. This seems to suggest that the benefits of applying the DSSS topology could be substantial.

Appendix: Design guidelines

We are given the maximum output power (for ZCS) $P_{o\,max}$, output voltage V_o, the range of input voltages $V_{in\,low}, \ldots, V_{in\,high}$, the ripple of the main inductor current $(\Delta I_L/I_L)_{max}$ (in Cuk, Zeta and Sepic converters the ripple currents of both inductors must be given), and the switching frequency f_s.

(*a*) Calculate the minimum and maximum values of the equivalent duty cycle $D_{e\,min}$ and $D_{e\,max}$ for the converter topology under consideration (from (22)–(24)).

(*b*) Calculate the maximum DC input current from $P_{o\,max}$ and $V_{in\,low}$

$$I_{in} = \frac{P_{o\,max}}{\eta V_{in\,low}}$$

where η is the efficiency ($\eta = 0{\cdot}94, \ldots, 0{\cdot}97$).

(*c*) Calculate the average output current from $P_{o\,max}$

$$I_o = \frac{P_{o\,max}}{V_o}$$

(*d*) Find the equivalent current I_e and the equivalent voltage V_e from Table 1 (note that in Buck, Buck-Boost, Cuk, Zeta and Sepic converters V_e corresponds to $V_{in\,low}$).

(*e*) Find the maximum value of the equivalent current, in Buck, Boost and Buck–Boost converters:

$$I_{e\,max} = I_e\left[1 + \left(\frac{\Delta I_L}{I_L}\right)_{max}\right]$$

in Cuk, Zeta and Sepic converters:

$$I_{e\,max} = I_e\left[1 + \left(\frac{\Delta I_{L1}}{I_{L1}}\right)_{max} + \left(\frac{\Delta I_{L2}}{I_{L2}}\right)_{max}\right]$$

(*f*) Set $g = 1{\cdot}3, \ldots, 1{\cdot}5$.

(*g*) Calculate the resonant capacitor peak current

$$I_{pk} = gI_{e\,max}$$

(*h*) Calculate the required characteristic impedance of the resonant circuit

$$Z_r = \frac{V_e}{I_{pk}}$$

(*i*) Choose $\Delta i/\Delta t = 10, \ldots, 100$ A μs in the interval $t_1 - t_2$. Note that $\Delta i/\Delta t$ will determine the peak of the reverse recovery current of the main diode D accordingly $\Delta i/\Delta t\, t_{rr}$, where t_{rr} is the reverse recovery time of the diode.

(*j*) Calculate the resonant inductance

$$L_r = \frac{V_e}{\frac{\Delta i}{\Delta t}}$$

(*k*) Calculate the resonant capacitance

$$C_r = \frac{L_r}{Z_r^2}$$

(*l*) Calculate the resonant frequency

$$f_r = \frac{1}{2\pi(L_r C_r)^{1/2}}$$

and check realization of the constraints (26) and (28). If the calculated value of f_r is too low, return to step (*i*) and increase $\Delta i/\Delta t$.

(*m*) Calculate the average and peak currents of the main transistor Q_1 using (31) and (32), of the auxiliary transistor Q_2 using (33) and (34) and of the anti-parallel diodes D_1 and D_2 using (35), (35′), (36) and (36′).

(*n*) Calculate the average current of the main diode D using (37′).

(*o*) Choose the transistors Q_1 and Q_2 and the diodes D_1, D_2 and D from the results of steps (*m*) and (*n*), and taking into account that the maximum voltage value applied to Q_1, Q_2, D_1 and D_2 is V_e but $2V_e$ for D.

(*p*) Calculate the minimal duration of the gate voltage impulse of the auxiliary switch using (9), (11) and (14)

$$t_{g2\,\min} = t_{4-5} + t_{5-6} + t_{6-7}$$

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