The Dynamics of a PWM Boost Converter with Resistive Input

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***Abstract*— This paper investigates the large- and small-signal response issues and, in particular, the inner loop gain and outer loop response of an indirect control method for active power-factor correction. The control scheme is based on sensing the average inductor current and generating a D_{OFF} (the complement of the switch duty cycle) which is proportional to the current. The method is demonstrated by considering the performance of a boost-type active power-factor corrector (APFC) that does not need to sense the input voltage. Theoretical and experimental results confirm the validity of the approach and demonstrate that the proposed method can be useful in the design of robust APFC with low total harmonic distortion. The indirect control method investigated in this paper is also compared to the classical direct APFC control method, pointing to the differences between the two.**

***Index Terms*— Active power-factor corrections, modeling, power converters, simulation.**

I. Introduction

THE current interest in active power-factor correction (APFC) [1]–[10] prompts investigators to look for improved methods to shape the input current of pulsewidth modulation (PWM) converters. Two groups of solutions have been proposed hitherto for continuous-current-mode (CCM) systems, those that rely on direct current feedback [2] and those that apply indirect input current control [3]–[10]. The main difference between the two groups is related to input voltage sensing. In the direct methods, the control of the input current is achieved by an "inner" feedback loop for which the rectified input voltage serves as the reference to the desired shape of the input current. In the indirect control method, the information regarding the desired input current shape is obtained by sensing the inductor current, the switch current, or the diode current [3]. This is possible, in theory, considering the fact that these currents are a function of the input voltage. The indirect control method has many advantages, such as being less susceptible to the switching noise which is normally superimposed on the rectified input voltage node.

The indirect control scheme of APFC introduced in [11] is similar to the approach presented earlier in [6], the main difference being the way in which the input current is averaged. In [6], one-cycle averaging was used, whereas, in [11], a simply low-pass filtering is suggested. Other earlier approaches of indirect APFC sensed the peak current [3]–[6] or switch current [7]. The objective of this paper was to study the large- and small-signal responses of a boost converter applying the indirect control APFC of [11]. This was accomplished by developing average models of the system and deriving their small-signal response. Finally, the difference between the proposed control scheme and the classical, inner current feedback method [2] is also explained in terms of basic control theory ideas. Although the main thrust of this paper is to discuss the dynamics of the system, we first summarize the concept of the control method—for the sake of completeness.

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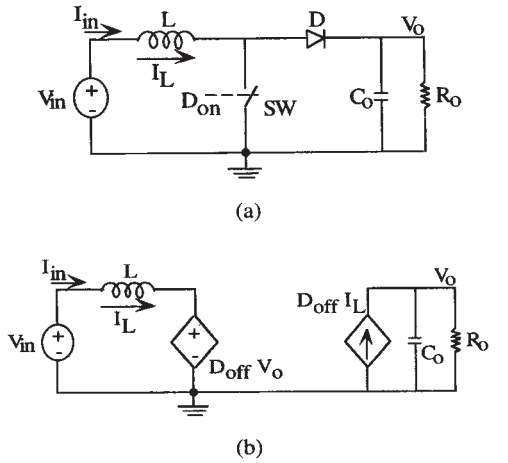


Fig. 1. (a) The boost converter and (b) its behavioral average model (after [9] and [10]).

II. The Boost Topology

The indirect APFC control method to be studied will first be described by a simple intuitive reasoning in relation to the boost converter [Fig. 1(a)]. It is assumed that the converter is driven by a duty cycle D_{on} and that it operates under CCM conditions. As shown previously [13], [14], the function of the converter can be represented by the behavioral model of Fig. 1(b). One can now apply a power circuit theory corollary: under stable conditions, the average voltage across a power inductor L must be zero (otherwise, the current will rise to infinity).

Assuming that the circuit is stable (as will be shown below), this implies [Fig. 1(b)]

$$V_{in}(av) = D_{off} V_o(av) \tag{1}$$

where D_{off} is $(1 - D_{on})$, $V_{in}(av)$ is the average input voltage, and $V_o(av)$ is the average output voltage. Averaging is over

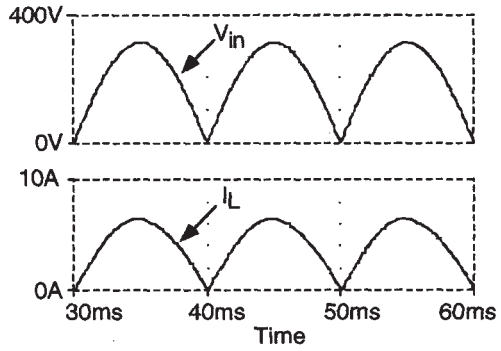


Fig. 2. Results of average simulation of proposed control on the behavioral model of Fig. 1(b).

one switching cycle under the assumption that the switching frequency is much higher than the bandwidth of V_{in} and of V_o.

Since the average input current $I_{\text{in}}(\text{av})$ is equal to the average inductor current $I_L(\text{av})$, (1) can be manipulated to the form

$$\frac{V_{\text{in}}(\text{av})}{I_{\text{in}}(\text{av})} = \frac{D_{\text{off}} V_o(\text{av})}{I_L(\text{av})}. \tag{2}$$

Similar expressions were obtained in [3].

To make the input resistive with an input resistance R_e, we require

$$\frac{V_{\text{in}}(\text{av})}{I_{\text{in}}(\text{av})} = R_e = \frac{D_{\text{off}} V_o(\text{av})}{I_L(\text{av})}. \tag{3}$$

That is, a resistive input will be observed if D_{off} is programmed according to the rule

$$D_{\text{off}} = \left(\frac{R_e}{V_o(\text{av})}\right) I_L(\text{av}), \qquad 0 < D_{\text{off}} < 1. \tag{4}$$

It should be noted that this relationship introduces negative feedback and, hence, helps to insure stable operating conditions (as is shown in the more rigorous analysis given below).

The control concept of (4) was tested by running a behavioral SPICE simulation [13], [14] on the model of Fig. 1(a). The results presented in Fig. 2 are for a typical 1-kW APFC stage. D_{off} was set according to (4), $(R_e/V_o(\text{av}))$ was 0.127 A^{-1}, and $V_{\text{in}}(\text{av}) = |310 \sin(2\pi 50t)|$ (volts), where t is time (seconds). Other parameters were $R_o = 144\ \Omega$, $C_o = 1000\ \mu\text{F}$, and $L = 1.1$ mH. The system reached a steady-state output voltage of 380 V while the input current clearly demonstrates the resistive nature of the converter's input terminals (Fig. 2).

In active power-factor correction systems, V_o needs to be stabilized and R_e adjusted as a function of the load and input voltage. One possible way to achieve this is proposed in Fig. 3. The voltage error amplifier (*E/A*) should have a slow response, so as not to react within the mains cycle. The multiplier (*M*) generates the programmed voltage that is modulated by the PWM modulator to obtain D_{off}. This control scheme was tested by a PSPICE (Microsim Company) cycle-by-cycle simulation. The parameters of the power stage and modulator were as given above. The bandwidth of the error amplifier (*E/A*) was 10 Hz, switching frequency was 50 kHz,

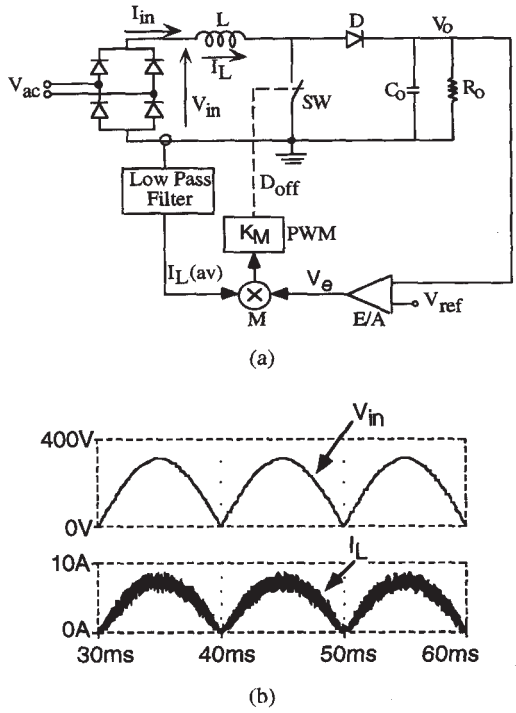


Fig. 3. (a) Possible realization of proposed control method. (b) Results of cycle-by-cycle simulation of its performance.

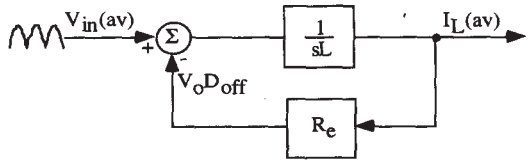


Fig. 4. Simplified block diagram of proposed APFC control scheme.

and the bandwidth of the low-pass filter [Fig. 3(a)] was 80 kHz. The simulation results [Fig. 3(b)] clearly demonstrate the validity of the approach.

III. Dynamic Response

A. Current Tracking—Approximate Analysis

The dynamic response of the proposed converter can be studied by the simplified control block diagram presented in Fig. 4, which describes the left mesh of Fig. 1(b). The summing junction reconstructs the total voltage imposed on the inductor (L), while the feedback path represents the D_{off} programming according to (3) and (4). This block diagram representation assumes that the output voltage (V_o) is constant with negligible ripple and that R_e is set to a given constant value. It is also assumed that the bandwidth of the low-pass filter [Fig. 3(a)] is wider than the system's response. Under these conditions, the system (Fig. 4) is linear and the loop gain (βA) is found to be

$$\beta A = (R_e)\left(\frac{1}{sL}\right) = \frac{R_e}{sL} \tag{5}$$

which represents a bandwidth of $R_e/2\pi L$ and a phase margin of 90°. This implies that the "inner" current feedback loop is

unconditionally stable for any input or output voltages—under the assumption that V_o is constant, but, as the additional analysis given below shows, this conclusion is also valid for practical cases.

The closed-loop response (input current as a function of input voltage) is clearly

$$\frac{I_L(\text{av})}{V_{\text{in}}(\text{av})} = \frac{1}{R_e}\frac{1}{1+s\dfrac{L}{R_e}} \tag{6}$$

where $I_L(\text{av})$ and $V_{\text{in}}(\text{av})$ are the (low frequency) inductor (and input) current and the (low frequency) input voltage, respectively. This result implies that the tracking bandwidth is $R_e/2\pi L$. This equation agrees with [4, eq. (33)], which also shows that the response is represented by a first-order system, but there it was not related to R_e. However, as discussed below, the single-pole representation is only an approximation.

In practical APFC applications for 50/60-Hz power lines, the tracking bandwidth ($\text{BW}_{I_{\text{in}}}$) should be at least 1 kHz [17] or, in general,

$$\frac{R_e}{2\pi L} = (\text{BW}_{I_{\text{in}}}). \tag{7}$$

This constraint can now be checked against other design considerations and, in particular, the size of the inductor required to keep the current ripple within reasonable limits. Maximum ripple is reached at $D_{\text{on}} = 0.5$, that is, when $V_{\text{in}}(\text{av}) = 1/2\ V_o(\text{av})$. The ripple ($\Delta I$) at this point will be

$$(\Delta I)_{D_{\text{on}}=0.5} = \frac{V_{\text{in}}(\text{av})}{2f_sL} \tag{8}$$

where f_s is the switching frequency. The ripple ratio ($\Delta I/I_{\text{in}}(\text{av})$) will be

$$\left(\frac{\Delta I}{I_{\text{in}}(\text{av})}\right)_{D_{\text{on}}=0.5} = \frac{\dfrac{V_{\text{in}}(\text{av})}{2f_sL}}{\dfrac{V_{\text{in}}(\text{av})}{R_e}} = \frac{R_e}{2f_sL}. \tag{9}$$

Combining (7) and (9), we obtain

$$\left(\frac{\Delta I}{I_{\text{in}}(\text{av})}\right)_{D_{\text{on}}=0.5} = \frac{\pi}{f_s}(\text{BW}_{I_{\text{in}}}) \tag{10}$$

or

$$(\text{BW}_{I_{\text{in}}}) = \frac{1}{\pi}f_s\left(\frac{\Delta I}{I_{\text{in}}(\text{av})}\right)_{D_{\text{on}}=0.5} \tag{11}$$

which implies that, for a design of, for example,

$$\left(\frac{\Delta I}{I_{\text{in}}(\text{av})}\right)_{D_{\text{on}}=0.5} = 0.1$$

the tracking bandwidth will be about $f_s/30$. This is obviously more than enough for modern switch-mode systems in which $f_s > 50$ kHz. For higher ripple ratios, the bandwidth will be larger.

Bandwidth limitation might be a problem only when the input inductor becomes very large, but this is also the case in conventional CCM APFC [16]. It is also interesting to note that the inner current loop bandwidth is linear with R_e (7). Hence, when the load power drops and, hence, R_e becomes larger, the possible bandwidth gets, in fact, larger. That is, once designed for maximum output power, tracking is assured for lower power levels as long as CCM is maintained.

Similar to the case of the classical APFC control, the propagation of the inductor ripple may give rise to subharmonic oscillations. However, this instability effect is less likely here, because the complete inductor current is compared to the ramp. Since the ripple will be normally a small fraction of the current, and since the ramp acts as a "slope compensation" [12], the system will be more robust. This situation is different from the conventional APFC control scheme [2] in which the "dc" value of the current is offset (by the output of the error amplifier), but the ripple is amplified. Nonetheless, when large ripple currents are expected, it might be advisable to attenuate the ripple component by a proper low-pass filter, and the system will be more robust.

The analysis of discontinuous-current-mode (DCM) operation is beyond the scope of this paper and will be discussed in a subsequent publication.

B. Current Tracking—Small-Signal Response

A more rigorous analysis of the current tracking raises two issues: 1) for a finite output capacitor V_o cannot be assumed to be constant and 2) for a nonconstant V_o, the system is nonlinear. To overcome these problems, the system was linearized around a given operating point by differentiating the average model of Fig. 1(b) [13], [14]. Here, we treat the system as a dc–dc converter with the input voltage frozen to one value. This often-used simplification is needed in order to gain an insight into the dynamic issue and should be treated as an approximation.

The inner loop gain was derived by the model shown in Fig. 5, in which all the dc values (e.g., V_{in}) were subtracted. The loop gain is derived by assuming that d_{off}, which drives the system is an independent variable and calculating the dummy dependent variable d'_{off}. The inner (current) loop gain (βA) is, thus, equal to $d'_{\text{off}}/d_{\text{off}}$ (Fig. 5). Following this method, the inner loop gain was found to be

$$\beta A = \frac{sC_oR_oR_e + R_e + D_{\text{off}}^2R_o}{s^2LC_oR_o + sL + D_{\text{off}}^2R_o} \tag{12}$$

where capital D_{off} denotes the steady-state values. For $C \to \infty$, the function reduces to (5) found earlier for the case V_o = constant. The exact solution of the loop gain (12) includes a zero (f_z) at

$$f_z = \frac{1}{2\pi}\left(\frac{1}{C_oR_o} + \frac{D_{\text{off}}^2}{C_oR_e}\right) \tag{13}$$

and a complex pole (f_p) at

$$f_p = \frac{D_{\text{off}}}{2\pi\sqrt{LC_o}}. \tag{14}$$

To preserve a safe phase margin, the double pole should be at a lower frequency than the crossover of βA (12). That is, the ratio between the crossover frequency of $\beta A(R_e/2\pi L)$

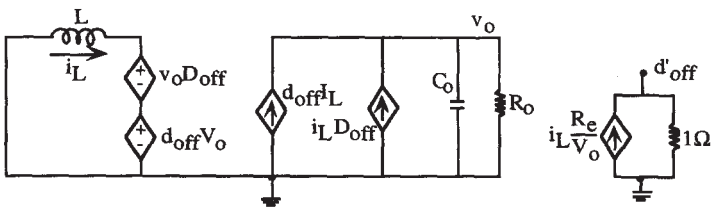


Fig. 5. Average behavioral small-signal model for deriving inner loop gain.

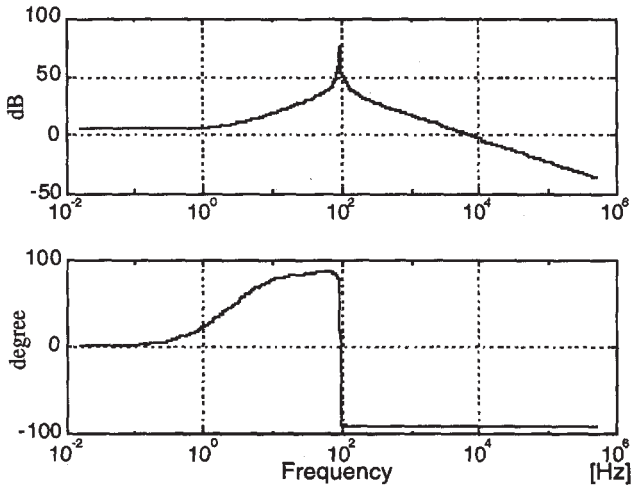


Fig. 6. Inner (current) loop gain for the boost stage drawn from (12) for the parameter values given in Section II. Upper trace: amplitude. Lower trace: phase.

and f_p should be at least five, namely,

$$\frac{R_e}{D_{\text{off}}}\sqrt{\frac{C_o}{L}} > 5. \tag{15}$$

The bode plots of Fig. 6, drawn for the values given in Section II and $D_{\text{off}} = 0.57$, demonstrate the nature of (12). With these practical values, the crossover is around 10 kHz (as predicted from the approximate analysis) with a phase margin of 90°. In engineering design, care should be paid to the location of the complex pole. If the crossover slope of the current loop gain is maintained at −20 dB/°, the general behavior will be like predicted by the approximate analysis (5).

Following the same linearization procedure, the inner loop response (i_L/v_{in}) was found to be

$$\frac{i_L}{v_{\text{in}}} = \frac{sC_oR_o + 1}{s^2LC_oR_o + s(L + C_oR_oR_e) + 3R_e} \tag{16}$$

with a zero at

$$f_z = \frac{1}{2\pi C_oR_o} \tag{17}$$

and a double pole at

$$f_p = \frac{1}{2\pi}\sqrt{\frac{3R_e}{LC_oR_o}}. \tag{18}$$

When $C_o \to \infty$, the output voltage can be considered constant and (16) is reduced to the approximate analysis solution (6). The nature of (16) can be appreciated by considering the bode plots of Fig. 7 that were drawn for the numerical values

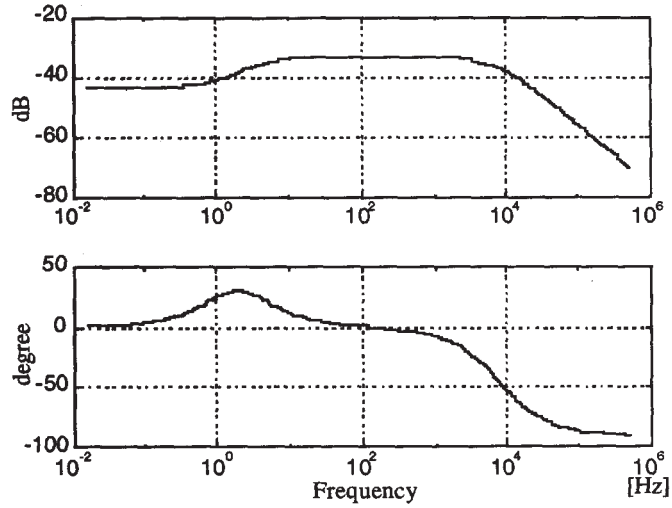


Fig. 7. Small-signal line-voltage to input-current transfer function (16) for the parameter values given in Section II. Upper trace: amplitude. Lower trace: phase.

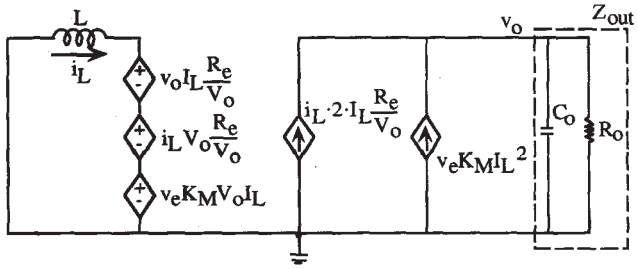


Fig. 8. Average behavioral small signal model for deriving outer loop transfer function.

given in Section II. For the range of interest (100 Hz–1 kHz), tracking is excellent. At very low frequencies (dc), the gain is somewhat lower due to the fact that V_o is now variable. This might introduce some distortion [17]. However, as is demonstrated below, the actual distortion introduced is minor.

C. Outer Loop Gain

The outer open-loop response (v_o/v_e) was also derived by linearizing the system around a given operating point (Fig. 8). Here, again, we treat the system as a dc–dc converter with the input voltage frozen to one value. The outer response was found to be

$$\frac{v_o}{v_eK_M} = \frac{sLI_L^2R_o - V_o^2}{s^2LC_oR_o + s(L + C_oR_oR_e) + 3R_e} \tag{19}$$

where K_M is the transfer constant of the PWM modulator [D_{off}/(volt·ampere)].

This transfer function includes a right-half-plane zero (RHPZ) at

$$f_z = \frac{R_e}{2\pi L} \tag{20}$$

and a double pole at

$$f_p = \frac{1}{2\pi}\sqrt{\frac{3R_e}{LC_oR_o}} \tag{21}$$

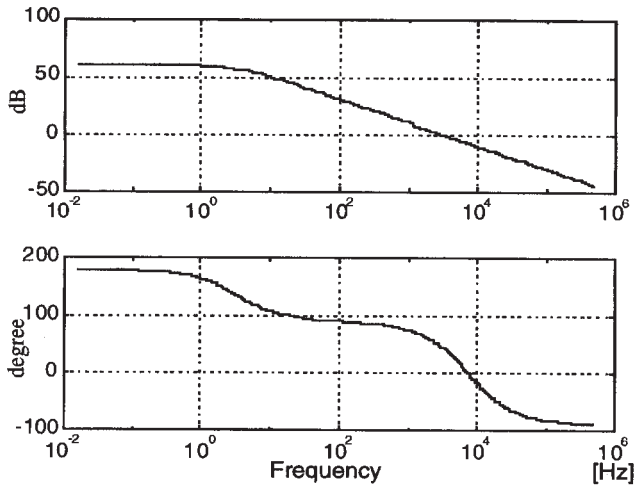


Fig. 9. Outer loop transfer function (19) for the parameter values given in Section II. Upper trace: amplitude. Lower trace: phase.

The typical response of Fig. 9 (for the value given in Section II) reveals the nature of the outer loop transfer function. Excess phase shift is evident due to the RHPZ. However, since the required bandwidth is small (up to 10 Hz), classical phase compensation procedures should suffice to stabilize the outer loop [Fig. 3(a)].

The gain of (19) at low frequencies ($s \rightarrow 0$) reduces to

$$\frac{v_o}{v_e K_M} = \frac{[V_o(\text{av})]^2}{3R_e} \tag{22}$$

Namely, the dc gain is a function of R_e, that is, the power level and rms input voltage. For optimum outer loop response, one may wish to introduce feedforward compensation [17]. This, however, will require sensing of the input voltage, but only for the dc (heavily filtered) component.

D. Effect of Output Ripple

Output ripple due to the practical finite value of the output capacitor will tend to distort the input current. Two effects can be envisioned. One is related to the fact that V_o (Fig. 1) includes an ac component and is not pure dc, as assumed. Second, the output of the outer loop error amplifier [Fig. 3(a)] will have an ac component that will modulate the current programming signal. The latter is not different from the case in conventional CCM APFC control [16], [17] and will not be dealt with here. The nonlinear effect of the ripple on the inner loop was studied by simulation for the 1-kW case considered in Section II, and the results are summarized in Table I. It is evident that, even for the impractical case of $L = 0.5$ mH and $C_o = 100$ μF (1 kW), which results in a ripple (V_r) of 83 $V_{p\text{-}p}$, the expected THD is relatively small, about 5% (Table I).

Simulation was also used for studying the effect of input voltage on the input current distortion (Fig. 10). From a practical point of view, the THD change for the range 85–250 V_{rms} is negligibly small.

IV. Experimental Results

The theoretical considerations and results of the analyses given in the above sections were verified by average simulation and laboratory experiments. The agreement between the theoretical derivation and average simulation was excellent to the point of being identical. It is indeed felt that average simulation could be conveniently used as a design assistant to check dependence on input voltage, power level, etc.

A prototype converter was also built and tested in open outer loop, that is, without controlling the output voltage [Fig. 3(a)]. In this mode, the output voltage will depend on the value of the programmed R_e. The actual implementation (Fig. 11) included a boost stage and a simple D_{off} programming scheme. The bandwidth of the current amplifier was kept very high (80 kHz) to test the sensitivity to subharmonic oscillations. None was observed.

The tracking quality obtained experimentally is demonstrated by comparing the line current to the rectified input

TABLE I
Percent Harmonic Distortion and THD of Input Current (for 3–9 Harmonic Components) as Obtained by Average Simulation for 1-kW APFC, $V_o = 380$ V, and Input Voltage of 220 V_{rms}

L mH	C_o mF	V_r Volt (p-p)	3rd harmonic %	5th harmonic %	7th harmonic %	9th harmonic %	THD3-9 %
1	1	8	0.4	1.1	1.2	0.6	1.8
1	0.5	16	0.9	1.1	1.1	0.7	1.9
1	0.1	82	4.3	1.3	1.1	0.6	4.6
0.5	1	8.5	2.1	1.9	1.2	0.7	3.2
0.5	0.5	17	2.1	1.8	1.1	0.6	3.0
0.5	0.1	83	4.4	2.3	1.2	0.7	5.1

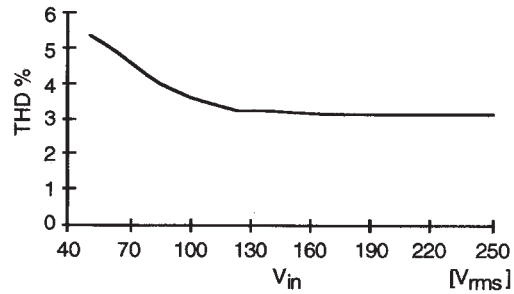


Fig. 10. THD as a function of the input voltage as obtained by average simulation for 1-kW APFC, $V_o = 380$ V, $L = 1$ mH, and $C_o = 1$ mF.

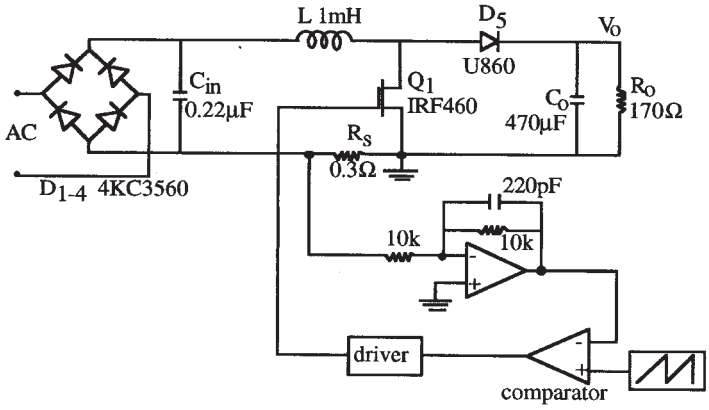


Fig. 11. Experimental setup.

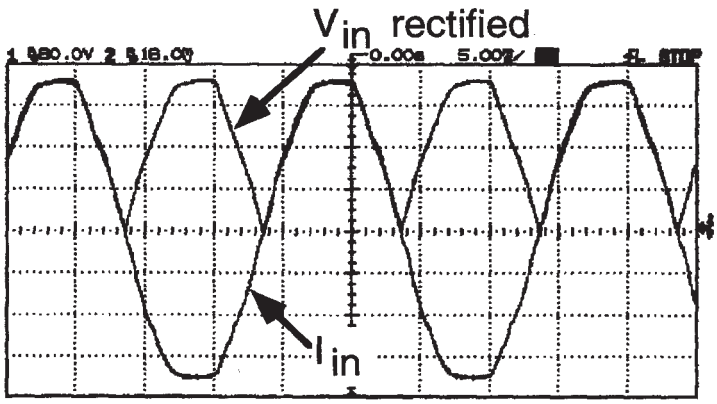
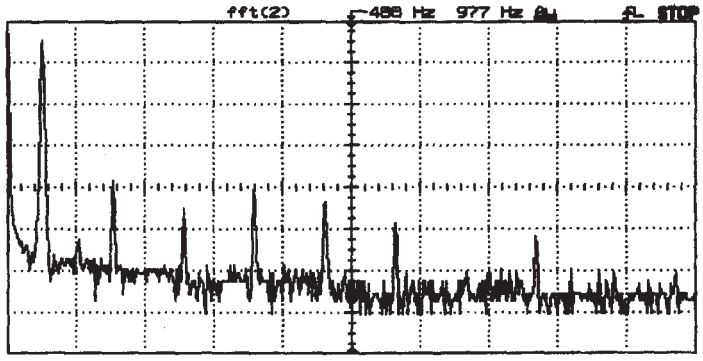
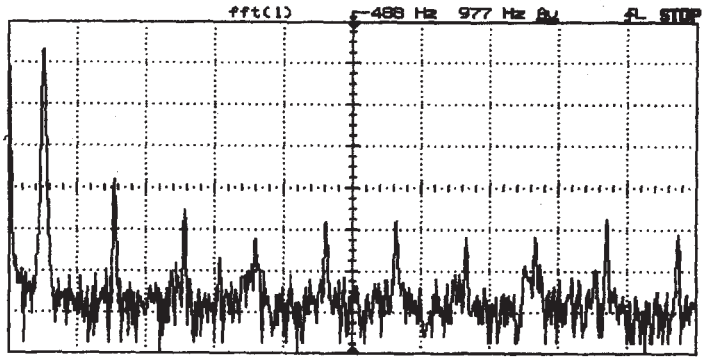


Fig. 12. Rectified line voltage and input current of experimental circuit (Fig. 11) for 1-kW power level. Vertical scale: 80 V/div and 1.6 A/div. Horizontal scale: 5 ms/div.



(a)



(b)

Fig. 13. Fast Fourier transform of (a) line voltage and (b) input current. Vertical scale: 10 dB/div. Horizontal scale: 97.6 Hz/div.

voltage (Fig. 12). The spectra of the input voltage and input current [Fig. 13(a) and (b)] suggest that the tracking introduces only minor excess THD.

V. Discussion

To further explore the salient differences between the proposed approach and the "classical" CCM implementation, we compare the two when represented by control-type block diagrams (Fig. 14). Only the parts associated with the current tracking are depicted. In each case, there would be a need for an outer loop amplifier to keep the output voltage constant

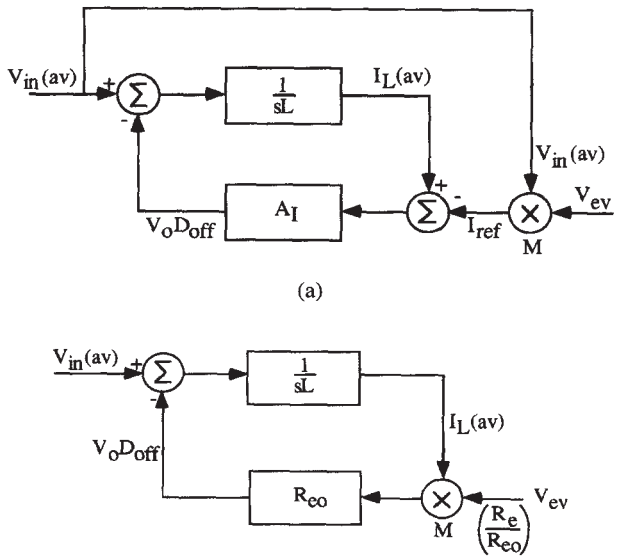


Fig. 14. Block diagram of (a) conventional and (b) proposed power-factor-correction control.

under variable operating conditions. The output of that error amplifier (V_{ev}) is used to drive the inner current loop. The two block diagrams are approximate. Both assume that the output voltage has no ripple component. We will also neglect here the ripple on V_{ev} and possible feedforward circuits [16], [17].

In the conventional control scheme shown in Fig. 14(a), we recognize an inner current loop and a multiplier that generates the reference to the inner loop. The feedback loop is composed of two parts: the inductor which sees two opposing voltages, $V_{\text{in}}(\text{av})$ and $V_o D_{\text{off}}$ [13], [14], and a current error amplifier A_I. The latter is taken to include the modulator transfer function, sensing resistor, etc. The drive signal of this inner loop is a reference current I_{ref} which is generated by multiplying the rectified input voltage by the output of the outer loop error amplifier (V_{ev}). On the other hand, the proposed control scheme uses the input voltage $V_{\text{in}}(\text{av})$ as the excitation signal of the inner current loop [Fig. 14(b)]. In this case, the output of the outer loop operational amplifier (V_{ev}) modulates the effective input resistance (R_e). Nominal value is assumed to be R_{e0} and for any other operating condition V_{ev} will change the input resistance so as to keep V_o at the desired level. For the conventional control scheme [Fig. 14(a)], $V_{\text{in}}(\text{av})$ is, in fact, a disturbance. However, due to the high loop gain provided by A_I, which is built around an operational amplifier, the conventional current loop can suppress this disturbance, as well as that caused by the output ripple. In the proposed control scheme [Fig. 14(b)], the magnitude of loop gain is evidently smaller (5), but if the interaction between the inductor L and output capacitor are taken into account [see (12) and Fig. 6], one finds that the increase in the loop gain due to the passive components is rather significant. As it happens, a practical value of L and C_o will have a resonant frequency around the low frequency range. A theoretical analysis of this question is beyond the scope of this paper, but examination of practical examples clearly shows that the resonant range is as pointed out. For example, a normal engineering choice is 1 mF for a

1-kW APFC, while the inductor will be in the range 0.5–1 mH for this power range (depending on the switching frequency). This will result in a resonant frequency of 160 Hz. Damping will move the resonant frequency somewhat, but, still, it is expected to be in the right range.

The high loop gain due to the passive resonant phenomena explains the excellent tracking and the rejection of the disturbance due to the output ripple. In the conventional case, the rejection is due to the high loop gain provided by A_I [Fig. 14(a)], but the high gain of the operational amplifier plus the extra phase shifts of the phase compensation network may deteriorate the phase margin. Furthermore, the introduction of a very-high-gain operational amplifier may render the system sensitive to switching noise. In light of the above, it appears that the lack of an operational amplifier in the inner current loop may not be a deficiency, but, rather, an advantage.

VI. Conclusions

The results of this paper suggest that the proposed control scheme yields a stable control system and provides good tracking of the input current. The inner loop gain of the system is well behaved and should not pose instability problems. The expected and actually measured bandwidth of current tracking should suffice in most, if not all, practical applications. It was further shown that the effect of output ripple is really minor from the practical point of view. It would, thus, appear that the proposed current programming scheme has all desirable characteristics required for implementing APFC.

The actual closed (outer loop) realization of the proposed control scheme could follow that of Fig. 3(a) or can be realized without an analog multiplier [6], [11]. The difference between the two may be insignificant if implemented by microelectronics technology.

The intuitive reasoning, theoretical analysis, simulation, and experimental results of this paper seem to indicate that the proposed control scheme is useful and practical. Some questions are still open, concerning operation in DCM, the need and implication of a feedforward path [16], [17], and optimal realization of the complete controller.

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