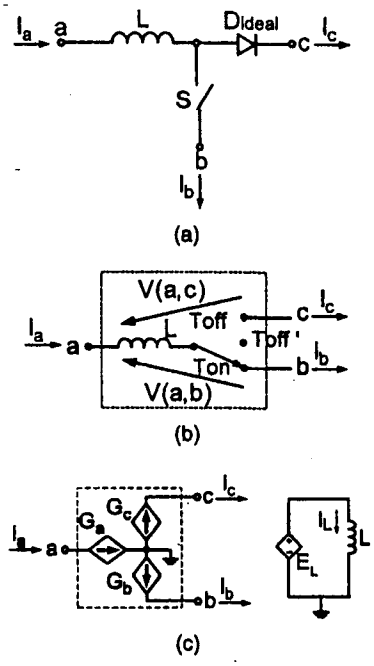

Fig. 1. Average simulation method. (a) Switched inductor in PWM topologies. (b) Switched inductor assembly. (c) GSIM [1–6].

Generalized Switched Inductor Model (GSIM): Accounting for Conduction Losses

The method of average modeling and simulation of pulsewidth modulation (PWM) converters is extended to include conduction losses. The method covers losses due to the inductor's resistance and due to the voltage drops across the switch and the diode. The method is demonstrated by considering an average model that is applicable to both current conduction mode (CCM) and discontinuous conduction mode (DCM) operations, and the switching from one to the other is automatic. The large-signal model is SPICE compatible and as such can be used to run dc (steady state), TRAN (large signal, time domain) and ac (small signal, frequency domain) analyses.

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INTRODUCTION

As previously shown [1–6], classical pulsewidth modulation (PWM) converters share a common, topology independent switching module: a switched inductor (Fig. 1(a)). Although normally realized by a switch and a steering diode, the switching action with ideal diode can be described by a toggle switch which alternately connects one end of the inductor to two terminals b and c (Figs. 1(a),(b)). A generic switched inductor model (GSIM) which includes three dependent current sources (Fig. 1(c)) was used to describe the interaction of the switched inductor module with the interface circuitry. The dependent sources of the GSIM represent the average terminal currents of the switched inductor assembly [1–6].

Alternative equivalent circuit oriented average models of PWM converters were proposed by many investigators (for a survey of the early history see Vincent Bello's website: http://members.aol.com/drvgb/). Vorperian's switch models for continuous current mode (CCM) and discontinuous conduction mode (DCM) [7, 8] were recently modified by Chen and Ngo [9, 10] while in [11] the GSIM [5] and the switch model [7, 8]

where combined into a model that is claimed to be efficient for simulation of large systems. However, all circuit oriented average models presented hitherto, failed to accurately account for conduction losses. At best, some studies suggest inserting the resistance of the switch or diode in the relevant branch [6, 8, 9]. This, however, is a poor approximation (in DCM) since it assumes that the conduction losses are caused by the average current in the branch rather then the rms current passing through the parasitic element. Furthermore, none of the previously published models took into account the actual voltage drop of the transistor or diode when carrying the pulsed inductor current.

The objective of this study was to expand the averaging methodology to include, in a more accurate way, the conduction losses due to the inductor's resistance, the voltage drops across the switch and diode. The approach is demonstrated by considering the GSIM method in which the suggested modification is easy to implement. This is due to the fact that, 1) the same equivalent circuit is used for both CCM and DCM as well as for peak current mode (PCM) and average current mode (ACM) control and, 2) that the running values of the inductor current and of D_{off}, required for calculating the conduction losses, are available in the GSIM block. Nonetheless, the proposed method is general and can be implemented in any average modeling scheme.

II. THE BASIC GSIM WITH NO LOSSES

The GSIM topology-independent equivalent circuit is developed by considering the average voltage across the inductor V_L. Examination of Figs. 1(b), (c) reveals that V_L is a function of the average voltage across the terminals $V_{(a,b)}$, $V_{(a,c)}$ and the time that the switch is in the ON (T_{ON}) and OFF (T_{OFF}) positions:

$$E_L \equiv V_L = \frac{V_{(a,b)}T_{\text{on}} + V_{(a,c)}T_{\text{off}}}{T_s} = V_{(a,b)}D_{\text{on}} + V_{(a,c)}D_{\text{off}} \tag{1}$$

where T_s is the period of the switching cycle, $D_{\text{on}} = T_{\text{on}}/T_s$, $D_{\text{off}} = T_{\text{off}}/T_s$. Equation (1) is correct under the assumption that the voltages $V_{(a,b)}$ and $V_{(a,c)}$ can be considered constant over a switching cycle. The effect of pulsed voltage drops in the physical circuit is treated in detail in the next sections.

The average voltage impressed on the inductor will develop the corresponding average current. Once the current is available, the dependent current sources of the GSIM model (Fig. 1(c)) can be readily defined by considering the way by which the current is split between the terminals. Since the current of terminal (a) is identical to the inductor current (I_{Lav})

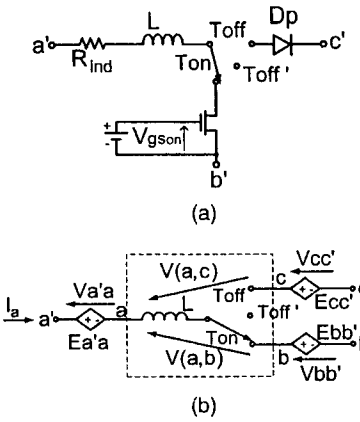

Fig. 2. Proposed modeling steps. (a) Switched inductor in PWM topologies with conduction losses. (b) Generalized model of switched inductor assembly.

the dependent current source G_a can be defined as

$$G_a \equiv I_{Lav}. \tag{2}$$

The current is then divided between terminal (b) and (c) (Figs. 1(b), (c)) according to the fraction of time the inductor is connected to them, namely,

$$G_b \equiv \frac{I_{Lav}D_{\text{on}}}{D_{\text{on}} + D_{\text{off}}} \tag{3}$$

$$G_c \equiv \frac{I_{Lav}D_{\text{off}}}{D_{\text{on}} + D_{\text{off}}} \tag{4}$$

where in case of CCM (Fig. 2(a)):

$$D_{\text{on}} + D_{\text{off}} = 1 \tag{5}$$

and therefore:

$$D_{\text{off}} = 1 - D_{\text{on}}. \tag{6}$$

In the case of DCM: $D_{\text{off}} < 1 - D_{\text{on}}$. From geometrical consideration [2–4] the expression for D_{off} is

$$D_{\text{off}} = \frac{2I_{Lav}Lf_s}{V_{(a,b)}D_{\text{on}}} - D_{\text{on}}. \tag{7}$$

For the case of DCM the dependent current sources G_b and G_c (eqs. (3), (4)) are normalized by $(D_{\text{on}} + D_{\text{off}})$ in order to obtain the correct average current during the conduction intervals of the inductor: T_{on} and T_{off} [2–4].

The GSIM model can be made to automatically follow CCM-DCM changes by selecting D_{off} according to the rule:

$$D_{\text{off}} = \min\left\{(1 - D_{\text{on}}), \left(\frac{2I_{Lav}Lf_s}{V(a,b)D_{\text{on}}} - D_{\text{on}}\right)\right\} \tag{8}$$

where $f_s = 1/T_s$ – switching frequency.

In SPICE implementation of the GSIM, analog behavioral dependent sources are used to emulate E_L, G_a, G_b, and G_c. Further, since SPICE recognizes time dependent variables which are either voltage or currents, D_{on} and D_{off} are coded into voltage.

The minimum function (8) is recognized as a valid expression by most modern circuit simulators. Consequently, the simulation model will automatically follow a CCM to DCM change by selecting the correct D_{off} for each case. Another important feature of the GSIM is that it can be used as-is to run dc (steady state), TRAN (large signal, time domain) and ac (small signal, frequency domain) analyses. The latter is due to the fact that the GSIM is formulated as SPICE compatible large-signal model that is automatically linearized by the simulator before running the ac analysis. No further derivations are needed beyond the formulation of the large signal model.

III. THE GSIM WITH LOSSES

The circuit of Fig. 2(a) represents the problem on hand.[1] It shows that the basic switched inductor assembly includes additional elements: the resistance of the inductor, the voltage drop of the transistor and the voltage drop across the diode. These effects can be taken into account by adding the additional voltage drops to the original port's voltages (a', b', c' in Fig. 2(a)). However, care should be taken to account for the fact that the voltage drops are, in general, not a function of the average current that is passing through a given port, but rather to the average current during the time that the inductor is connected to a given port. For example, the model should take into account the fact that when the inductor is connected to the transistor (Fig. 2(a)), the relevant voltage drop is a function of the average voltage drop across the transistor during the T_{on} time. This fine detail is especially important in DCM that may be characterized by a high current during T_{on} but having a low average current (when computed over T_s). It follows then that additional dependent sources: $E_{a'a}$, $E_{bb'}$, and $E_{cc'}$ (Fig. 2(b)) that account for the parasitic voltage drops need to be formulated in term of the added voltage seen by the inductor when connected to a given port. Under these conditions, the average voltage across the inductor (V_L) is

$$V_L = \{V(a',b') - V(a'a) - V(bb')\}D_{on} + \{V(a',c') - V(a'a) - V(c',c)\}D_{off}. \quad (9)$$

The method used to derive the expressions for $E_{a'a}$, $E_{bb'}$, and $E_{cc'}$ is explained with reference to Fig. 3. Here we distinguish between the average inductor current (I_{Lav}), which is averaged over T_{on}, and I_{Ls}, the average current during the conducing interval $T_{on} + T_{off}$ (Fig. 3). From basic geometrical considerations we find

$$I_{Ls} = \frac{I_{Lav}}{D_{on} + D_{off}}. \quad (10)$$

[1]See the Appendix for the effect of the filter capacitors' ESR.

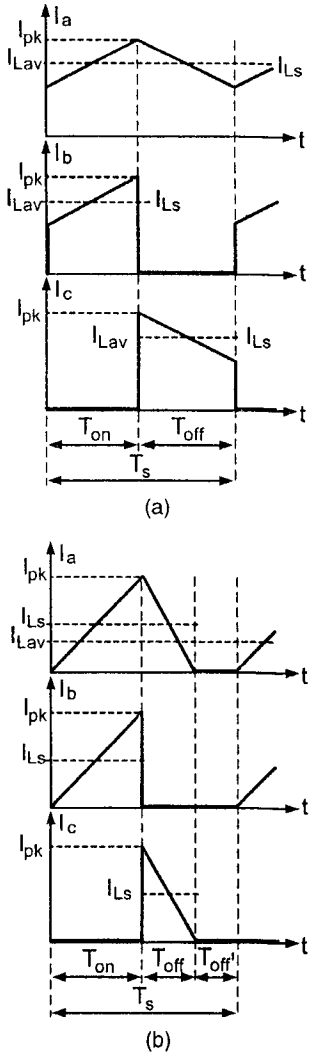

Fig. 3. Waveforms of terminal currents of switched inductor assembly. (a) Under CCM. (b) Under DCM.

In the private case of CCM (Fig. 3(a)):

$$I_{Ls} = I_{Lav}. \quad (11)$$

Based on the above we can now define dependent voltage sources that will emulate the parasitic voltage drops:

$$E_{a'a} \equiv V_{a'a} = I_{Ls} * R_{ind} \quad (12)$$

$$E_{bb'} \equiv V_{bb'} = V(\text{Switch\_Model})@I_{Ls} \quad (13)$$

$$E_{cc'} \equiv V_{cc'} = V(\text{Diode\_Model})@I_{Ls} \quad (14)$$

where $V(\text{Switch\_Model})@I_{Ls}$ and $V(\text{Diode\_Model})@I_{Ls}$ are the actual voltage drops across the transistor and diode, respectively, when the current I_{Ls} is passing through them.

These voltage sources account for the real voltage drops that are caused by the actual current flowing through the parasitic elements: inductor's resistance, transistor and diode voltage drops. By this method we can expand the generalized model (Fig. 1(c)) to include the effect of conduction losses. The approach

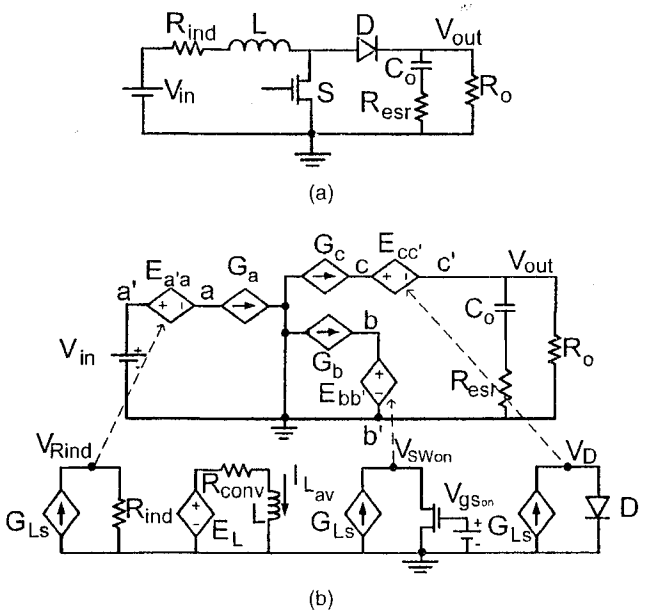

Fig. 4. Simulation circuit. (a) Benchmark circuit used to demonstrate proposed simulation approach. (b) SPICE compatible average model for benchmark circuit. See text for definition of behavioral dependent sources.

takes into account the physical characteristics of the elements by applying the SPICE models of the actual switch (MOSFET, IGBT, etc.) and diode and by calculating the voltage drops for each instance of the simulation. In the absent of SPICE model, one can use linear models to take into account the resistances and voltage offset (if any) of the elements. It should be noted that except for the added voltage sources $E_{a'a}$, $E_{bb'}$, and $E_{cc'}$, the model is identical to the original GSIM (Fig. 1(c)).

IV. SPICE IMPLEMENTATION

The proposed generalized model can be used to develop input files for general purpose electronic circuit simulator which includes algebraic behavioral models. To simulate a given topology, the model has to be placed in the corresponding orientation.

The proposed model is demonstrated by considering a Boost converter with practical parasitic losses R_{ind}, D, and S (Fig. 4(a)). The power stage is reduced to SPICE-compatible circuit (Fig. 4(b)) by applying the generalized model (Fig. 2(b)). The dependent voltage sources $E_{a'a}$, $E_{bb'}$, and $E_{cc'}$ duplicate the voltage drops V_{ind}, V_{SWon}, and V_D, respectively. These voltage drops are generated on "the fly" during the simulation by passing the I_{Ls} current (calculated each instance by the dependent current source G_{Ls}) via the models of the diode and switch. Consequently, the voltage drops represent the actual voltage that the inductor will see as it connects to the corresponding elements. The definition of the dependent sources are as given above. R_{conv} is a small resistor placed to prevent a short at dc (when the simulator shorts the inductor during the evaluation of the bias point). Missing in Fig. 4(b) is the voltage junction that represents D_{on} and D_{off} [5, 6]. D_{on} is the primary drive that can be generated by an independent voltage source (for open loop simulation) or a function of the output voltage of the error amplifier for close loop simulation [2–4]. Simulation can be carried out for voltage mode control or current mode control (average or peak) by applying the proper duty cycle generator (DCG) [5, 6].

V. LOSS CALCULATIONS

The comparison of the conduction losses in the physical circuit to the ones calculated by the model can be approached two ways. On the one hand one can argue that since the model imposes the correct terminal voltages on the switched inductor (Fig. 1), the resulting average current is calculated correctly. Another approach would be to compare the power dissipated by the parasitic elements, in the switched circuit, to the one calculated by the model. This comparison will be made under the general approximation of the present model that neglects the ripple component. That is, it is assumed that the pulsed current at terminals (b), (c) (in CCM and DCM) and (a) (in DCM) are rectangular. It can be shown that in the worst case (DCM and a resistive element) the error is 8% of the estimated loss.

Under this rectangular approximation, the power dissipated in the physical circuit by a resistive element (R_{ind}) in the inductor branch $\{P(R_{\text{ind}})\}$ is

$$P(R_{\text{ind}}) = \{(I_{Ls})^2 * R_{\text{ind}}\} \cdot (D_{\text{on}} + D_{\text{off}}) \tag{15}$$

or

$$P(R_{\text{ind}}) = \{I_{Ls} * R_{\text{ind}}\} \cdot I_{Lav} \tag{16}$$

which is identical to the power dissipation calculated by the model. In CCM $I_{Ls} = I_{Lav}$ and hence the power dissipation is a function of the average inductor current—as expected under the "zero ripple" approximation.

For an element EL in the (b) or (c) branches (Fig. 1), in which the current of the switched circuit is pulsating, the power dissipated by the element $\{P(EL)\}$ will be equal to the voltage drop of the element while conducting the inductor current $\{V(EL)@I_{Ls}\}$, multiplied by the inductor current and averaged out on the duty cycle of the branch (D_b):

$$P(EL) = V(EL)@I_{Ls} \cdot I_{Ls} \cdot D_b. \tag{17}$$

In the average model, the power dissipated by element EL will be the voltage drop of the $E_{b'b}$ or $E_{c'c}$ source (Fig. 2), that is $\{V(EL)@I_{Ls}\}$, times the average current of the branch $\{I_{Ls} \cdot D_b\}$. Hence, the power dissipated in the average model is identical

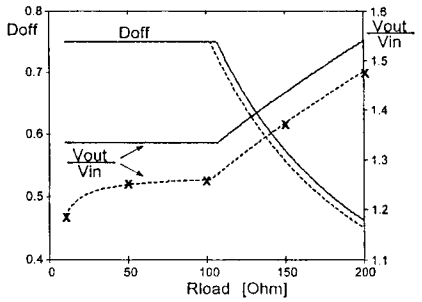

Fig. 5. DC transfer function and D_{off} of lossless converter (solid line) and lossy converter (dashed line) verified against cycle-by-cycle simulation results (crosses).

to the power dissipated by the EL element in the switched circuit (17).

It should be pointed out though, that the loss estimates are for the model of the power stage itself and not for the auxiliary circuits (bottom part of Fig. 4(b)). The power dissipated in these subcircuits is not derived from the main power path and consequently they are irrelevant to power balance of the converter. The power dissipated by the $E_{a'a}$, $E_{bb'}$, and $E_{cc'}$ is derived from the primary source and will show up as an increase in the input current.

VI. SIMULATION RESULTS

The proposed generalized model (Fig. 4(b)) was verified against a time domain (cycle-by-cycle) simulation of the complete circuit. The small signal transfer function was evaluated in the cycle-by-cycle simulation by injecting the low frequency sinusoidal perturbation to the duty cycle (formed by a ramp and comparator), and measuring the amplitude and phase of the low frequency component at the output. The parameters of the converter were as follows: V_{in} = 10 V, D_{on} = 0.25, R_{ind} = 0.08 Ω, L = 75 μH, practical diode MUR405 (from Orcad Version 9 library), C_o = 220 μF, R_{esr} = 0.07 Ω and switching frequency f_s = 100 KHz. In these runs, the transistor model was replaced by an ideal switch in series with a resistor (R_{SWon} = 1 Ω) rather than a SPICE model as shown in Fig. 4(b). This demonstrates the versatility of the model that can either apply full SPICE models or piecewise linear models. It also eliminates the effect of the transistor's nonlinearity and some of the switching losses (that are not treated in the proposed average mode). To further reduce the switching losses—that might introduce an element of uncertainty in the comparison between the average model and time domain simulation—the Orcad model of the diode (MUR405) was modified to reduce the reverse recovery to minimum. This was done by setting the transition time parameter (tt) to zero.

The solid line in Fig. 5 shows the DC transfer function V_{out}/V_{in} and D_{off} as a function of the value of the load resistance R_{load}—under continuous and discontinuous operating conditions of the ideal converter. For the converter with conduction losses, a very good agreement between the proposed generalized model (Fig. 5, dashed line) and the cycle-by-cycle simulation results (depicted by X) is observed over the whole load range.

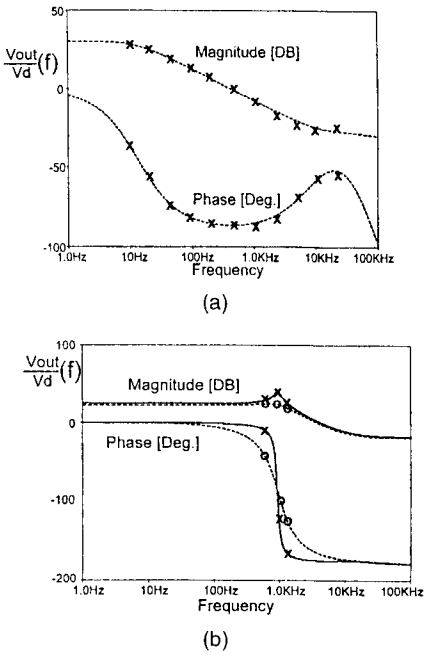

Fig. 6. Small signal output-voltage to duty-cycle transfer function of Boost converter (Fig. 4). (a) Under DCM. (b) Under CCM. Solid lines: ideal converter. Dashed lines: lossy converter. Discrete points (crosses and circles): results of cycle-by-cycle simulation.

The power loss agreement attempt was made to reduce the switching losses. Losses between the switched and average circuit also showed up in the input current of the primary voltage source (V_{in}). The average input currents were practically identical in the two circuits.

The open loop, small signal, transfer functions between duty cycle and output voltage $V_{out}/V_d(f)$ (Fig. 6) were obtained by running two sets of simulations: for DCM and CCM . The resulting Bode plots of $V_{out}/V_d(f)$ and phase under deep DCM condition (R_{load} = 200 Ω,) are shown in Fig. 6(a), and under CCM condition (R_{load} = 10 Ω) in Fig. 6(b). The solid lines in Fig. 6 represent the transfer functions of the lossless converter and the dashed lines are for the converter with parasitic losses. Crosses and circles mark the cycle-by-cycle simulation results. Excellent agreement is observed between the simulation results obtained by the proposed generalized model (lines) and the cycle-by-cycle simulation results over most of the frequency range. The discrepancy at high frequency reflects the inaccuracy of the average modeling method when the frequency of the modulated signal approaches the switching frequency.

VII. CONCLUSIONS

The modified GSIM methodology presented here can be used to estimate conduction losses, large signal response and the real small signal transfer functions that take into account the damping effect of the losses. The method provides an estimate of the power dissipation of the inductor, switch and diode caused by conduction losses. By taking the ratio of output to input power the efficiency (associated with conduction losses) can be also easily obtained. These could help to optimize the design of switch mode systems. The proposed model handles the problems of conduction losses and completely neglects switching losses. The latter might be more important than conduction losses in practical circuits. Further, the model assumes an equivalent average current through the devices and neglects the nonlinearity of their V-A curves. More research is clearly needed to combine other losses and nonlinear effects into the average models.

APPENDIX. ACCOUNTING FOR THE ESR OF FILTER CAPACITORS

In many modern power electronics systems the effect of the filter capacitors' equivalent series resistance (ESR) on the basic response of a switched mode converter [7] is small. Nonetheless, in cases that the ESR effect is not negligible, it can be easily combined in the proposed conduction loss model by applying the methodology described above.

The possible effect of the capacitors' ESR is encountered in several cases. In the case of Boost topology (Fig. 7(a)) the output network is connected to terminal (c) and the ESR will cause a pulsating voltage at the output [7]. In the Buck topology (Fig. 7(b)) the input filter is connected to terminal (b) and consequently, the voltage across an input filter capacitor with ESR will be pulsating. In the case of the Buck-Boost converter (Fig. 7(c)), both the input and output voltage will be pulsating. These effects can be taken into account (Fig. 8) by adding the additional voltage drops E_{ec} and E_{eb} to the original port's voltages b', c' in Fig. 2(b).

From basic geometrical considerations we find (for both CCM and DCM):

$$E_{ec} \equiv V_{ec} = I_{Ls} * (1 - D_{\text{off}}) * r_{e_c} \tag{18}$$

$$E_{eb} \equiv V_{eb} = I_{Ls} * (1 - D_{\text{on}}) * r_{e_b} \tag{19}$$

where r_{e_c} and r_{e_b} are the resistance seen between terminal (c) to ground and terminal (b) to ground, respectively, at infinite frequency (Fig. 7).

For example, in case of a Boost converter (Fig. 7(a)) the resistance of r_{e_c} is equal to R_{esr} in parallel to R_{o}.

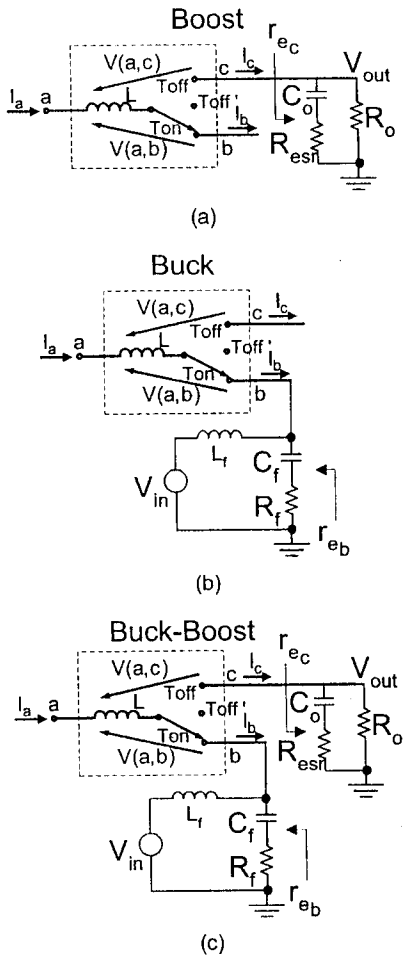

Fig. 7. Filter capacitors' ESR in basic PWM configurations. (a) Boost. (b) Buck. (c) Buck-Boost.

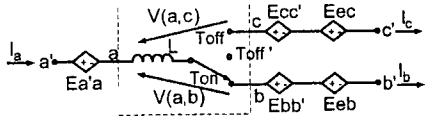

Fig. 8. GSIM including effect of filter capacitors' ESR.

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