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TOWARD A PLUG-AND-PLAY APPROACH FOR ACTIVE POWER FACTOR CORRECTION

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The feasibility of producing a modular Active Power Factor Correction (APFC) system was studied analytically and experimentally. It is shown that the novel control scheme that does not need the sensing of the input voltage is highly compatible with the modular, plug-and-play concept. Modularity is achieved by aggregating practically all the electronics in an IC or hybrid unit that may also include the power switch. This unit plus a line rectifier, inductor and bus capacitor are all that it takes to form an APFC system. It is demonstrated that dynamic stability is assured by the proposed inherent robust control method. This plug-and-play solution will greatly simplify and reduce the cost of the design and manufacturing of APFC front ends.

Keywords: Power factor; plug-and-play; modular approach; smart power.

1. Introduction

In recent years, power electronic technology is following the trend of system integration in which a large part of the circuit is included in a microelectronic chip or module. Modern integrated units (such as the TopSwitch of Power Integration Inc.) include not only the controller circuitry but also the drivers and power switches. These "Smart Power" devices significantly reduce the effort associated with designing and compensating control loops, placement of the external devices on the PCB, eliminating some of the "ground loops" problems, etc.

Ideally, one would like to have all the electronics in one unit such that, by adding few power passive elements, one will be able to construct a complete converter system in a "plug-and-play" manner, that is, without the need for special power electronics expertise. It would be advantageous, in particular, if the "plug-and-play"

solution will relieve the user from the need to redesign the control loop for, say, different power levels. Clearly, this goal cannot be achieved by simply packaging conventional converter circuitry into a module or an IC chip.

New control techniques and possibly new converter technologies will have to be developed before the "plug-and-play" solutions in power electronics can be realized. This study explores the possibility of achieving very high level of integration in Active Power Factor Correction (APFC) front ends operating in Continuous Current Conduction Mode (CCM).

Conventional embodiment of CCM APFC systems[1] includes a controller that senses the input voltage and the line current (Fig. 1). The shape of a rectified power line voltage, obtained via a divider comprised of resistors R_1 and R_2 from the input voltage V_{in}, is used as the reference for the desired shape of the input current. The controller also receives a signal that is proportional to the input current. The current level is adjusted for any given load by monitoring output voltage V_{out} via a divider comprised of resistors R_3 and R_4, and by multiplying the reference signal of the current control loop by the deviation from the desired output voltage level, so as to trim the effective reference signal to the load.

A major drawback of the conventional implementation of the CCM APFC is the need for sensing the input voltage, namely the line voltage after rectification. Due to the switching effects, the input voltage is normally noisy and is susceptible to interference pick-up that may distort the reference signal and hence the input current. Also, the extra pin required for input voltage sensing will increase the number of pins of a modular device built in the conventional APFC scheme. Furthermore as experience engineers learned the hard way, designing an APFC system around a conventional controller is no easy task. Making the inner (current) loop stable is tricky and fighting the ground loops is exhausting.

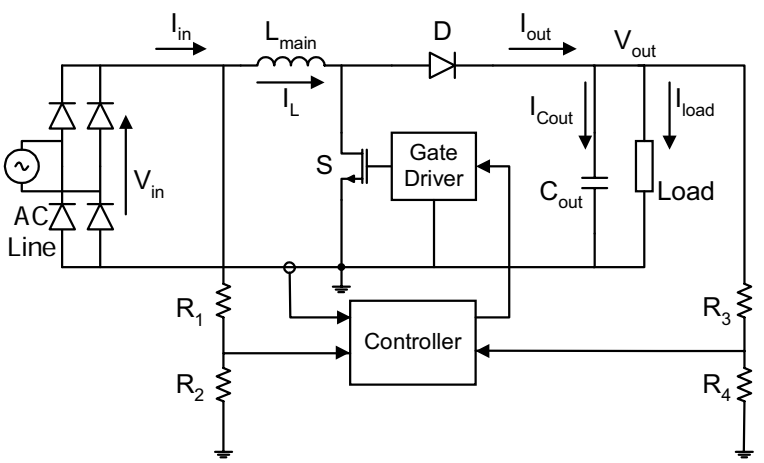


Fig. 1. Conventional CCM APFC approach.

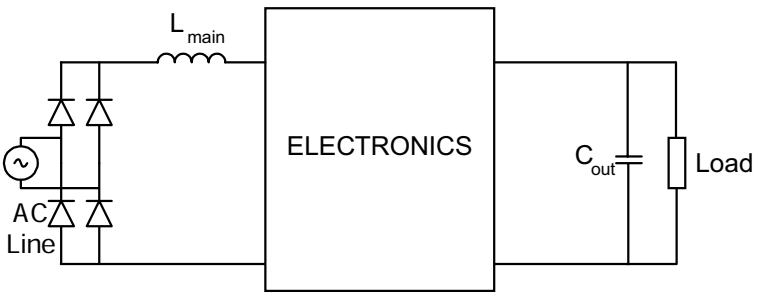


Fig. 2. Modular APFC approach.

An alternative solution for APFC control is to operate a Boost topology in Discontinuous Conduction Mode (DCM). In this case the input current of the converter will follow the average input voltage — when the power stage is driven by a constant duty cycle during the power line period.[2,3] Consequently sensing of the input voltage in such cases is not required. Unfortunately, the high ripple of the inductor current limits the application the DCM to low power. It is generally recognized that CCM mode of operation is the practical solution for medium and high power levels. Other solutions utilizing "voltage follower" approach in different topologies[4] are also restricted to low power levels only.

In this study we explored the possibility of utilizing the APFC control method to realize a modular design for a CCM power stage in which all the electronics is packaged together in an IC or module (Fig. 2).

2. The Control Concept

Since the analysis of the control concept has been published earlier[5–7] we repeat here, for the sake of brevity, only the essentials. The proposed APFC method is based on the Boost topology operating in the CCM. The system (Fig. 3) includes a power stage and a control scheme that senses the input current and produces a D_{off} duty cycle proportional to the average value of this current. The outer loop is used to trim the proportionality constant (between the input current and D_{off}) to accommodate any given load. The principle of operation can be understood by considering the average model of Fig. 4 that represents the power stage (Fig. 4(a)) and its average model (Fig. 4(b)) according to Refs. 8 and 9.

Assuming that the circuit is stable (as will be shown below), this implies (Fig. 4(b)):

$$V_{\text{in}}(av) = D_{\text{off}} V_o(av)\,, \tag{1}$$

where D_{off} is $(1 - D_{\text{on}})$, D_{on} is the duty cycle, $V_{\text{in}}(av)$ is the average input voltage and $V_o(av)$ is the average output voltage. Averaging is over one switching cycle under the assumption that the switching frequency is much higher than the bandwidth of V_{in} and of V_o.

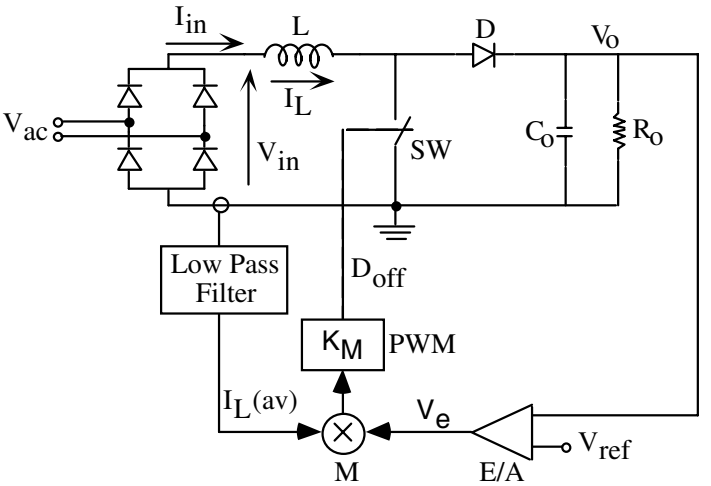


Fig. 3. Implementation of an APFC control scheme with no sensing of input voltage.

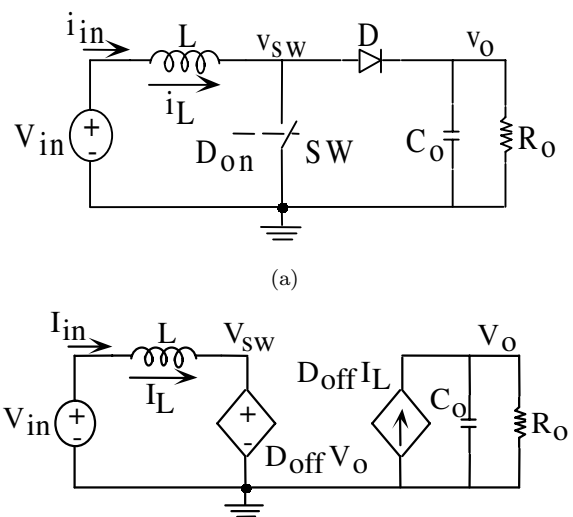


Fig. 4. (a) The boost converter and (b) its behavioral average model (after Refs. 8 and 9).

Since the average input current $I_{\text{in}}(av)$ is equal to the average inductor current $I_L(av)$, Eq. (1) can be manipulated to the form

$$\frac{V_{\text{in}}(av)}{I_{\text{in}}(av)} = \frac{D_{\text{off}} V_o(av)}{I_L(av)} \,. \tag{2}$$

To make the input resistive with an effective input resistance R_e, we require

$$\frac{V_{\text{in}}(av)}{I_{\text{in}}(av)} = R_e = \frac{D_{\text{off}} V_o(av)}{I_L(av)}\,, \tag{3}$$

that is, a resistive input will be observed if D_{off} is programmed according to the rule

$$D_{\text{off}} = \left(\frac{R_e}{V_o(av)}\right) I_L(av)\,, \quad 0 < D_{\text{off}} < 1\,. \tag{4}$$

The stability of the circuit can be appreciated by considering the simplified block diagram of Fig. 5.

In this control scheme the voltage imposed on the inductor (V_L) is equal to the input voltage minus the average voltage at the switch (Fig. 4(b)). The summing junction reconstructs the total voltage imposed on the inductor (L) while the feedback path represents the D_{off} programming according to Eq. (4). This block diagram representation assumes that the output voltage (V_o) is constant with negligible ripple and that R_e is set to a given constant value. Under these conditions, the system (Fig. 4) is linear and the loop-gain (βA) is found to be

$$\beta A = (R_e)\left(\frac{1}{sL}\right) = \frac{R_e}{sL}\,, \tag{5}$$

which represents a bandwidth of $R_e/2\pi L$ and a phase margin of 90°. This implies that the "inner" current feedback loop is unconditionally stable for any input or output voltages — under the assumption that V_o is constant. But as the more analysis given below shows, this conclusion is also valid for practical cases.

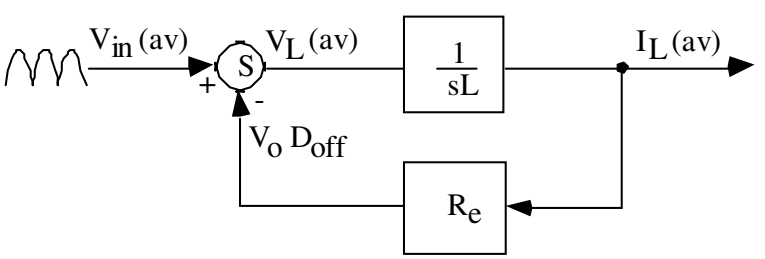


Fig. 5. Simplified block diagram of current control loop.

The closed loop response (input current as a function of input voltage) is clearly

$$\frac{I_L(av)}{V_{\text{in}}(av)} = \frac{1}{R_e}\frac{1}{1+s(L/R_e)}\,, \tag{6}$$

where $I_L(av)$ and $V_{\text{in}}(av)$ are the low frequency component of the inductor (and input) current and the low frequency component of the input voltage, respectively. This result implies that the tracking bandwidth is $R_e/2\pi L$ as would be expected from Eq. (5).

In practical APFC applications for 50/60 Hz power line, the tracking bandwidth ($BW_{I_{\text{in}}}$) should be at least 1 kHz[10] or, in general

$$\frac{R_e}{2\pi L} = BW_{I_{\text{in}}}\,. \tag{7}$$

This constraint can now be checked against other design considerations and in particular the size of the inductor required to keep the current ripple within reasonable limits. Maximum ripple is reached at $D_{\text{on}} = 0.5$ that is when $V_{\text{in}}(av) = 1/2V_o(av)$. The ripple ($\Delta I$) at this point will be

$$(\Delta I)_{D_{\text{on}}=0.5} = \frac{V_{\text{in}}(av)}{2f_sL}\,, \tag{8}$$

where f_s is the switching frequency. The ripple ratio ($\Delta I/I_{\text{in}}(av)$) will be

$$\left(\frac{\Delta I}{I_{\text{in}}(av)}\right)_{D_{\text{on}}=0.5} = \frac{(V_{\text{in}}(av)/2f_sL)}{(V_{\text{in}}(av)/R_e)} = \frac{R_e}{2f_sL}\,. \tag{9}$$

Combining Eqs. (7) and (9) we obtain

$$\left(\frac{\Delta I}{I_{\text{in}}(av)}\right)_{D_{\text{on}}=0.5} = \frac{\pi}{f_s}(BW_{I_{\text{in}}}) \tag{10}$$

or

$$(BW_{I_{\text{in}}}) = \frac{1}{\pi}f_s\left(\frac{\Delta I}{I_{\text{in}}(av)}\right)_{D_{\text{on}}=0.5}\,, \tag{11}$$

which implies that for a design of say $(\Delta I/I_{\text{in}}(av))_{D_{\text{on}}=0.5} = 0.1$ (that is, maximum current ripple is 10% of the nominal current value), the tracking bandwidth will be about $f_s/30$. This is obviously more than enough for modern switch mode systems in which $f_s > 50$ kHz. For higher ripple ratios the bandwidth will be even larger.

The dynamics of the proposed control scheme was thoroughly studied earlier.[7] It was found that the expression for the inner (current) loop is

$$\beta A = \frac{sC_oR_oR_e + R_e + D_{\text{off}}^2R_o}{s^2LC_oR_o + sLR + D_{\text{off}}^2R_o}\,, \tag{12}$$

and for practical values ($C_o = 1$ mF; $L = 1$ mH, $R_o = 140\ \Omega$) it is well behaved (Fig. 6).

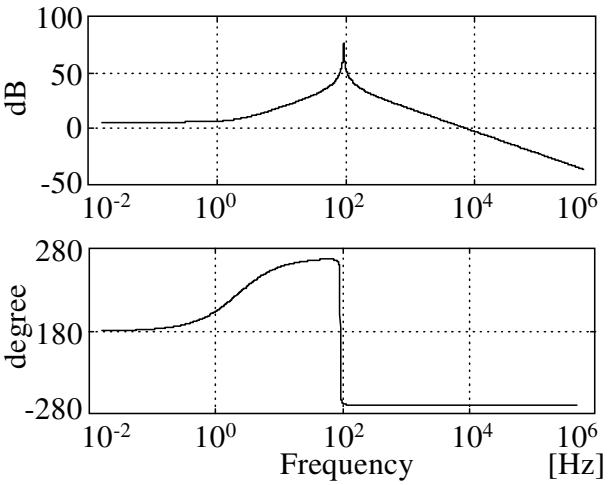


Fig. 6. Loop gain of the current control loop.

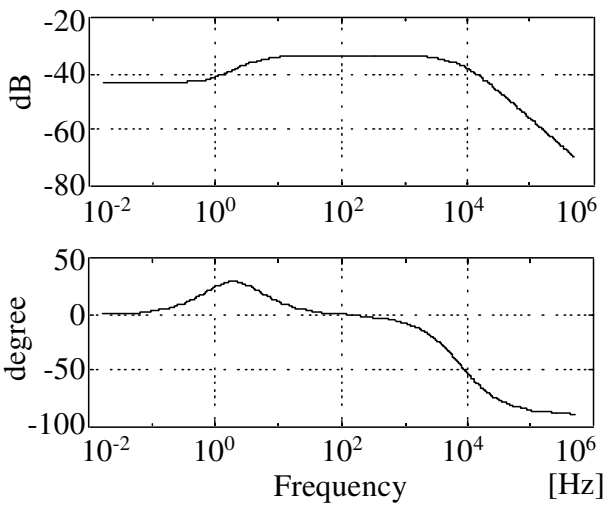


Fig. 7. Transfer function of the current control loop.

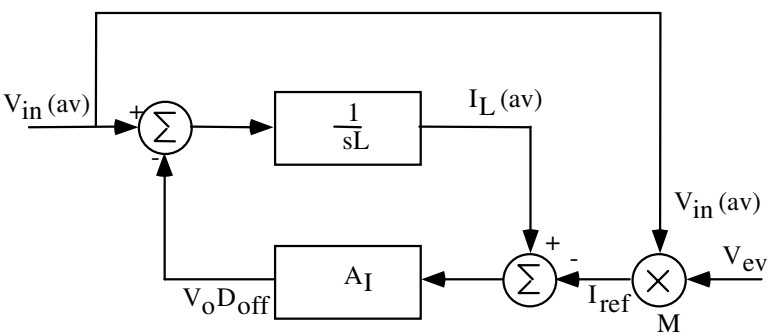
Consequently, good current tracking is obtained over the required frequency range (Fig. 7).

To further explore the salient differences between the proposed approach and the "classical" CCM implementation we compare the two when represented by control-type block diagrams (Fig. 8). Only the parts associated with the current tracking are depicted. In each case there would be a need for an outer loop amplifier to keep the output voltage constant under variable operating conditions. The output of that error amplifier (V_{ev}) is used to drive the inner current loop. The two block diagrams

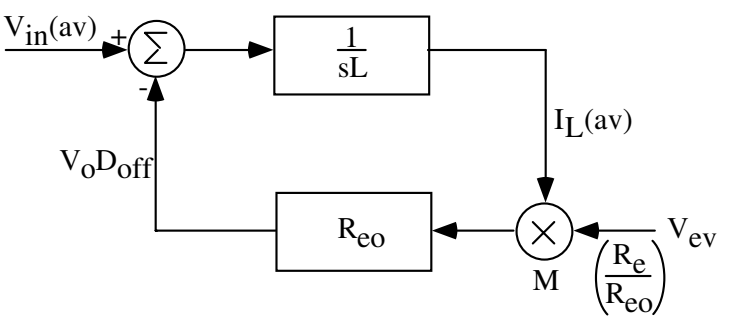
are approximate. Both assume that the output voltage has no ripple component. We will also neglect here the ripple on V_{ev} and possible feedforward circuits.[11,12]

In the conventional control scheme shown in Fig. 8(a), we recognize an inner current loop and a multiplier M that generates the reference to the inner loop. The feedback loop is composed of two parts: the inductor that sees two opposing voltages, $V_{\text{in}}(av)$ and $V_o D_{\text{off}}$[8,9] and a current error amplifier A_I. The latter is taken to include the modulator transfer function, sensing resistor and amplifier gain. The drive signal of this inner loop is a reference current I_{ref} which is generated by multiplying the rectified input voltage by the output of the outer loop error amplifier (V_{ev}).

On the other hand, the proposed control scheme uses the input voltage $V_{\text{in}}(av)$ as the excitation signal of the inner current loop (Fig. 8(b)). In this case, the output of the outer loop operational amplifier (V_{ev}) modulates the effective input resistance (R_e). Nominal value is assumed to be R_{eo} and for any other operating condition V_{ev} will change the input resistance so as to keep V_o at the desired level. For the conventional control scheme (Fig. 8(a)) $V_{\text{in}}(av)$ is in fact a disturbance.



(a)



(b)

Fig. 8. Block diagrams of (a) a conventional and (b) proposed power factor correction control.

However, due to the high loop gain provided by A_I, which is built around an operational amplifier, the conventional current loop can suppress this disturbance as well as that caused by the output ripple. In the proposed control scheme (Fig. 8(b)), the magnitude of loop gain is evidently smaller (Eq. (6)), but if the interaction between the inductor L and output capacitor C_o is taken into account (Fig. 6) one finds that the increase in the loop gain due to the passive components is rather significant. As it happens, practical values of L and C_o will have a resonant frequency around the low frequency range. A theoretical analysis of this question is beyond the scope of this paper.

But examination of practical examples clearly shows that the resonant range is as pointed out. For example, a normal engineering choice is 1 mF for a 1 kW APFC while the inductor will be in the range 0.5 mH to 1 mH for this power range (depending on the switching frequency). This will result in resonant frequency of 160 Hz.

Damping will move the resonant frequency but it is somewhat still expected to be in the right range.

The high loop gain due to the passive resonant phenomena explains the excellent tracking and the rejection of the disturbance due to the output ripple. In the conventional case, the rejection is due to the high loop gain provided by A_I (Fig. 8(a)). But the high gain of the operational amplifier plus the extra phase shifts of the phase compensation network may deteriorate the phase margin. Furthermore, the introduction of a very high gain operational amplifier may render the system sensitive to switching noise. In the light of the above, it appears that the lack of an operational amplifier in the inner current loop is a significant advantage.

3. The Plug-and-Play Approach

The main obstacle in using the conventional CCM APFC control scheme of Fig. 1 for the modular plug-and-play approach is the large number of pins required for proper operation of the controller. Indeed, in addition to output voltage and input current sensing terminals one has to allow external connections for input voltage sense and compensation network of a current control loop.

In the proposed control scheme, however, no sensing of the input voltage is required. This eliminates the interferences due to the noise that is typically found in conventional AFC approaches and reduces the number of external pins in the controller.

Moreover, as was shown above (Eqs. (5) and (12)) the proposed current control loop is unconditionally stable with tracking bandwidth of Eq. (7). As can be realized from inspection of the R_e/L term in Eq. (7) the proposed current control loop has a natural scaling capability, that is, in practice one would choose L to be proportional to R_e (the equivalent input resistance that defines the power level) and hence the loop gain will be the same for APFC stages designed for different power levels. This implies that there is no need to trim the phase compensation

of the inner loop for each power level design. Consequently, the compensation network can be utilized inside the controller since no connection terminals for external compensation network are required anymore.

It should be pointed out that the proposed control law (1) provides also an inherent current limiting capability stemming from the fact that a high input current will automatically increase D_{off}.

Based on these advantages the design of a universal controller that will fit any power level with minimum external pins is possible as shown on Fig. 9(a). An APFC system built around such a controller is sketched on Fig. 9(b). The time constant of a compensation capacitor C_{comp}, plus associated voltage divider R_1, R_2, should be chosen so as to filter out a low frequency ripple, coming from the output of the converter's — as normally required in every APFC stage.

Combining the proposed controller together with a power switch in one package will result in a Self Containing Unit (SCU) (Fig. 10(a)). Since SCU requires only few external pins it can be packaged in a very standard five pins TO-220 or TO-247 package providing a low cost solution while integrated in APFC system (Fig. 10(b)).

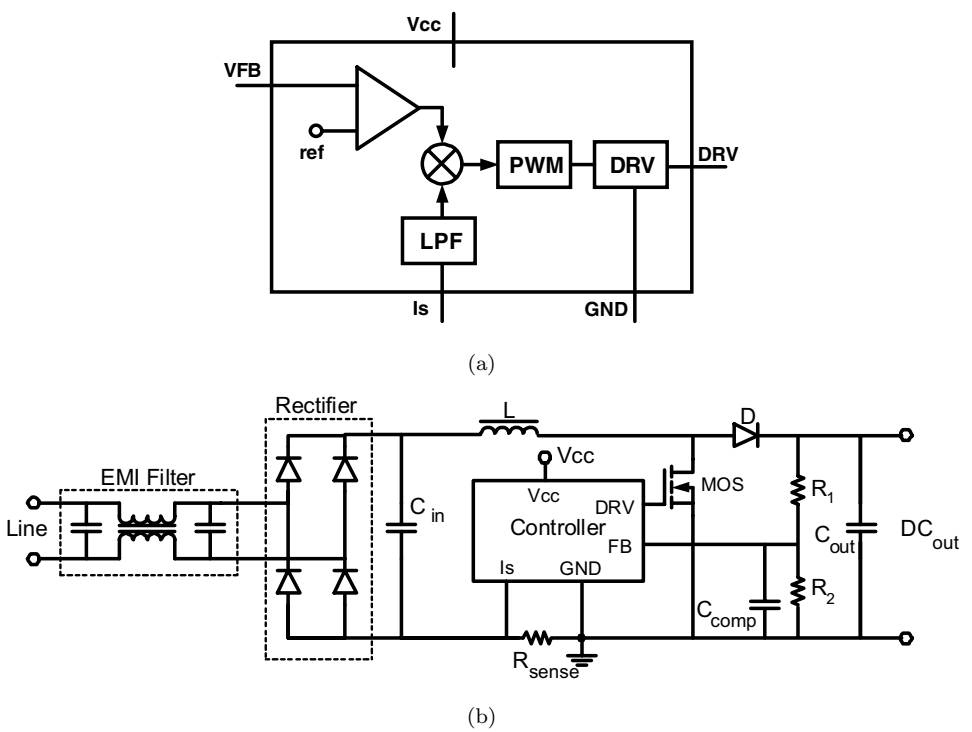


Fig. 9. Implementation of proposed control scheme in a "discrete" form. (a) A proposed controller and (b) APFC stage built around it.

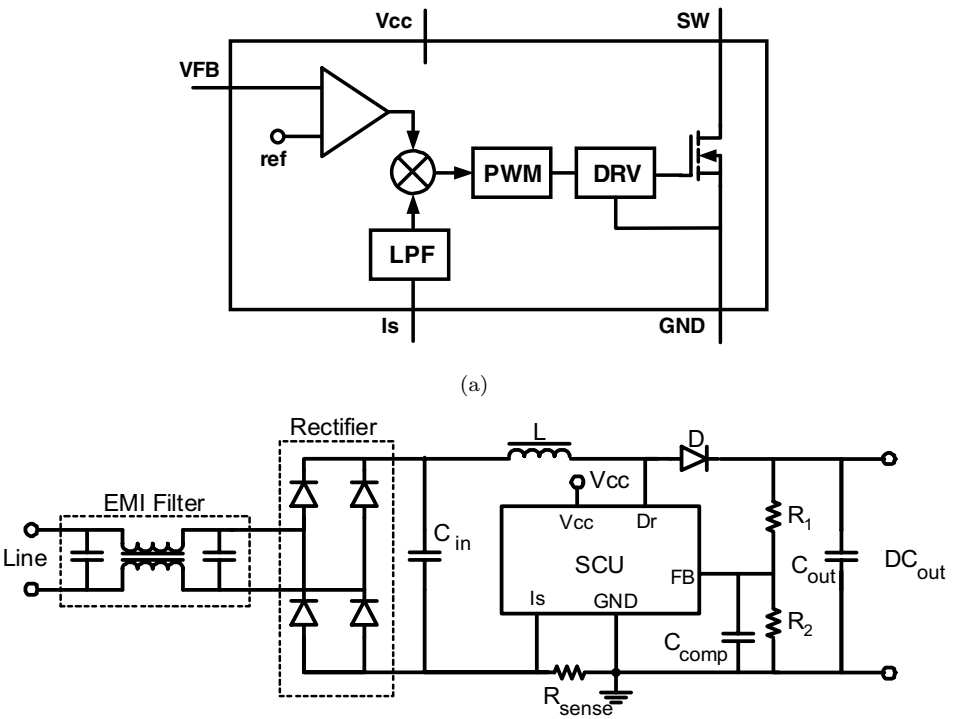


Fig. 10. Implementation of proposed control scheme in an IC form. (a) Self Contained Unit and (b) APFC stage built around it.

4. Experimental

To explore the concept developed above, a prototype converter was built and tested in open and closed outer loop. The actual implementation (Fig. 11) included a PCB on which all the control components were placed. The tracking quality obtained experimentally is demonstrated by comparing the line current to the rectified input voltage (Fig. 12). The measured harmonics were low, easily complying with the EN61000-3-2 standard (Fig. 13).

5. Conclusions

The present study suggests that the "Smart Power" approach to APFC construction is feasible and it can lead to great simplification of APFC system design and integration — to a "plug-and-play" level. The analysis presented here shows that the proposed control law ensures adequate dynamic response and stability for any power level. For low power systems (up to about 250 W), the approach can lead to an APFC IC that will greatly simplify and reduce the cost of the APFC stage.

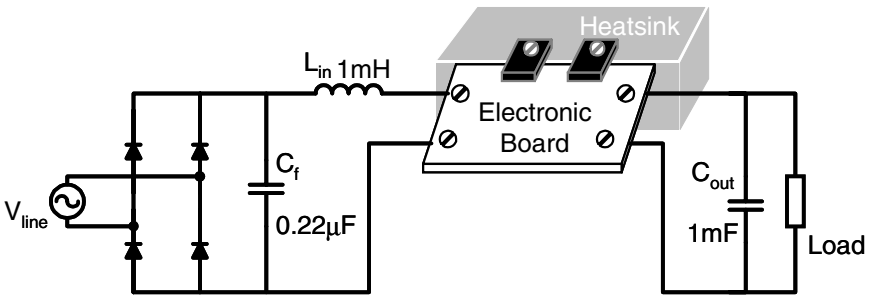


Fig. 11. Experimental set up (1 kW).

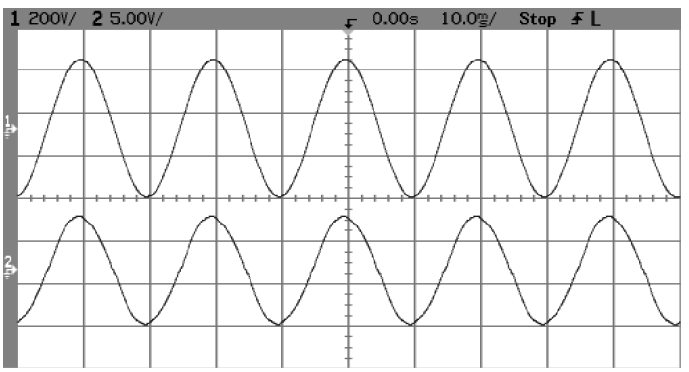


Fig. 12. Experimental results. Upper trace: line voltage (230 $V_{\rm rms}$). Lower trace: input current (5 A/div). Horizontal scale: 10 mS/div.

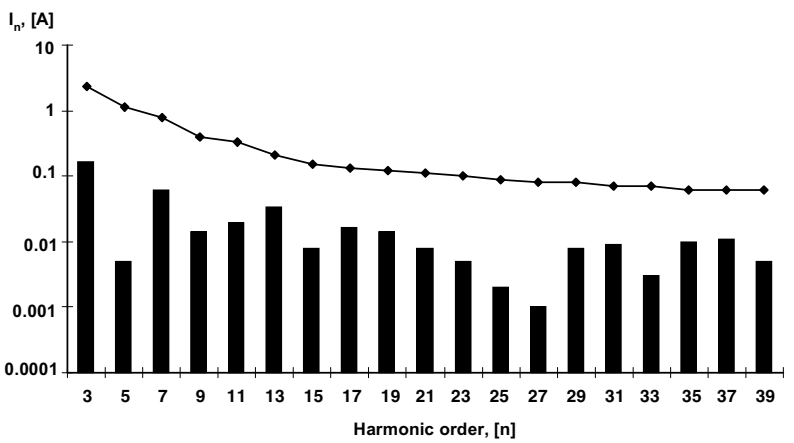
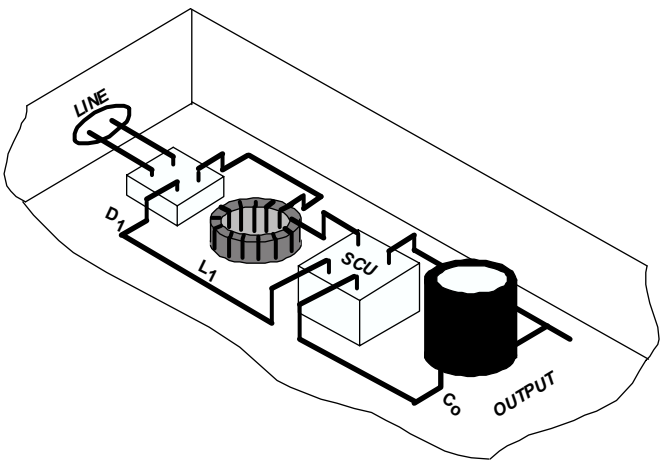


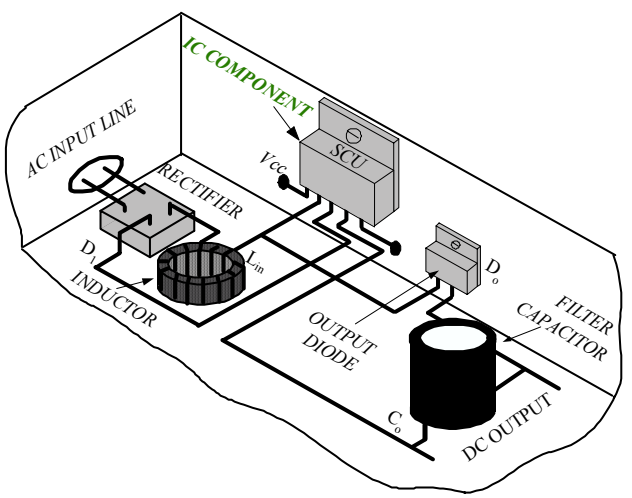
Fig. 13. Compliance with EN61000-3-2 standard at the 1 kW level. Line: standard limits. Bars: measured harmonics. Notice the logarithmic scale.

All that would be required is to add the passive power components: rectifier, small high frequency by pass capacitor, inductor, and bus capacitor.

An artist concept of possible implementations is shown in Fig. 14. An extra benefit of the proposed approach is the flexibility in the physical placement of the components in the system. For example, this is a result of the fact that the modular unit needs only two connections ports to function. Consequently, the one can thus conceive a line of devices that will cover the full power range of one-phase applications. Power electronic designers will surely welcome such devices.



(a)



(b)

Fig. 14. Modular implementation of proposed APFC technology. (a) Hybrid and (b) IC, monolithic or multichip.

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