Average-Current-Based Conduction Losses Model of Switched Capacitor Converters

Michael Evzelman, *Student Member, IEEE*, and Shmuel (Sam) Ben-Yaakov, *Fellow, IEEE*

***Abstract*—A generic modeling methodology that analyzes the losses in switched capacitor converters (SCC) operating in open loop was developed and verified by simulation and experiments. The proposed analytical approach is unified, covering both hard- and soft-SCC topologies that include active switches and/or diodes. An important feature of the proposed model is that it expresses the losses as a function of the average currents passing through each flying capacitor during each switching phase. Since these currents are linearly proportional to the output current, the model is also applicable to SCC with multiple capacitors if it can be assumed that each of the subcircuits of the modeled SCC can be described or approximated by a first-order system. The proposed model can be used to assess the effect of the operational conditions of the SCC, such as switching frequency and duty cycle, on the expected losses. As such, the model can help in the optimization of SCC systems and their control to achieve high efficiency and the desired regulations.**

***Index Terms*—Conduction losses, modeling, power converters, resonant converters, soft switching, switched capacitors converters (SCC).**

I. Introduction

SWITCHED capacitor converters (henceforth referred to as SCC for plural and singular) suffer from a fundamental power loss deficiency which makes their use in some applications prohibitive. Nonetheless, the SCC do have some noticeable advantages, such as the absence of magnetic components and very-large-scale integration compatibility that make their use in some applications preferable. The power loss has been traditionally explained as being due to the inherent energy dissipation when a capacitor is charged or discharged by a voltage source or another capacitor [1]–[4]. Two types of SCC have been considered in the literature, hard- and soft-SCC. The soft-SCC employs a small series inductor to achieve zero current switching [5]–[15]. Previous studies that analyze losses in SCC covered the hard switching case [1]–[4], [16]–[26], or the soft switching case [5], [11], [14]. A comparison between the two was carried out in [6] and [12] which applied the first harmonics approximation to analyze the soft switching case in a unity SCC converter. This paper presents a generic, scalable, and intuitive model that is applicable to both hard- and soft-SCC and a closed form solution is derived for the two cases. The major advantage of the model presented here is that it expresses, in a modular and expandable approach, the SCC losses as a function of the average current passing through each flying capacitor during each switching phase. Since these currents are linearly proportional to the output current, the individual losses of each subcircuit derived by the proposed model can be linearly added to obtain the total loss of complex topologies such as multicapacitors and multiphase SCC. The model is valid for cases where the subcircuits of the converter can be described or approximated by a first-order *RC* network. Furthermore, the model is applicable to SCC that include diodes since diode losses are also expressed as a function of average currents. The model could be used as a tool for the examination of new theoretical concepts, as a designer's aid [27], or as an educational tool for understanding the intricate loss mechanism in SCC and in capacitor charging and discharging in general [28]. An additional feature of the proposed model is its seamless compatibility with circuit simulation software packages. This is due to the fact that the model is developed in terms of average equivalent circuits rather than state space equations [20], [29]–[32].

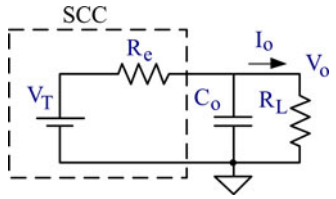

Fig. 1. SCC generic average equivalent circuit.

II. Model Derivation—the Concept

It has been previously shown that any SCC operating in open loop can be represented as a voltage source denoted as the target voltage V_T connected in series with an equivalent system resistance R_e that expresses the losses (see Fig. 1) [9], [12], [16]–[20]. This model is applicable to cases in which the charge and discharge of the flying capacitors can be represented by *RC* or *RLC* for the resonant SCC networks. This model does not apply to cases in which the flying capacitor(s) is charged by a current source to facilitate output voltage control [33]–[38]. The target voltage of the equivalent circuit (see Fig. 1) refers to the no-load output voltage of the converter and can be evaluated for a given switched capacitor converter by a set of algebraic equations. The equivalent resistance of the equivalent circuit, as developed further in this paper, expresses the conduction losses of the converter caused by the current that passes via the series resistances in the capacitors' charge/discharge paths. Switching

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The authors are with Power Electronics Laboratory, Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev, Beer-Sheva 84105, Israel (e-mail: evzelman@ee.bgu.ac.il; sby@ee.bgu.ac.il).

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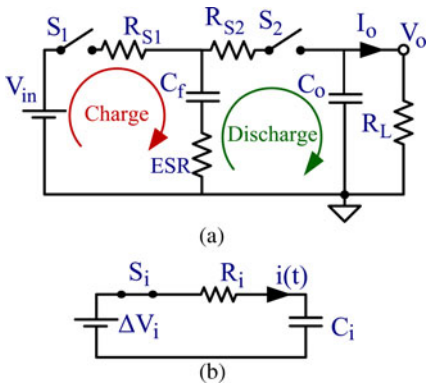

Fig. 2. Unity SCC and the basic charge/discharge RC subcircuit: (a) Unity SCC—switching circuit, (b) Basic and generic, instantaneous *RC* subcircuit.

losses [39], switch drive losses, losses due to stray capacitances [40], [41], and other parasitic losses, due, for example, to a shoot-through, are out of the scope of this paper, except for diode losses, which are considered and taken into account.

The derivation of proposed model is based on dividing the SCC into switching phases according to the operational modes. This division results in subcircuits, indexed i, for each operational phase. For example, in a simple unity converter [see Fig. 2(a)], there are two operating modes, the charge mode $i = 1$ and the second, discharge mode $i = 2$. Each of these charge/discharge processes can be represented by the basic, generic, instantaneous *RC* circuit of Fig. 2(b) (henceforth referred to as "the basic *RC* circuit"), in which ΔV_i is the initial voltage across the switch S_i just before closure, R_i is the total resistance of the loop (switch resistance R_{S_i} and capacitor's ESR) and C_i is the total capacitance of the loop. It should be pointed out that the currents in the basic *RC* circuit of Fig. 2(b) are instantaneous $i(t)$ and that the basic *RC* circuit is valid both for the charge and discharge processes when a capacitor is connected to a voltage source or to another capacitor. However, the basic *RC* circuit of Fig. 2(b) is valid only if the subcircuits can be represented, or approximated, by a first-order system. Such an approximation will be acceptable in the 1:1 SCC of Fig. 2(a) if $C_o \gg C_f$. The latter is universally assumed, albeit sometime implicitly, in previous SCC modeling approaches [4], [6], [42]. In the soft-SCC, additional component will appear such as the total inductance of the loop L_i.

Each of the switching phases which are represented by the corresponding subcircuits is responsible for a power loss, P_i, which is due to the power dissipated by the total subcircuit resistance, R_i, during the operating cycle of the subcircuit. This power loss of each subcircuit, P_i, can then be referenced to the output current, which serves as a common reference to all subcircuits' currents of the converter. This reflection to the output side is possible thanks to the fact that each subcircuits' average current is linearly proportional to the average output current [17]–[19]. It should be noted that the phrase "subcircuit's average current", which is also termed in this paper as "average subcircuit's capacitor current", or "capacitor average current" refers to the total charge transferred in the subcircuit to/from a capacitor during the switching period T_i, of phase, i,

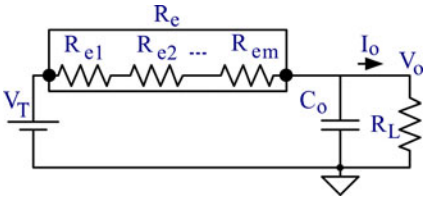

Fig. 3. SCC generic average equivalent circuit that shows the contribution of the partial subcircuits equivalent resistances R_{ei} to the total equivalent circuit R_e. (For the unity SCC example [see Fig. 2(a)], R_{e_1} is the loss contribution of charge subcircuit and R_{e_2} is the loss contribution of discharge subcircuit.)

divided by the total switching period T_s. Clearly, a given capacitor will be involved in at least two subcircuits such that it will be charged and discharged periodically by the subcircuits "capacitor's average currents" which will sum up to zero in steady-state condition [43], [44]. Applying the proportionality constants k_i that relate the average subcircuits' currents to the average output current [17]–[19], the losses of the subcircuits can be expressed as a function of the output current. This allows the representation of the losses in each subcircuit i as a partial equivalent resistance R_{e_i} which represents the contribution of the ith subcircuit to the total equivalent resistance of the converter (see Fig. 3). Repeating the independent calculations for each switching phase, these partial equivalent resistances for the "m" switching phases, $R_{e_1}, R_{e_2} ... R_{e_m}$, are found and connected in series to form the total equivalent resistance R_e, of the converter (see Fig. 3)

$$R_e = \sum_{i=1}^{m} (R_{e_i}). \tag{1}$$

Along with the switches and capacitors, SCC systems may include diodes [2], [8], [26], [31], [32], [45]–[50]. The extension of the SCC equivalent model to take into account the losses contributed by the diodes is based on the same concept as described earlier for the equivalent resistance. Namely, the loss of each diode in each subcircuit is calculated independently as a function of the average subcircuit's current in each switching phase. The losses are then expressed as a function of the output current via the proportionality coefficients k_i. As a result, the diodes' losses can be emulated by a voltage source V_D in series with R_e. This extension is further discussed and illustrated in Section VI.

The proposed modeling approach can handle a dual phase as well as multiphase SCC and is valid for asymmetrical switching duration of the subcircuits. It is assumed though that each of the subcircuits could be represented by a first-order *RC* circuit for the hard switching case and a simple, underdamped second-order *RLC* circuit for the soft switching case.

III. Equivalent Resistance Calculation: Hard Switching Case

The generic equivalent *RC* circuit of Fig. 2(b) represents each out of i operational phases of the hard-SCC. The energy loss E_{R_i} dissipated in the subcircuit's total resistance R_i as a result of charge/discharge current flow $i(t)$, during the time interval

T_i is calculated by integrating the instantaneous power $p(t) = i^2(t) \cdot R_i$ over the duration of T_i. The basic, first-order *RC* circuit of Fig. 2(b) has an exponential current waveform, and the integration result takes the form of the following equation:

$$E_{Ri} = \frac{\Delta V_i^2 \cdot C_i}{2} \cdot (1 - \mathrm{e}^{-2\beta_i}) \tag{2}$$

where $\beta_i = T_i/R_i\mathrm{C}_i$.

The charge q_i transferred during time interval T_i to/from a capacitor C_i is calculated to be

$$q_i = \Delta \mathrm{V}_i \cdot \mathrm{C}_i \cdot [1 - \mathrm{e}^{-\beta_i}] \tag{3}$$

The charge q_i transferred to/from a capacitor, during the subcircuit's operating time T_i, is used to define the "average subcircuit's capacitor current," $I_{C_{av_i}}$, during phase i (averaged over the total switching cycle $T_s = 1/f_s$)

$$I_{C_{av_i}} = \frac{q_i}{T_s} = q_i f_s. \tag{4}$$

Rearranging (3) and (4) to express the voltage difference ΔV_i as a function of average capacitor current during phase i, one finds

$$\Delta V_i = \frac{I_{C_{av_i}}}{f_s C_i \cdot [1 - e^{-\beta_i}]}. \tag{5}$$

Substituting (5) into (2) results in an expression for the energy dissipated in the *RC* subcircuit i, during the switching period T_i as a function of the average subcircuit's capacitor current $I_{C_{av_i}}$. From (2)–(5) we find

$$E_{R_i} = I_{C_{av_i}}^2 \cdot \frac{1}{f_s} \cdot \frac{1}{2 f_s C_i} \cdot \frac{(1 + e^{-\beta_i})}{(1 - e^{-\beta_i})}. \tag{6}$$

The power loss as a function of average subcircuit's capacitor current during phase i, of periodically charged or discharged *RC* subcircuit, with switching frequency f_s can now be evaluated as follows:

$$P_{R_i} = I_{C_{av_i}}^2 \cdot \frac{1}{2 f_s C_i} \cdot \frac{(1 + e^{-\beta_i})}{(1 - e^{-\beta_i})}. \tag{7}$$

The average subcircuit's capacitor current during phase i can be expressed as a function of the average output current I_o [17]–[19].

$$I_{C_{av_i}} = k_i \times I_o \tag{8}$$

where k_i is the proportionality factor that is calculated by KCL taking into account the charge balance equations for all of the SCC switching capacitors as exemplified and detailed in [16]–[19], (an additional example of the proportionality factor calculation is given in Chapter V section *C* that demonstrates the extension of the methodology to more complex cases).

From (8) and (7), the power loss of ith subcircuit could be expressed as a function of common reference, the average output current of the SCC (9)

$$P_{R_i} = I_o^2 \cdot \left[k_i^2 \cdot \frac{1}{2 f_s C_i} \cdot \coth\left(\frac{\beta_i}{2}\right) \right]. \tag{9}$$

The form of (9) resembles the classical expression for resistive power dissipation ($P = I^2 \cdot R$) and thus, the expression in brackets (9) represents an equivalent resistance. That is, expression (10) is the equivalent resistance, R_{e_i}, of the ith operational phase of the hard-SCC, as discussed in Part II

$$R_{e_i} = k_i^2 \cdot \frac{1}{2 f_s C_i} \cdot \coth\left(\frac{\beta_i}{2}\right). \tag{10}$$

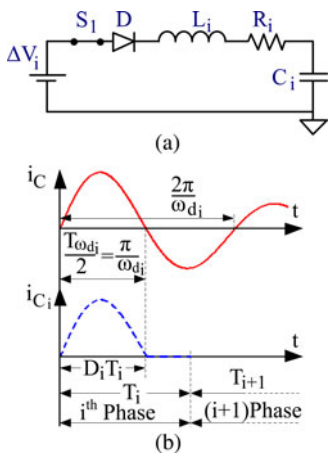

Fig. 4. Resonant charge/discharge process: (a) Basic and generic, instantaneous *RLC* circuit. (b) *Current waveforms*: straight (red) trace—resonant current waveform with no diode. Dashed (blue) trace—actual capacitor charging current waveform with blocking diode.

IV. Equivalent Resistance Calculation: Soft Switching Case

The generic charge/discharge subcircuit of the soft switching case is represented by the corresponding *RLC* circuit of Fig. 4(a). At this point, an ideal diode (zero forward voltage) is assumed while the impact of the diode forward voltage on the losses is detailed in Section VI. The energy loss E_{R_i} dissipated in the subcircuit's total resistance R_i as a result of charge/discharge current flow during the time interval T_i [see Fig. 4(b)] is calculated by integrating instantaneous power $p(t) = i^2(t) \cdot R_i$ during T_i. The generic second-order *RLC* circuit of Fig. 4(b) has a sinusoidal current waveform and the integration result is found to be

$$E_{Ri} = \frac{\Delta V_i^2 C_i}{2}(1 - e^{-2\pi \cdot \zeta_{d_i}})$$

$$\text{or} \qquad E_{Ri} = \frac{\Delta V_i^2 C_i}{2}\left(1 - e^{(-\pi/\mathrm{Q}_i)\sqrt{1 - \frac{1}{4\mathrm{Q}_i^2}}}\right) \tag{11}$$

where

$$\omega_{0i} = \frac{1}{\sqrt{L_i C_i}}, \quad Q_i = \frac{1}{R_i C_i \cdot \omega_{0_i}} = \frac{\omega_{0_i} \cdot L_i}{R_i}, \quad \alpha_i = \frac{R_i}{2L_i}$$

$$\omega_{d_i} = 2\pi \cdot f_{d_i} = \sqrt{\omega_{0_i}^2 - \alpha_i^2}, \ \zeta_{d_i} = \frac{\alpha_i}{\omega_{d_i}}. \tag{12}$$

It should be noted that (11) is valid for oscillatory *RLC* circuits, i.e., when the quality factor $Q_i > 1/2$. It is also assumed that the time interval T_i of the ith phase is always larger or equal to half the period of the damped resonant frequency of the basic *RLC* circuit, [i.e., $T_i \geq T_{\omega_{d_i}}/2$, where $T_{\omega_{d_i}}$ is the period of the damped resonant frequency and equals to

$T_{\omega_{d_i}} = 1/f_{d_i} = (2\pi)/\omega_{d_i}$ Fig. 4(b)], and that the ideal diode D [see Fig. 4(a)] blocks the reverse current [after $t = T_{\omega_{d_i}}/2$ Fig. 4(b)]. The charge q_i transferred during time interval T_i to/from a capacitor C_i is calculated to be

$$q_i = \Delta V_i \cdot C_i \cdot (1 + e^{-\pi \cdot \zeta_{d_i}}). \tag{13}$$

On the other hand, the transferred charge q_i is related to the average subcircuit's current (averaged over the total switching period $T_s = 1/f_s$),$I_{C_{av_i}}$ by

$$q_i = \frac{I_{C_{av_i}}}{f_s}. \tag{14}$$

Comparing (13) and (14), and solving for the voltage difference ΔV_i results in (15), which is a function of average subcircuit's capacitor current during the phase i

$$\Delta V_i = \frac{I_{C_{av_i}}}{f_s C_i \cdot (1 + e^{-\pi \cdot \zeta_{d_i}})}. \tag{15}$$

By substituting (15) into (11), the energy dissipated in an *RLC* subcircuit as a function of the average subcircuit's capacitor current is obtained.

From (13)–(15), the energy loss, as a function of average subcircuit's capacitor current is found to be

$$E_{R_i} = I^2_{C_{av_i}} \cdot \frac{1}{f_s} \cdot \frac{1}{2 f_s C_i} \cdot \frac{(1 - e^{-\pi \cdot \zeta_{d_i}})}{(1 + e^{-\pi \cdot \zeta_{d_i}})}. \tag{16}$$

The power loss as a function of the subcircuit's average capacitor current during phase i, of a periodically charged or discharged *RLC* subcircuit, with frequency f_s can therefore be expressed as follows:

$$P_{R_i} = I^2_{C_{av_i}} \cdot \frac{1}{2 f_s C_i} \cdot \frac{(1 - e^{-\pi \cdot \zeta_{d_i}})}{(1 + e^{-\pi \cdot \zeta_{d_i}})}. \tag{17}$$

It should be noted that (17) is correct for $T_i \geq T_{\omega_{d_i}}/2$. The optimal operating condition (lowest power dissipation) is when T_i equals half of the period of the damped resonant frequency of the basic *RLC* circuit, (i.e., $T_i = T_{\omega_{d_i}}/2$).

Applying the hyperbolic tangent function, (17) can be expressed as follows:

$$P_{R_i} = I_o^2 \cdot \left[k_i^2 \cdot \frac{1}{2 f_s C_i} \cdot \tanh\left(\frac{\pi \cdot \zeta_{d_i}}{2} \right) \right]. \tag{18}$$

This leads to the definition of the partial equivalent resistance R_{ei} of the soft-SCC due to the losses of subcircuit i, as discussed in Section II

$$R_{e_i} = k_i^2 \cdot \frac{1}{2 f_s C_i} \cdot \tanh\left(\frac{\pi \cdot \zeta_{d_i}}{2} \right). \tag{19}$$

Equation (19) can also be expressed in terms of ith *RLC* subcircuit quality factor Q_i

$$R_{e_i}(Q_i) = k_i^2 \cdot \frac{2Q_i^2 \cdot \pi \cdot R_i}{df_i \cdot \sqrt{4Q_i^2 - 1}} \cdot \tanh\left(\frac{\pi}{2\sqrt{4Q_i^2 - 1}} \right) \tag{20}$$

where df_i is the ratio of switching frequency to the ith *RLC* subcircuit damped resonant frequency

$$df_i = \frac{f_s}{f_{d_i}} = \frac{2\pi \cdot f_s \cdot R_i C_i}{2} \cdot \sqrt{4Q_i^2 - 1}. \tag{21}$$

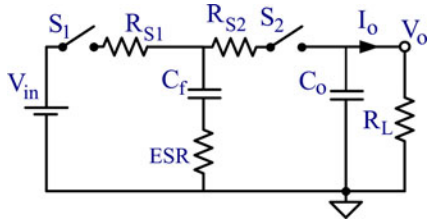

Fig. 5. Simple hard switched 1:1 SCC, switching circuit.

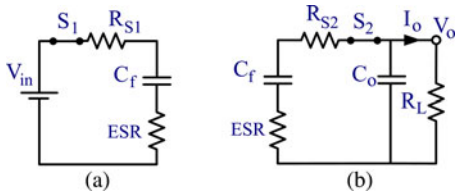

Fig. 6. Hard switched 1:1 SCC operation phases: (a) Charge. (b) Discharge.

Examination of the power loss in the hard and soft switching cases (9, 18) reveals that they both can be expressed as a resistor loss (10), (19), and (20), as shown in previous publications for the hard switching case [6], [12], [16]–[20]. The aforementioned analysis shows that the total equivalent resistance R_e, of the converter is in fact the sum of the partial equivalent resistances for "m" switching phases, $R_{e_1}, R_{e_2} \cdots R_{e_m}$, (1), (see Fig. 3). The value of the equivalent voltage source V_T often referred to as the "target voltage" of the converter is the open circuit voltage of the SCC, that is, the no load output voltage.

V. Examples

A. Unity Gain Hard-SCC

Model simplicity and its intuitive application are demonstrated by considering a 1:1 SCC. The analysis is carried out under the assumption that $R_{S1} = R_{S2} = R_S$. ESR$_o$ is assumed to be negligibly small, $C_o \gg C_f, T_{1,2} = 1/2 f_s$ and $C_o R_L \gg T_{1,2}$. It is further assumed that the SCC is in the steady state for which the proposed static model is relevant. The hard switched version of the SCC is first analyzed (see Fig. 5). The SCC is divided into two phases, charge phase $i = 1$ [see Fig. 6(a)] and discharge phase $i = 2$ [see Fig. 6(b)]. Each of the switching subcircuits presented in Fig. 6 is reduced to the basic charge/discharge *RC* circuit of Fig. 2(b), and R_i, C_i, k_i, and β_i are calculated for $i =$ 1,2

$$R_{1,2} = R_S + \text{ESR}; \qquad C_{1,2} = C_f$$
$$\beta_{1,2} = \frac{1}{2 f_s \cdot R_{1,2} C_{1,2}} = \frac{1}{2 f_s \cdot (R_S + \text{ESR}) \cdot C_f}. \tag{22}$$

The value of the proportionality constants k can be obtained by simple charge considerations. Under steady-state condition, the average subcircuit's capacitor current during the charge state is equal to the average subcircuit's capacitor current during the discharge state. Furthermore, the average subcircuit's capacitor current during discharge [see Fig. 6(b)] is equal to the average

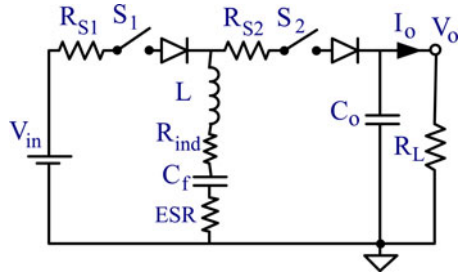

Fig. 7. Simple soft switched 1:1 SCC, switching circuit.

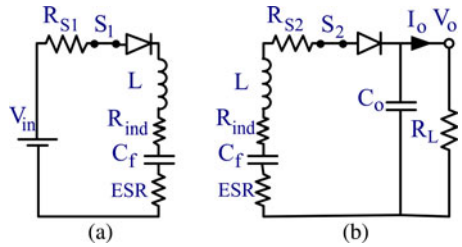

Fig. 8. Soft switched 1:1 SCC operation phases: (a) Charge. (b) Discharge.

output current. Consequently, all the average currents are equal and hence, $k_{1,2} = 1$.

Applying (10) R_{e_i} is calculated for $i = 1, 2$

$$R_{e_{1,2}(RC)} = \frac{1}{2f_s C_f} \cdot \coth\left(\frac{\beta_{1,2}}{2}\right). \tag{23}$$

And the total equivalent resistance for unity SCC according to (1) and Fig. 3 is

$$R_{e(RC)} = \frac{1}{f_s C_f} \cdot \coth\left(\frac{\beta}{2}\right); \quad \beta = \frac{1}{2f_s \cdot (R_S + \mathrm{ESR}) \cdot C_f}. \tag{24}$$

B. Unity Gain Soft-SCC

The soft-SCC case (see Fig. 7) is also analyzed by dividing it into two phases, the charge phase $i = 1$ [see Fig. 8(a)] and the discharge phase $i = 2$ [see Fig. 8(b)]. Each of the switching subcircuits presented in Fig. 8 is reduced to the simple charge/discharge *RLC* circuit of Fig. 4(a), and L_i, R_i, C_i, k_i, and Q_i are calculated for $i = 1, 2$

$$R_{1,2} = R_S + R_{\mathrm{ind}} + \mathrm{ESR};\ L_{1,2} = L;\ C_{1,2} = C_f;$$
$$Q_{1,2} = \frac{1}{(R_S + R_{\mathrm{ind}} + \mathrm{ESR})} \cdot \sqrt{\frac{L}{C_f}}. \tag{25}$$

Average subcircuit's currents relationship in soft switched converter is identical to the hard switched case and again $k_{1,2} = 1$. Applying (20), $\mathrm{R_{e_i}}$ is calculated for $i = 1, 2$

$$R_{e_{1,2}(\mathrm{RES})} = \frac{2Q_{1,2}^2 \cdot \pi \cdot R_{1,2}}{df_{1,2} \cdot \sqrt{4Q_{1,2}^2 - 1}} \cdot \tanh\left(\frac{\pi}{2\sqrt{4Q_{1,2}^2 - 1}}\right). \tag{26}$$

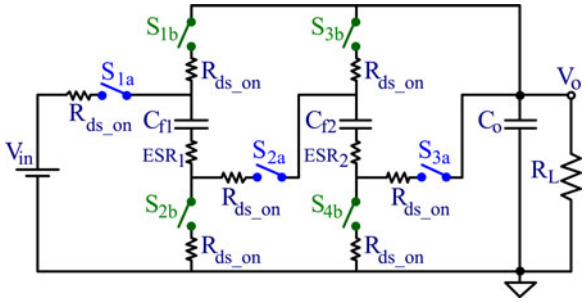

Fig. 9. Step down 3:1 SCC, switching circuit.

Hence, the total equivalent resistance for soft switched unity SCC according to (1) and Fig. 3 is

$$R_{e(\mathrm{RES})} = \frac{4Q_{1,2}^2 \cdot \pi \cdot R_{1,2}}{df_{1,2} \cdot \sqrt{4Q_{1,2}^2 - 1}} \cdot \tanh\left(\frac{\pi}{2\sqrt{4Q_{1,2}^2 - 1}}\right)$$
$$Q_{1,2} = \frac{1}{(R_S + R_{\mathrm{ind}} + \mathrm{ESR})}\sqrt{\frac{L}{C_f}}$$
$$df_{1,2} = \frac{2\pi \cdot f_s \cdot R_{1,2} C_f}{2}\sqrt{4Q_{1,2}^2 - 1}. \tag{27}$$

C. Step Down 3:1 Hard-SCC

The extension to higher order SCC is demonstrated by considering a step down 3:1 converter (see Fig. 9) [51] that includes two phases as shown in Fig. 10(a) and (b). It is assumed that the circuit is symmetrical, i.e., R_{ds_on} of all the switches are equal (denoted R_s), all the capacitances of flying capacitors are equal (denoted C) and their ESRs are also equal (denoted ESR). ESR_o is assumed to be negligibly small, $C_o \gg C_f$, and $C_o R_L \gg T_{1,2}$. Under these assumptions, serially connected capacitors of Fig. 10(a), and the parallel flying capacitor branches of Fig. 10(b) can be combined into a single capacitor and resistor assembly Fig. 10(c) and (d), respectively. This is because, the initial voltages of the parallel capacitors [see Fig. 10(b)] will be close to each other, since in the complimentary switching phase [see Fig. 10(a)] they are charged/discharged by the same current. The components of serial circuit of Fig. 10(a) therefore represented by a single capacitor $(C/2)$, single ESR resistor (2·ESR), and a single switch resistance $(3R_{ds\_\mathrm{on}})$, as shown in Fig. 10(c). The parallel branches of Fig. 10(b) therefore represented by one capacitor $(2C)$, one series resistor (ESR/2), and one switch resistor (R_{ds_on}) as shown in Fig. 10(d). These simplifications overcome the limitation of a first-order circuit per subcircuit for which the proposed model is valid. It should be noted that the circuits of Fig. 10(c) and (d) are further reduced to a basic *RC* subcircuit of Fig. 2(b) and for the matter of equivalent resistance calculation the total subcircuit resistances and capacitances are derived in (30) and (31). The k_i coefficients, which represent the ratio between the average subcircuit's current and the average output current at the steady state, are found by Kirchhoff's current law (KCL) and capacitor charge balance at the steady state, as described in [17], [19] and exemplified in [16] and [18]. It should be noted that the present analysis

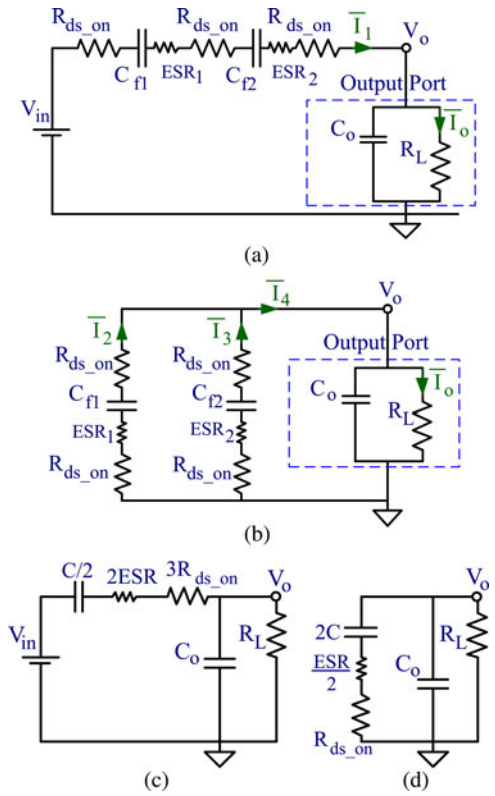

Fig. 10. Step down 3:1 SCC operation phases: (a) Phase 1. (b) Phase 2. (c) Simplified subcircuit of phase 1. (d) Order reduction of the subcircuit of phase 2. *Arrows*: average subcircuits currents.

follows the approach, applied throughout this study, by which the average current of each subcircuit is defined as the charge transferred in the subcircuit divided by the complete switching cycle period, T_s. The average subcircuits' currents, $\bar{I}_1 ... \bar{I}_4$, and the average output current, $\bar{I}_o$, which flows through the load resistor R_L are marked with arrows in Fig. 10. Matrix (28) summarizes the relationships between the currents. The two first rows are capacitors' C_{f1} and C_{f2} charge balance equalities, third row is the KCL equation of the network shown in Fig. 10(b), and the last, fourth row is the contribution of the two phases to the output current $\bar{I}_o$. It is worth mentioning here that the two subcircuits are sharing the output port [see Fig. 10(a) and (b)], and the charge transferred per switching cycle by the average currents $\bar{I}_1$ and $\bar{I}_4$ together to the output port, equals to the average output current

$$\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 0 & 1 & 1 & -1 \\ 1 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} \bar{I}_1 \\ \bar{I}_2 \\ \bar{I}_3 \\ \bar{I}_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \bar{I}_o \end{bmatrix}. \tag{28}$$

The average currents matrix equation (28) has a unique solution (29) for capacitors average charge/discharge currents I_i $(i = 1, 2, 3)$

$$\bar{I}_1 = \bar{I}_2 = \bar{I}_3 = \frac{1}{3}\bar{I}_o. \tag{29}$$

This implies that the ratio between the first subcircuit's current [see Fig. 10(c)] and the average output current is $k_1 = \bar{\bar{I}}_1/\bar{I}_o = 1/3$ [see Fig. 10(a) and (c)]. For the second subcircuit [see Fig. 10(d)] due to the merge of two capacitors, C_{f1} and C_{f2}, which carried $1/3 \cdot \bar{I}_o$ each, $\bar{I}_2$ and $\bar{I}_3$ [see Fig. 10(b) and (d)], $k_2 = \bar{I}_2/\bar{\bar{I}}_o + \bar{I}_3/\bar{\bar{I}}_o, k_2 = 2/3$. The total equivalent capacitances of the subcircuits for phases 1 and 2 are

$$C_1 = \frac{C \cdot C_o}{2 \cdot C_o + C}; \qquad C_2 = \frac{2 \cdot C_o \cdot C}{C_o + 2 \cdot C}. \tag{30}$$

The total resistances of the subcircuits are

$$R_1 = 3R_S + 2\text{ESR}; \qquad R_2 = R_S + \text{ESR}/2. \tag{31}$$

Defining T_1 and T_2 as the duration of the first and second phases, β_1 and β_2 are expressed as follows:

$$\beta_1 = \frac{T_1}{R_1 C_1} = \frac{T_1}{(3R_S + 2\text{ESR}) \cdot \left(\frac{C \cdot C_o}{2 \cdot C_o + C}\right)}$$
$$\beta_2 = \frac{T_2}{\left(R_S + \frac{\text{ESR}}{2}\right)} \cdot \left(\frac{2 \cdot C_o \cdot C}{C_o + 2 \cdot C}\right). \tag{32}$$

The partial equivalent resistances for each phase can thus be expressed as follows:

$$R_{e_1} = \left(\frac{1}{3}\right)^2 \cdot \frac{1}{2f_s^2 \cdot \left(\frac{C \cdot C_o}{2 \cdot C_o + C}\right)} \cdot \coth\left(\frac{\beta_1}{2}\right)$$
$$R_{e_2} = \left(\frac{2}{3}\right)^2 \cdot \frac{1}{2f_s^2 \cdot \left(\frac{2 \cdot C_o \cdot C}{C_o + 2 \cdot C}\right)} \cdot \coth\left(\frac{\beta_2}{2}\right) \tag{33}$$

and the total equivalent resistance of the converter is

$$R_e = \frac{1}{18 f_s C C_o}$$
$$\left[(2C_o + C) \cdot \coth\left(\frac{\beta_1}{2}\right) + 2\,(C_o + 2C) \cdot \coth\left(\frac{\beta_2}{2}\right)\right]. \tag{34}$$

For infinitely large output capacitor C_o, the output equivalent resistance R_e is reduced to

$$R_e = \frac{1}{9} \cdot \frac{1}{f_s C} \left\{\coth\left(\frac{\beta_1}{2}\right) + \coth\left(\frac{\beta_2}{2}\right)\right\} \tag{35}$$

where $\beta_1 = \frac{T_1}{C(1.5R_S + \text{ESR})}$; $\beta_2 = \frac{T_2}{C(2R_S + \text{ESR})}$.

Being a 3:1 step-down converter, the target voltage V_T is in this case: $V_T = V_{\text{in}} / 3$.

VI. Inclusion of Diode Losses

The extension of the SCC equivalent model to include the losses contributed by diodes is demonstrated by considering an inverting 1:1 SCC (see Fig. 11), which operates in two phases as shown in Fig. 12.

Each of the switching subcircuits of Fig. 12 is reduced to the basic charge/discharge *RC* circuit of Fig. 2(b) that includes a

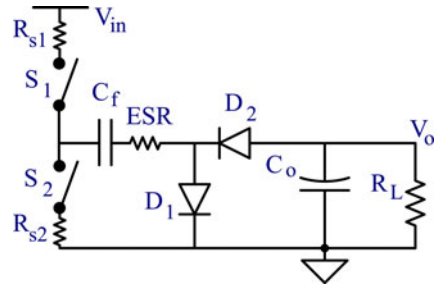

Fig. 11. Inverting 1:1 SCC, switching circuit.

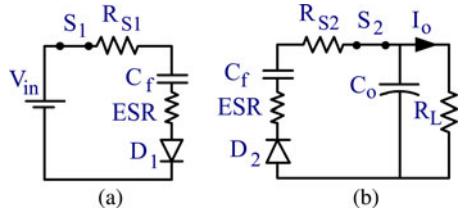

Fig. 12. Hard switched inverting 1:1 SCC operational phases: (a) Charge. (b) Discharge.

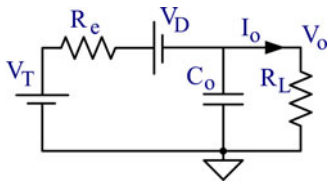

Fig. 13. SCC generic average equivalent circuit including diode losses.

diode, and R_i, C_i, k_i, and β_i are calculated for $i = 1{,}2$ to be

$$R_1 = R_{S_1} + \text{ESR};\ R_2 = R_{S_2} + \text{ESR};\ C_1 = C_f$$
$$C_2 = \frac{C_f \cdot C_o}{C_f + C_o} \tag{36}$$
$$\beta_1 = \frac{1}{2f_s(R_{S_1} + \text{ESR})C_f}$$
$$\beta_2 = \frac{1}{2f_s(R_{S_2} + \text{ESR})\left(\frac{C_f \cdot C_o}{C_f + C_o}\right)}. \tag{37}$$

Since the average current of the load is transferred by the flying capacitor, $k_{1,2} = 1$. Applying (10), R_{e_i} is calculated for $i = 1, 2$

$$R_{e_1} = \frac{1}{2f_s C_f} \cdot \coth\left(\frac{\beta_1}{2}\right);\ R_{e_2} = \frac{1}{2f_s\left(\frac{C_f \cdot C_o}{C_f + C_o}\right)} \cdot \coth\left(\frac{\beta_2}{2}\right) \tag{38}$$

and the total equivalent resistance for the inverting SCC according to (1) and Fig. 3 is

$$R_e = \frac{1}{2f_s C_f} \cdot \left[\coth\left(\frac{\beta_1}{2}\right) + \frac{C_f + C_o}{C_o} \cdot \coth\left(\frac{\beta_2}{2}\right)\right]. \tag{39}$$

Diode conduction losses are modeled by adding to the generic equivalent circuit a voltage source V_D (see Fig. 13) that is equal to the sum of the forward voltage drops V_{f_i} of all the diodes in the circuit, times their proportionality constants k_i, which relate

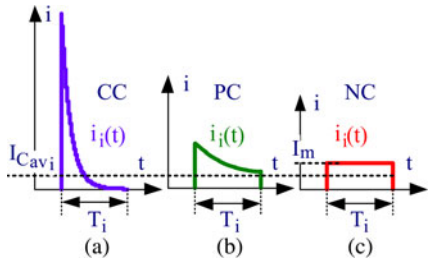

Fig. 14. Charge/discharge instantaneous current waveforms: (a) Complete charge—"CC" mode. (b) Partial charge—"PC" mode. (c) No charge—"NC" mode.

the average subcircuit's current through each diode to the output current

$$V_D = \sum_{i=1}^{m} (k_i \cdot V_{f_i}). \tag{40}$$

Since in this inverting SCC $m = 2$, $k_{1,2} = 1$, and assuming equal diodes $V_{f_1} = V_{f_2} = V_f$ one finds: $V_D = 2V_f$, where V_f is the average voltage drop across a single diode. Being an inverting 1:1 SCC, the target voltage V_T in this case is: $V_T = -V_{\text{in}}$ (see Fig. 13), V_D is also of negative polarity to correctly introduce the power loss for the negative current that will flow.

VII. Limits of Operating Modes

The behavior of SCC at the boundaries has been previously derived for the hard [6], [16]–[18], [28] and soft switching [6] cases. For the sake of completeness, we present here the limits by applying the loss expressions developed in this study.

Analysis of the loss expressions for the hard switched case reveals that the losses of a given SCC will depend on the value of (10) for each of the subcircuits. This value depends, in turn, on the operating mode of the SCC and in particular on the value of β_i, which will determine if (a) the charging/discharging process is completed within T_i having the current waveform shown in Fig. 14(a) (denoted here as the "CC" case), (b) the charging is partially completed (PC) having the current waveform that is presented in Fig. 14(b) or (c) the current will be about constant [see Fig. 14(c)] and the capacitor will have a practically constant voltage (denoted as No Charging—NC).

The modes of operation (CC, PC, or NC) depend on the value of β_i namely on the relationship between T_i and $R_i C_i$. The behavior of the function (10) can be conveniently examined by considering its asymptotic values when $\beta_i \ll 1$ and $\beta_i \gg 1$.

The asymptotic value for the NC case $\beta_i \ll 1$ ($T_i \ll R_i C_i$) is

$$R_{e_i\,(\text{NC})} = R_{e_i}\Big|_{\beta_i \ll 1} = \left\{k_i^2 \frac{R_i}{f_s T_i}\right\} \tag{41}$$

And for the CC case $\beta_i \gg 1$ ($T_i \gg R_i C_i$)

$$R_{e_i\,(\text{CC})} = R_{e_i}\Big|_{\beta_i \gg 1} = \left\{k_i^2 \frac{1}{2f_s C_i}\right\}. \tag{42}$$

Since β_i is a function of R_i, the general expression (10), which is applicable to the PC case, is clearly dependent on the switch resistance. Similarly, the losses in the NC case (41)

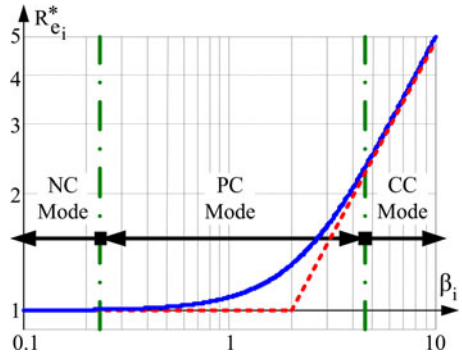

Fig. 15. Normalized equivalent resistance.

are also dependent on the switch resistance. Hence in these operating regions the switch resistance will affect the efficiency. In contrast, expression (42) implies that in the private case of the complete charge (CC), the switch resistance does not influence the losses. The same resistance independent result is obtained by an energy balance calculation, when a capacitor is charged to the full value of the charging voltage source. The behavior of R_{e_i} over the full range of the charge/discharge regions (CC, PC, and NC) is given in Fig. 15 which presents the normalized equivalent resistance of a single charge or discharge subcircuit, derived from (10) and normalized by the factor $\frac{1}{m \cdot k_i^2 \cdot R_i}$ and assuming symmetrical operation (same switching duration for each of the m subcircuits) (43)

$$R^*_{e_i} = \frac{R_{e_i}}{m \cdot k_i^2 \cdot R_i} = \frac{\beta_i}{2} \cdot \coth\left(\frac{\beta_i}{2}\right). \tag{43}$$

The curve can be approximated by two linear sections (see Fig. 15), one for high betas and one for low betas. For the high beta cases, which correspond to the CC mode (42), $1/f_s C$ is a dominant term forcing the equivalent resistance to increase linearly as beta increases. In the case of low betas (which correspond to the NC zone (41)), R_e is maintained constant due to the convergence of (43) to a constant value (41) as beta approaches zero. It can thus be concluded that when the switching duration is larger than the time constant of the subcircuit (corresponding to large betas), the equivalent resistance is independent of the switch resistance but heavily dependent on T_i, and thus the switching frequency. In this region, the lower the switching frequency, the larger will be the losses (for the same average subcircuit's current).

The lower loss at short switching times is a direct outcome of the fact that in this case [see Fig. 14(c)], the charge/discharge RMS current is smaller than in the exponential case [see Fig. 14(a)], which prevails in the longer switching time. When the switching time is much shorter than the time constant of the circuit, the current is practically constant during the switching time and hence the RMS value is the lowest possible. For the nonsymmetrical case, the RMS currents of each phase are not equal and the total equivalent resistance will reach higher values as depicted in Fig. 17 for the two phases, hard switched, unity converter.

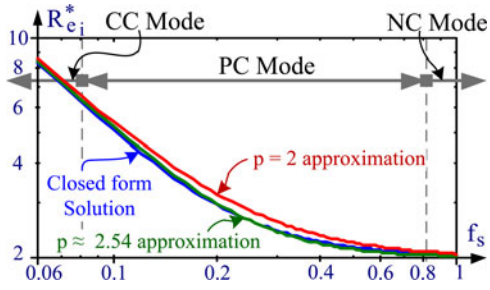

Fig. 16. Comparison of two equivalent resistance empirical equations to closed form solution.

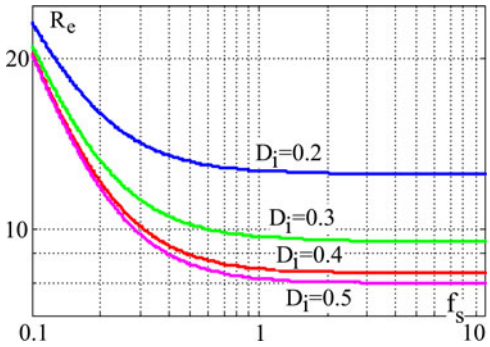

Fig. 17. Dependence of the equivalent resistance on the duty cycle D as a function of normalized frequency in a two phase hard switched unity SCC.

It has been suggested in [16] and [52] that the values of R_e around the breakpoint of the curve shown in Fig. 15 can be approximated by an empirical equation (44) that applies the boundary values of R_e, (41) and (42), that were derived earlier [6], [16]–[18], [28]

$$R_{e_i} = \sqrt[p]{R^p_{e_i(\mathrm{NC})} + R^p_{e_i(\mathrm{CC})}} \tag{44}$$

where $p = 2$. However, in a following study [53], Makowski re-examined the approximation by comparing it to (10) and showed that a better fitting is obtained when $p = 2.54$. An example of the fitting accuracy is given in Fig. 16.

Similar to the hard switching case, the loss expressions for the soft switched converters was evaluated in this study as a function of the output current (19, 20) which imply that the total equivalent resistance of the SCC also follows the simple addition concept as depicted in Fig. 3, as proposed in this work. Expression (20) reveals that the losses are a function of three key parameters: R_i, which is the subcircuit's resistance, df_i, which is the ratio between the switching frequency, f_s, and the damped resonant frequency, f_{di}, of the *RLC* subcircuit, we call it the "frequency ratio," and Q_i, which is the *RLC* subcircuits' quality factor. The dependence of the normalized RLC subcircuit's equivalent resistance, R^* (45), on the quality factor Q_i, with df_i as a parameter is depicted in Fig. 18, where

$$R^* = \frac{R_{e_i}}{k_i^2 \cdot R_i} = \frac{2Q_i^2 \cdot \pi}{df_i \cdot \sqrt{4Q_i^2 - 1}} \cdot \tanh\left(\frac{\pi}{2\sqrt{4Q_i^2 - 1}}\right). \tag{45}$$

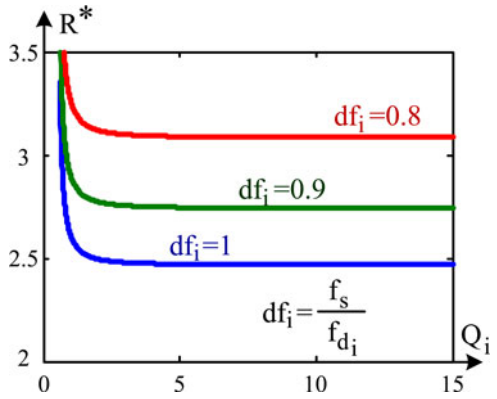

Fig. 18. Dependence of the normalized *RLC* subcircuit's equivalent resistance on the subcircuit's quality factor Q_i with frequency ratio df_i as a parameter.

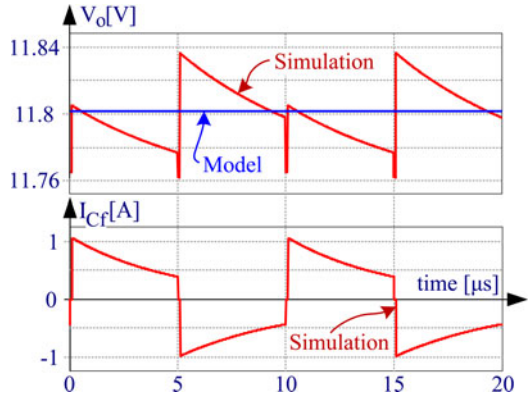

Fig. 19. Simulated and model calculated results of hard switched 3:1 step-down SCC: Upper traces—output voltage. Lower trace—capacitor current C_{f1}.

Fig. 18 reveals that the normalized equivalent resistance is a weak function of Q, once the quality factor is above 3. However, the frequency ratio has a strong effect on the equivalent resistance Fig. 18. This is due to the fact that the rms current of the subcircuit increases as df_i becomes smaller ($df_i = f_s/f_{di}$). The increase in R_e can be used, as in the case of the hard-SCC, to regulate the output voltage. This can conveniently be done by controlling the switching frequency f_s. To maintain soft switching, the boundary $T_i \geq \pi/\omega_{d_i}$ must be observed.

The highest efficiency in the soft-SCC are thus reached when two conditions are met: 1) the value of the quality factor is at least 3 and 2) the switching duration T_i is matched to half damped resonant period, $T_i = \pi/\omega_{d_i}$.

For the high-quality factor case, condition 1)—($Q_i \gg 1$), the expression of the equivalent resistance (20) can be significantly simplified. Applying Taylor's series extension one finds that $\tanh(x)$ can be approximated by x, when x approaches zero. A further simplification is obtained by approximating the term of $(4Q_i^2 - 1)$ as $4Q_i^2$, and consequently (20) can be approximated by expression (46)

$$\lim(R_{e_i})|_{Q_i \gg 1} = k_i^2 \cdot \frac{2Q_i^2 \cdot \pi \cdot R_i}{df_i \cdot \sqrt{4Q_i^2}} \cdot \left(\frac{\pi}{2 \cdot \sqrt{4Q_i^2}} \right) \tag{46}$$

which can be expressed as follows:

$$\lim(R_{e_i})|_{Q_i \gg 1} = k_i^2 \cdot \frac{\pi^2 \cdot R_i}{4 \cdot df_i}. \tag{47}$$

In the case of a symmetrical 1:1 SCC ($k_{1,2} = 1$), with matched frequencies for both phases ($f_{d(1,2)} = f_s, df_{1,2} = 1$), the limiting value for each of the subcircuits takes the form

$$\lim(R_{e_i})|_{Q_i \gg 1} = k_i^2 \cdot \frac{\pi^2 \cdot R_i}{4df_i} \approx \frac{1}{2} \cdot 5R_i. \tag{48}$$

The results of the private 1:1 SCC case (48) are similar to those presented in [6], which were derived by applying the first harmonic approximation. The more general expression, which is applicable for any Q value above 1/2 is given in (20), while the limiting equivalent resistance value for any *RLC*-based SCC, is expressed by (47).

VIII. Verification by Simulation and Experiments

The analytical expressions developed in this study were verified against simulation and experimental results. Output voltage measurements were used as an indicator for conduction losses of the converter, applying the fact that the efficiency of SCC is given by

$$\eta = \frac{V_o}{M \cdot V_{\text{in}}} = \frac{V_o}{V_T} \tag{49}$$

where η is an efficiency, V_{in} is an input voltage, M is the conversion ratio of the SCC, V_T is a target voltage of SCC, ($M \cdot V_{\text{in}} = V_T$), and V_o is an output voltage (see Fig. 1), [2]–[4], [9], [17], [21], [23], [27], [28], [32], [38]. It should be mentioned here that (49) is correct under the assumption that switching losses [39] and substrate capacitive leakage currents [41] and other extraneous effects are negligibly small as compared to the average current transferred by the SCC. Furthermore, charge flow paths within the converter that are not directly transferring charges from input to output [54] may also cause the efficiency value to deviate from (49). Hence, the measurement of the output average voltage while the output ripple is relatively low reflects the amount of losses in SCC

$$\frac{P_{\text{Loss}}}{P_{\text{in}}} = \frac{P_{\text{in}} - P_{\text{o}}}{P_{\text{in}}} = 1 - \eta = 1 - \frac{V_o}{V_T} \tag{50}$$

where P_{in} is the input power, P_o is the output power, and P_{Loss} is the conduction losses. Consequently

$$P_{\text{Loss}} = P_{\text{in}} \left(1 - \frac{V_o}{V_T} \right). \tag{51}$$

Furthermore, the value of V_o is in fact determined by R_e, since

$$\eta = \frac{R_o}{R_e + R_o} = \frac{V_o}{V_T} \tag{52}$$

and hence

$$R_e = \frac{R_o(V_T - V_o)}{V_o}. \tag{53}$$

Fig. 19 presents simulation and model derived results for a step down 3:1 hard-SCC shown in Fig. 9. The equivalent resistance was calculated using (34). SCC parameters were set

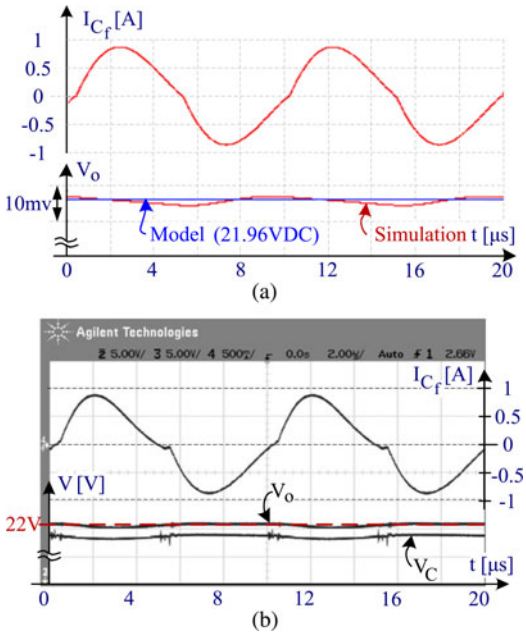

Fig. 20. Soft switched 1:1 unity converter waveforms: (a) Simulation and model. (b) Experimental details.

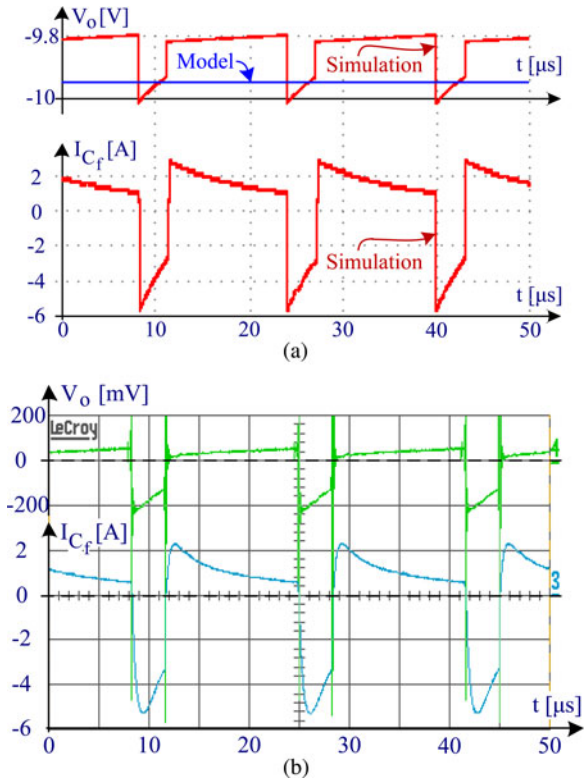

Fig. 21. Hard switched inverting 1:1 SCC waveforms: (a) Full circuit (cycle by cycle) simulation and model calculation. (b) Experimental details.

to be $V_{\rm in} = 36$ V, $C_{f1,2} = 22$ μF, ESR $= 100$ mΩ, $C_o = 560$ μF, ESR$_o$ is negligible, $R_L = 12$ Ω, $R_{ds\_{\rm on}} = 100$ mΩ, $f_s = 100$ kHz, and dead time of 100 ns. Model derived and step by step full circuit simulation output voltage was found to be 11.8 V, which corresponds to 2% losses [calculated using (50)].

Fig. 20(a) depicts simulation and model derived results of a soft switched 1:1 unity converter (see Fig. 7). $V_{\rm in} = 24$ V, $L = 2.3$ μHy, $C_f = 1$ μF, ESR $= 70$ mΩ, $C_o = 560$ μF, ESR$_o = 38$ mΩ (assumed to be zero for simulation and model evaluation), $R_L = 91$ Ω, $R_{ds\_{\rm on}} = 0.85$ Ω, $f_s = 100$ kHz, and dead time of 100 ns. The experimental waveforms for this soft switching case are presented in Fig. 20(b). The simulated and model derived output voltage was 21.96 V, which represents 8.5% losses, while the measured output voltage in this case was 22 V, which corresponds to a loss of 8.333% (50). Model equivalent resistance was calculated by (27).

The inverting SCC, as presented in Fig. 11 was evaluated under asymmetrical operation, at a duty cycle of 0.8. SCC parameters were as follows: $V_{\rm in} = 12$ V, $C_f = 22$ μF, ESR $= 100$ mΩ, $C_o = 560$ μF, ESR$_o = 38$ mΩ (assumed to be zero for simulation and model evaluation), $R_L = 12.1$ Ω, $f_s =$ 60 kHz, and dead time of 100 ns. Based on the datasheet and operational conditions, the average forward diode voltage drop of MBR320P diodes was estimated to be around 0.35 V. The switches were: S$_1$—SMU10P05, S$_2$—SMU15N05 with $R_{ds\_{\rm on}}$ of 0.28 and 0.1 Ω, respectively. The power associated with drive and control of the inverting prototype is not included in the efficiency calculations presented here. Rise and fall times of the switches were approximately 100 ns that is significantly shorter than the switching period, and as such switch transition associated losses (switching losses) are neglected in the efficiency calculations [39]. Model equivalent resistance was calculated using (39) and model equivalent diode voltage source was calculated using (40). Simulation and model results are presented in Fig. 21(a), and experimental results in Fig. 21(b). Model derived output voltage was found to be -9.95 V, which represents a loss of 17.1%, while the step by step simulation result yielded -9.84 V that represents a loss of 18%, experimentally measured output voltage was -9.81 V, corresponds to 18.25% loss.

An additional example of equivalent resistance and loss calculation and its experimental validation in a multiphase, multicapacitor, extended binary SCC is described in [51], [55]. Furthermore, recently proposed SCC [56]–[58] can be approximated by first-order RC subcircuits and can thus be analyzed by the proposed approach, which can also be applied to hybrid converters that include both a switch inductor and switched capacitors section [59], [60].

IX. Discussion and Conclusion

The loss analysis approach developed in this study resulted in a unified model that describes conduction losses of the subcircuits in the hard and soft-SCC cases. Closed form solutions were derived and verified against complete (cycle-by-cycle) simulation and experimentally.

An important feature of the proposed model is that it is based on the SCC subcircuits' average capacitor currents. This enables a systematic procedure for modeling multiphase and multicapacitor SCC systems over the complete range of operation (CC, PC, and NC) for the hard switching cases and for any switching frequency (provided that $T_i \geq T_{\omega_d}/2$) for the soft switched cases. The proposed model is applicable to SCC topologies for

which the subcircuits can be described by a first-order network. However, as demonstrated in this paper, subcircuits of practical SCC, which do not appear to meet this first-order requirement, can still be approximated as a first-order networks and can thus be analyzed by proposed modeling approach.

Another unique feature of the model is its ability to handle hard- and soft-SCC topologies that include diodes, topologies that are often referred to as "charge pumps" or "voltage multipliers." This capability is automatically achieved due to the fact that the analysis is based on the average currents in the subcircuits, which are the pivotal parameters for calculating diode loss.

The proposed model applies a new concept "the equivalent resistance of a subcircuit" R_{ei}, which is a measure of the dissipative component defined in terms of the average subcircuit's current. Since the average subcircuits currents are linearly proportional to the output current, the subcircuits' equivalent resistance can be considered as the basic components of the total equivalent resistance of the system (see Fig. 3). Since the losses of each subcircuit are evaluated independently, the contribution of each subcircuit is made clear and intuitive. This could help to optimize SCC designs by trimming the fundamental parameters that affect the losses. That is, the ratio between the subcircuits' switching time T_i and the time constant $R_i\mathrm{C}_i$, in hard switching and the quality factor and the ratio between the switching and the resonant frequencies, in the soft switched case. In addition, since the model is based on the equivalent circuit approach rather than the state space averaging model methodology, it is seamlessly compatible with general purpose circuit simulators and can be used to explore various output voltage regulation schemes [55], [61]–[63], and to develop average simulation models [43], [44], [60], [64].

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Michael Evzelman (S'09) received the B.Sc. degree in electrical and electronics engineering from the Samy Shamoon College of Engineering, Beer-Sheva, Israel, in 2006, and the M.Sc. degree in electrical and computer engineering from the Ben-Gurion University of the Negev, Beer-Sheva, Israel, in 2009, where he is currently working toward the Ph.D. degree.

His current research interests include modeling, simulation, and design of switched capacitor converters. His areas of interests also include power circuits modeling and simulation, and power factor correction.

Shmuel (Sam) Ben-Yaakov (M'87–SM'08–F'10) received the B.Sc. degree in electrical engineering from the Technion, Haifa, Israel, in 1961, and the M.S. and Ph.D. degrees in engineering from the University of California, Los Angeles, in 1967 and 1970, respectively.

He is currently an Emeritus Professor with the Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev (BGU), Beer-Sheva, Israel, where he served as Chairman from 1985 to 1989. He serves as the Head of the Power Electronics Group of BGU. His current research interests include power electronics, circuits and systems, electronic instrumentation, and engineering education.