Digital Control of Resonant Converters: Enhancing Frequency Resolution by Dithering

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***Abstract*- Resonant converters and related systems, such as piezoelectric transformers, may require a high-resolution frequency drive when the quality factor of the network is high or to avoid limit cycle oscillations. This high frequency resolution requirement could be beyond the capabilities of low cost microcontrollers. To remedy this problem, a frequency resolution enhancement algorithm was developed, tested by simulations and verified experimentally. The proposed approach is based on a modification of the fractional-N dithering concept and includes an adaptive dithering period and smooth DPWM frequency transitions. The implementation of the approach on the digital hardware is simple and requires modest additional workload from the CPU.**

Theoretical analysis was carried out to model the proposed dithering method when applied to drive resonant network in order to identify the causes and to quantify the expected output signal distortion when the signal is used to drive resonant networks. The proposed approach was tested experimentally on two types of resonant converters: a series-resonant parallel-loaded converter and a piezoelectric transformer. It was found that the output signal distortion is less than 1% of the peak amplitude of the output drive which would be acceptable in many applications. The experimental results were found to be in excellent agreement with the theoretical predictions, validating the usefulness of the dithering method as a frequency resolution enhancer for resonant network drive.

I. INTRODUCTION

In a variety of applications, variable frequency is the preferred method for output regulation of resonant converter (e.g. fluorescent lamp ballasts piezoelectric devices) [1-3]. In such cases, the frequency resolution of the drive is crucial to ensure accurate operating conditions and the desired load performance.

At present, the control of resonant converters is mostly dominated by analog controllers that use Voltage Controlled Oscillator (VCO) with very high resolution capability [4]. In digital controllers, the frequency generation is obtained by timers that can be programmed to reset at a desired value, while maintaining a constant duty ratio of 50%. This is conventionally realized by the embedded Digital PWM (DPWM) of microcontrollers and DSPs peripheral units since they include built-in timers, period compare registers and are capable to operate multiple channels (for synchronous bridge, interleaving etc.) with in-phase, complementary or deadband synchronization.

The frequency resolution and accuracy that can be attained by the DPWM units are limited by the system's clock frequency. Unfortunately, to achieve a performance that is similar to an analog VCO, very high clock frequencies are required that translates into rather costly processors. For example, a 50MHz DPWM clock is needed to generate a 50 KHz signal with frequency resolution of 10bit (50Hz steps).

Recent studies related to digital control of resonant converters [5, 6] report the use of either powerful processor with high DPWM clocks to achieve the required control accuracy, or settle for more relaxed specifications that translate into a modest digital hardware [7-9].

Another important aspect of the necessity for high frequency resolution drive, emerges when resonant converters operates in closed loop where the frequency serves as the control signal. In this case, analogous to PWM control design, to avoid limit cycle oscillations of the output at steady state, the frequency resolution of the DPWM has to be made high enough such that the output variation due to a LSB change of the DPWM will be smaller than the ADC resolution levels (one LSB).

The conventional method for obtaining a frequency resolution that is higher than what can be achieved by the clock frequency division is frequency dithering. In this approach, the DPWM output frequency is hopped between some values such that the average frequency over time will be in between the DPWM discrete frequencies. The main challenge of this method is that the frequency of the DPWM can be updated only at the beginning of a new count cycle, making this approach impractical in applications that include a low Q resonant tanks which respond fast to frequency changes.

The two most popular frequency dithering techniques are the fractional-N and sigma-delta modulation [10-13]. Both methods modulate the DPWM period between two neighboring values, where the frac-N approach operates at a defined rate whereas in sigma-delta the modulation rate changes arbitrarily. It is well documented that the sigma-delta method offers a "cleaner" spectral content of the yielded signal. However, proper operation the sigma-delta modulation requires over-sampling (updating the DPWM during count cycle) which is impractical for smooth signal generation. Furthermore, since frac-N dithering can be simply implemented on the digital

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hardware, makes it the preferred method for frequency generation by DPWM.

Some commercial microcontroller products [14, 15] include a frequency resolution enhancement (hardware embedded) by a variation of frac-N method and additional features dedicated to power applications. A significant drawback of the approach implemented in these products, which is based on the use of a fixed dither period (i.e. every predetermined 'k' number of PWM cycles) for all fractional frequencies (frequencies that are in between the original DPWM frequencies), is a considerably slow response of the system in closed loop.

The objective of this work was to develop a modified frac-N dithering method for frequency resolution enhancement that is based on adaptive dither period to maximize the response, and is easily implemented by the digital hardware already available in commercial microcontrollers and DSPs. Another objective was to explore the viability and features of the proposed method when used as a drive for resonant converters.

II. Proposed Frequency Dithering Approach

The basic operation of frequency generation by a DPWM unit consists of an up/down counter incremented every time interval that is set by the unit clock, TB_{clk}, (at the rate of the system's clock or its divisions), the counter is reset whenever the count reaches the value programmed (N_{per}) in its period compare register. The generated frequency, f_{DPWM}, can be expressed by

$$f_{DPWM} = \frac{1}{N_{per} TB_{clk}} \quad (1)$$

The frequency resolution, f_{res}, can be calculated as the difference between two nearest period settings (N_{per}) and (N_{per}+1)

$$f_{res} = \frac{1}{N_{per} TB_{clk}} - \frac{1}{(N_{per}+1) TB_{clk}} \approx \frac{1}{N_{per}^2 TB_{clk}} = TB_{clk} f_{DPWM}^2 \quad (2)$$

Frac-N dithering is facilitated by dithering the DPWM period between (N_{per}) and (N_{per}+1) at a defined rate, varied by the required accuracy. The "dither factor" 'n' is the number of DPWM cycles needed to achieve the desired fractional frequency. Dithering is accomplished by keeping a constant period over (n-1) DPWM cycles (will be referred as base period) and then changing the last slot (n) to another period. For example (Fig. 1), if a frequency fraction of $0.25f_{res}$ desired, the DPWM will generate one (N_{per}+1) period every 4th cycle. The resultant (average) frequency in this method can be calculated by

$$f_{DPWM\_dit} = \frac{1}{[(n-1)N_{per} + (N_{per}+1)]/n \, TB_{clk}} = \frac{1}{\left(N_{per} + \frac{1}{n}\right) TB_{clk}} \quad n = 1,2,3... \quad (3)$$

and the frequency resolution

$$f_{res\_dit} = \frac{1}{\left(N_{per} + \frac{1}{n+1}\right) TB_{clk}} - \frac{1}{\left(N_{per} + \frac{1}{n}\right) TB_{clk}} \approx \frac{1}{n(n+1) N_{per}^2 TB_{clk}} = \frac{TB_{clk} f_{DPWM}^2}{n(n+1)} \quad (4)$$

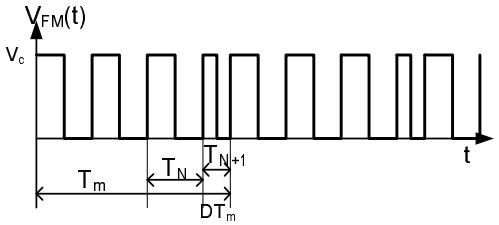

Figure 1. Dithered drive signal with frequency fraction of $0.25f_{res}$.

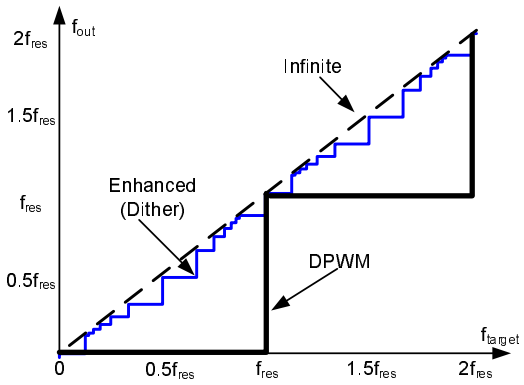

Figure 2. Output frequency versus desired frequency for ordinary DPWM and 3 bit resolution enhancement.

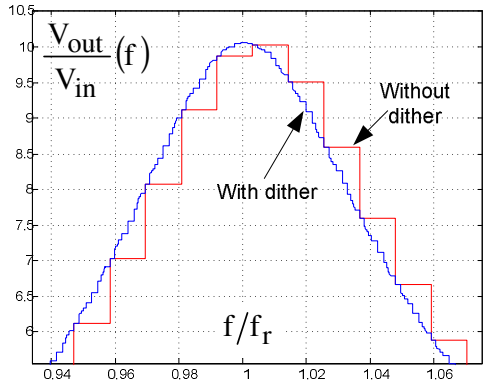

Figure 3. Simulated frequency response (sweep) of a resonant network, with DPWM frequency steps and proposed method.

Fig. 2 shows the possible frequency states of this method for a 3 bit frequency resolution enhancement, compared to the ordinary operating of the DPWM (as a frequency generator).

III. Proposed Frequency Dithering as a Resonant Converter Signal Drive

The effect of frequency resolution in resonant converts drive is depicted in Fig. 3 which is the simulated output response of a series-resonant parallel-loaded resonant network driven by an 8bit DPWM and by the proposed dithered-DPWM with 3bit resolution enhancement.

The dithered-DPWM drive can be modeled by a frequency signal (f_c, carrier) that is FM modulated by a fixed on-time, variable period squarewave, and is passed thru an amplitude limiter to obtain a squarewave output (Fig. 4). In this work this signal was used as a drive to resonant networks (Fig. 5) with Q>1 to assure proper operation of the resonant converter. In these cases the harmonic content that is not around the resonant

frequency will be filtered out which justifies the following approximation of the drive signal:

$$V_{FM}(t) = V_c \cos[\omega_c t + \varphi_{FM}(t)] \qquad (5)$$

The amplitude of the modulating signal, f_{dev}, (FM frequency deviation) corresponds to the base frequency step (f_{res}, eq. 2) of the DPWM. The dithered signal's period will be the base period times the dither factor as required to achieve the desired frequency fraction of the base resolution. The modulating (dither) signal, $V_m(t)$ (Fig. 6) can be expressed by the series

$$V_m(t) = Df_{dev} + \frac{2f_{dev}}{\pi} \sum_{j=1}^{\infty} \frac{1}{j} \sin(j\pi D)\cos(j\omega_m t) \qquad (6)$$

where 'j' is the harmonic's index, D=1/n is the duty ratio of $V_m(t)$, $\omega_m = \omega_c/n$ is the frequency of the modulating signal (ω_c is the DPWM base frequency of (1)). A typical spectral content of the modulating signal of (6) is depicted in Fig. 7.

Since the frequency deviation of the FM signal (amplitude of $V_m(t)$) is considerably smaller than the carrier frequency, the influence of harmonic content higher than ω_m is negligibly small, and a first harmonic approximation of $V_m(t)$ can be applied. The approximated signal will thus be

$$V_{m\_1st}(t) = Df_{dev} + \underbrace{\left[\frac{2f_{dev}}{\pi}\sin(\pi D)\right]}_{\alpha}\cos(\omega_m t) \qquad (7)$$

The phase of the dithered output is derived by integrating (7)

$$\varphi_{FM}(t) = 2\pi f_{dev} Dt + \frac{2\pi}{\omega_m}\alpha \sin(\omega_m t) \qquad (8)$$

Substituting (8) into (5) yields the FM modulated output

$$V_{FM}(t) = V_c \cos\left[(\omega_c + 2\pi f_{dev} D)t + \frac{2\pi}{\omega_m}\alpha \sin(\omega_m t)\right] \qquad (9)$$

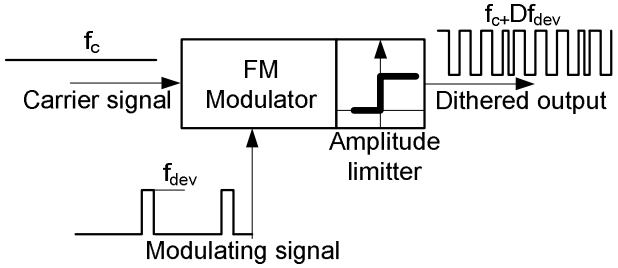

Figure 4. Simplified equivalent model of the dithered output generation.

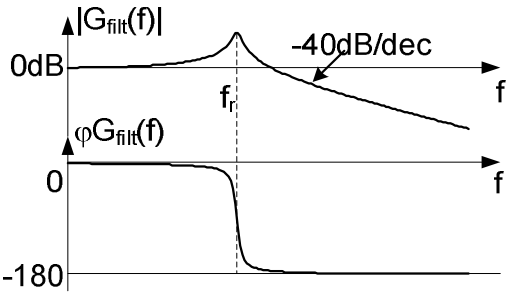

Figure 5. Frequency response of a series-resonant parallel-loaded network.

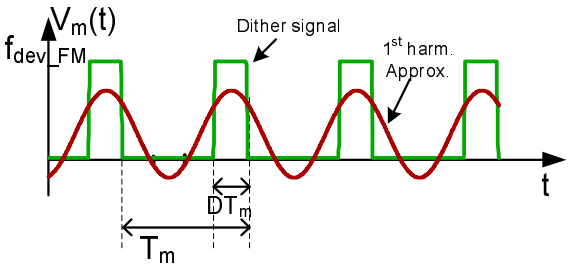

Figure 6. Dither (modulating) signal and its first harmonic approximation.

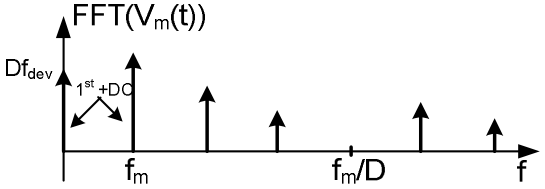

Figure 7 Typical Spectral content of the dithered signal of Fig. 6

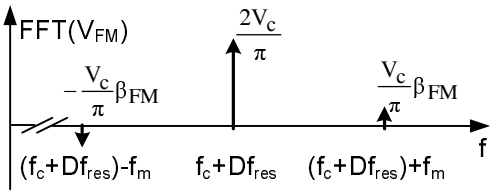

Figure 8. Spectral content of NBFM representation of the dithered output.

The last equation implies that the dither operation generates a FM signal with a new carrier frequency ω_d, shifted from the base frequency ω_c by the offset (DC) level of the dither squarewave, and sidebands determined by the modulation factor β_{FM}

$$\omega_d = \omega_c + 2\pi f_{dev} D \qquad \beta_{FM} = \frac{\alpha}{f_m} = \frac{2f_{dev}}{f_m \pi}\sin(\pi D) \qquad (10)$$

Considering the fact that the modulation factor β_{FM} is relatively small, (9) can be considered as a Narrow Band FM (NBFM) and can therefore be rewritten as

$$V_{FM}(t) = \frac{2V_c}{\pi}\cos(\omega_d t) - \frac{V_c}{2}\beta_{FM}\cos(\omega_d - \omega_m)t + \frac{V_c}{2}\beta_{FM}\cos(\omega_d + \omega_m)t \qquad (11)$$

Fig. 8 shows typical spectral content of NBFM signal of (11).

The effect of this type of drive on the output of a resonant network in terms of harmonic content can now be evaluated by considering the example of the resonant network of Fig. 5. It is clear that when the center frequency of the FM drive is around the resonant frequency, the already low magnitude sidebands will be further attenuated, leaving a clear sinusoidal output. However, when operation in off-resonance modes (e.g. for controlled output operation), the sidebands may not be filtered out, resulting in AM behavior at the output. The extreme case will obviously be when one of the sidebands will be around the resonance frequency. It was found however, that the effect of the sidebands is relatively small, introducing an AM envelope in the range of 1% of the peak output amplitude which would be acceptable in many applications.

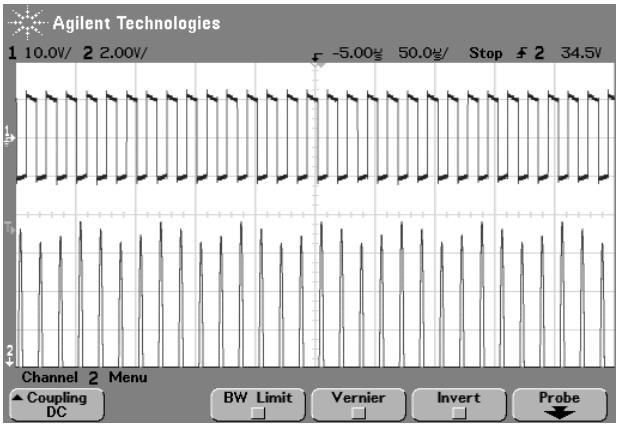

Figure 9. AM envelope content of the output voltage (lower trace, 2V/div) of a series-resonant parallel-loaded network driven by the proposed dithering method with dither factor n=4. Upper trace, frequency dithered input voltage (10V/div), horizontal scale: 50μS/div.

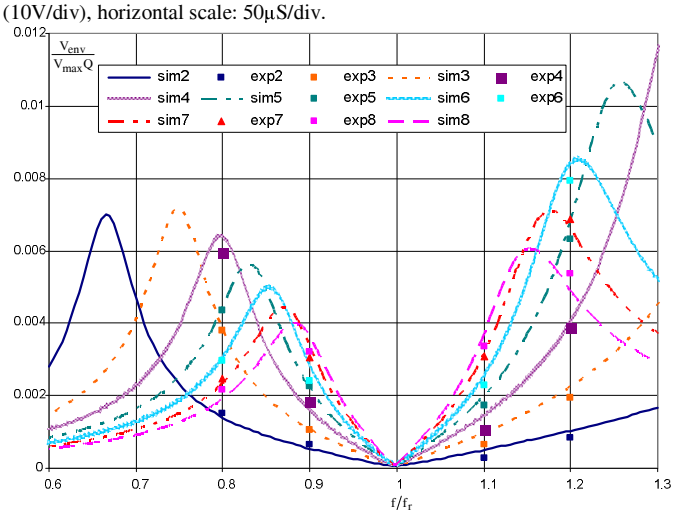

Figure 10. Simulation and experimental results of normalized AM content of the output voltage of a resonant network as a function of the frequency (normalized) for various dither factors (2-8). Symbols – experimental points.

Example of the AM envelope content of the output signal is depicted in Fig.9. A numerical calculation (carried out by MATLAB (Mathworks, USA)) of a resonant network subjected to the proposed drive signal was carried out to map the possible cases of the expected output waveform distortion. This was done by first deriving the response of the resonant network for the dithered drive of (11) at a given frequency and dither factor conditions using the 'lsim' command, extracting the AM envelope content of the output using Hilbert transform ('Hilbert' command in MATLAB) and comparing it to the mean peak amplitude of the output signal. This process was repeated over the frequency span of interest (between 0.6 to 1.3 of the resonant frequency) and the dither factors 'n' possible (2 to 8). The results were verified experimentally and are summarized in Fig. 10. It was found that the peak distortion curves (Fig. 10) are not symmetrical with respect to the resonant frequency of network. One reason for this is that the sidebands frequencies of the dithered drive signal (11) depend of the operation frequency ($\omega_m = \omega_c/n$) as can be seen in (6), Fig. 7. That is, at lower operating frequency the sidebands will be closer to the center frequency than they would have been at higher frequency. The second reason is more related to the frequency response of the network that is subjected to the dithered signal. Given the response shown in Fig. 5, it is obvious that at operation frequencies higher than the resonant frequency, the AM content of the output will be more substantial since the center frequency of the signal may also be attenuated.

IV. Experimental Verification

The capabilities of the proposed dither method as a frequency resolution enhancer and as a resonant network drive were verified experimentally. The proposed frequency dither was implemented digitally on a TMS320F2808 DSP for 3bit frequency enhancement. To demonstrate the operation in microcontrollers of modest frequency resolution, the DPWM unit clock was scaled down to 160nS (instead of the original 10nS), resulting in frequency steps of 560Hz around the operation range (40 KHz to 65 KHz). The experiments were carried out for two types of resonant converters: a series resonant parallel-loaded (Fig. 11) network and a piezoelectric transformer (ELECERAM ELM-610) (Fig. 12). In the piezoelectric transformer case the output signal of the drive (half bridge) signal was filtered to obtain a sinusoidal shape drive to eliminate undesired harmonic excitation [16].

Fig. 13 include a set of experimental measurements that show frequency sweeps of the resonant network and piezoelectric transformer with and without frequency dithering. The results validate the proposed method. Also shown in Fig. 13 is a magnified view of the frequency sweeps around resonance which depicts the fine steps of the enhanced resolution method. The results are in very good agreement with the simulations of Fig. 3.

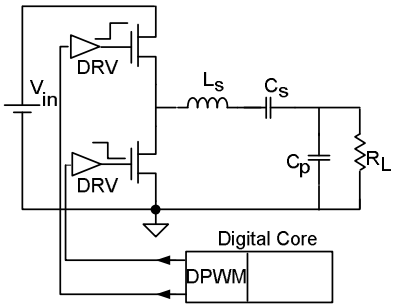

Figure 11. Experimental setup for a series-resonant parallel-loaded converter.

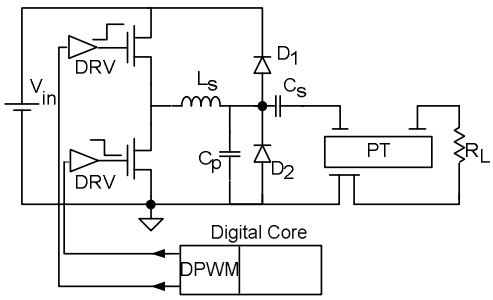

Figure 12. Experimental setup for a piezoelectric transformer drive.

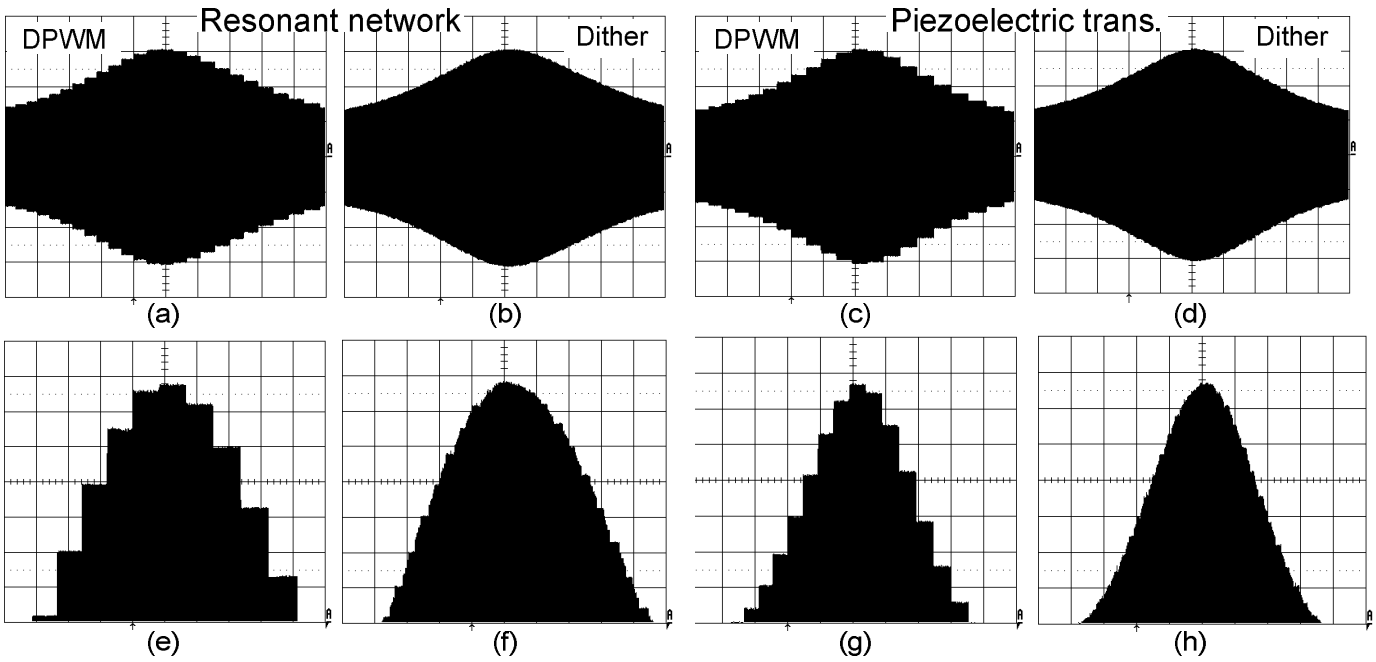

Fig. 13. Experimental results. Output signal during frequency sweep (a-d) and the corresponding magnified views (e-h) with DPWM operation (a, e ; c, g) and enhanced frequency resolution (b, f ; d, h) of a resonant network (a-b): 43KHZ-57KHz, 20V/div, (e-f): 46KHz-53KHz, 2V/div, and of a piezoelectric transformer (c-d): 46KHZ-55KHz, 50V/div, (e-f): 48KHz-52KHz, 5V/div, Horizontal scale (a-d): 100mS/div (e-h): 50mS/div.

V. Discussion and Conclusions

A new dithering method for enhanced frequency resolution for digitally controlled resonant converters was developed. The method has adaptive dither rate depending of the desired accuracy which improves the resolution of the frequency drive and hence the total response of the system. The realization of the dither algorithm on the digital core is straightforward and simple.

The output signal distortion (AM content) of the output of the resonant network when driven by frequency dithered signal depends of the dither factor 'n' and the quality factor Q of the resonant network driven. The intuitive interpretation of this behavior is the fact that the response time of a resonant network to frequency changes is approximately Q cycles, hence, when subjecting a resonant network with a high quality factor Q to a FM modulated signal with a high modulation rate, the instantaneous frequency changes will not be seen at the output, leaving only the average frequency and some residual AM content that is caused by the attenuated sidebands. .

Another way to look at the 'averaging" effect when the Q is high is by considering the modulation effect of the dithering action (Eq. 9) on the drive signal of resonant networks. This operation creates a frequency modulated (narrow banded) signal that include a new center frequency ω_d and sidebands that deviates from the base frequency ω_c by a factor that is proportional to frequency resolution and the dither factor. When this signal, which is in fact a form of amplitude modulation, is passed thru a resonant network with resonant frequency around ω_d, the carrier signal will be amplified whereas the sidebands will be further attenuated, leaving a clear shaped sinusoidal output signal at the frequency of ω_d.

The theoretical analysis that was carried out provides the methodology to identify the operation regions that are more prone to signal distortion given the system parameters and the desired operating conditions (frequency and resolution).

Numerical calculations and experiments verify the theoretical analyses developed in this work and demonstrate the viability of the method as drive signal generator for resonant converters, for both high and modest Q applications.

One object of the frequency resolution enhancement is to avoid limit cycle oscillations when operating in closed loop. The absolute criterion to overcome these oscillations is to assure a high enough frequency resolution of the control such that the output variation due to a LSB change of the command will be smaller than the ADC resolution levels (one LSB). However, one has to be aware that the power stage sensitivity to frequency changes depends to a large extent on the operating frequency and the network's quality factor. The complete derivation of limit cycles conditions of such systems is detailed in [17].

The resolution enhancement approach opens the gate for wider and more economical use of digital controllers for resonant converters applications, and offers a good solution to the issues of the control accuracy and limit cycle oscillations of these systems.

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REFERENCES

[1] C. Ordiz, J. M. Alonso, M. A. Dalla Costa, J. Ribas and A. J. Calleja, "Development of a high-voltage closed-loop power supply for ozone generation", *IEEE Applied Power Electronics Conference, APEC-2008*, pp. 1861-1867, Austin, Tx., 2008.

[2] S. Ben-Yaakov and G. Ivensky, "Drivers and rectifiers for piezoelectric elements," in *IEEE Power Electronics Specialists Conference PESC-2005,* Tutorial Recife, Brazil, 2005 [Online]. Available: http://www.ee.bgu.ac.il/~pel/public.htm#4

[3] R. L. Lin and Y. T. Chen, "Electronic ballast for fluorescent lamps with phase-locked loop control scheme", *IEEE Trans. on Power Electronics*, vol. 21, no. 1, pp. 254-262, Jan. 2006.

[4] Texas Instruments, "3863 Resonant-mode power supply controllers data sheet", available at www.ti.com, Doc No. uc3863.pdf.

[5] Y. Yin, M. Shirazi and R. Zane, "Fully integrated ballast controller with digital phase control" *IEEE Applied Power Electronics Conference, APEC-2005*, pp. 1065-1071, Austin, Tx., 2005.

[6] F. J. Diaz, F. J. Azcondo, R. Casanueva, C. Branas, and R. Zane, "Digital control of low-frequency square-wave electronic ballast with resonant ignition using", *IEEE Trans. on Industrial Electronics*, vol. 55, no. 9, pp. 3180-3191, Mar. 2004.

[7] Oh In-Hwan, M. Rayabhari, and M. A. Zecchini, "A full-digital dimming ballast with a digital power controller (DPC) for a fluorescent lamp", *IEEE Industry Applications Conference, IAS-2004*, pp. 333-337, 2004.

[8] Duk Jin Oh, Hee Jun Kim, and Kyu Min Cho,"A digital controlled electronic ballast using high frequency modulation method for the metal halide lamp", *IEEE Power Electronics Specialists Conference, PESC-2002*, pp. 181-186, Cairns, 2002.

[9] N. S. Bayindir, O. Kukrer, and M. Yakup, "DSP-based PLL-controlled 50-100 kHz 20 kW high-frequency induction heating system for surface hardening and welding applications", *Electric Power Applications, IEE Proceedings*, vol. 150, no. 3, pp. 365-371, May 2003.

[10] B. Miller, R. J. Conley, "A multiple modulator fractional divider", *IEEE Trans. Inst. and Meas*., vol. 40, no. 3, pp. 578-583, June 1991.

[11] A. Howard, "Delta-sigma modulator PLLs with dithered divide-ratio", Agilent EEsof EDA web files, http://eesof.tm.agilent.com/, Doc. no. HF_TechNote_110201.pdf.

[12] T.A.D. Riley, M. A. Copeland, and T.A. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis", *IEEE Journal of Solid-State Circuits*, vol. 28, no. 5, pp. 553 – 559, May 1993.

[13] M. Hovin, A. Olsen, T. S. Lande, and C. Toumazou, "Delta-sigma modulators using frequency-modulated intermediate values", *IEEE Journal of Solid-State Circuits*, vol. 32, no. 1, pp. 13 – 22, Jan. 1997.

[14] Atmel Corporation, "AT90PWMx microcontrollers data sheet", available at www.atmel.com, Doc No. doc7710.pdf.

[15] Microchip Technology, "dsPIC30F SMPS reference manual, sec. 29 oscillator section", available at www.microchip.com, Doc No. 70268A.pdf.

[16] G. Ivensky, G., M. Shvartsas, and S. Ben-Yaakov,"Analysis and modeling of a voltage doubler rectifier fed by a piezoelectric transformer". *IEEE Trans. on Power Electronics*, vol. 19, no. 2, pp. 542-549, Mar. 2004.

[17] M. M. Peretz and S. Ben-Yaakov,"Digital control of resonant converters: frequency limit cycles conditions", *IEEE Applied Power Electronics Conference, APEC-2009*, Wasington, DC, 2009.