Letters

Some Observations on Loss and Hysteresis of Ferroelectric-Based Ceramic Capacitors

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***Abstract*—Applying the observed frequency dependence of the equivalent series resistance of ferroelectric-based ceramic capacitors, the value of a parallel resistor that models the losses is extracted for small signal excitation. The result is then used to develop a loss equation of the studied ceramic capacitors, which is found to conform to the Steinmetz equation template. This leads to the conclusion that the small signal hysteresis curves of ferroelectric-based ceramic capacitors do not change with frequency. Based on the derived equations, a figure of merit is proposed to ease the comparison of ferroelectric capacitors with respect to losses.**

***Index Terms*—Ceramic capacitors, dielectric devices, dielectric losses, Steinmetz equation.**

I. Introduction

CERAMIC capacitors (CC) are widely used in the design of switch mode power conversion systems. Particularly popular are the CCs that are built around a ferroelectric dielectric (FDCC, labeled in the industry as class II and class III capacitors), since the high dielectric constant makes it possible to manufacture units of high capacitance in small size, especially when the multilayer structure (MLCC) is used. Furthermore, the FDCCs are relatively inexpensive, which makes them compatible with demanding cost-sensitive designs.

As is the case with other electronic devices, designers and researchers rely on the data that manufacturers supply in the so-called "data sheets." Unfortunately, the data provided by the FDCC manufacturers are meager [1]. The objective of this letter is to show how the available data can still be used to infer about some key attributes of FDCCs. The analysis, presented here, assumes small signal sinusoidal excitation of the FDCC such that both the voltage and current can be assumed to be sinusoidal. The FDCCs capacitance is voltage dependent, and hence, large signals will cause distortion [2]. Further research is clearly needed to explain the large signal behavior of the FDCCs.

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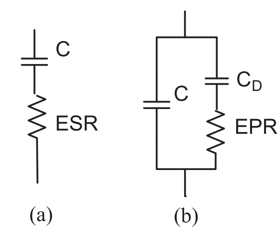


Fig. 1. FDCC loss model. (a) Conventional ESR model. (b) Proposed EPR model.

II. Equivalent Series Resistor (ESR)

The classical model of CC losses [see Fig. 1(a)] includes a capacitor and an equivalent series resistor (ESR), which, in the case of FDCCs, is temperature dependent. A cursory examination of the data given by vendors reveals that for most FDCC devices, the typical ESR–frequency dependence is similar to the one shown in Fig. 2(a) (other ESR–frequency profiles are discussed below).

Fig. 2(a) reveals that for the most part, the ESR's drop is inversely proportional to frequency until it levels off to the minimum value ESR_0. Beyond the latter point, the ESR increases. This high frequency range, which is ignored here, is of less importance in most applications since the behavior of the CC is inductive there. The frequency profile of the ESR [see Fig. 1(a)] suggests that the ESR–frequency function can be fitted to an expression of the form

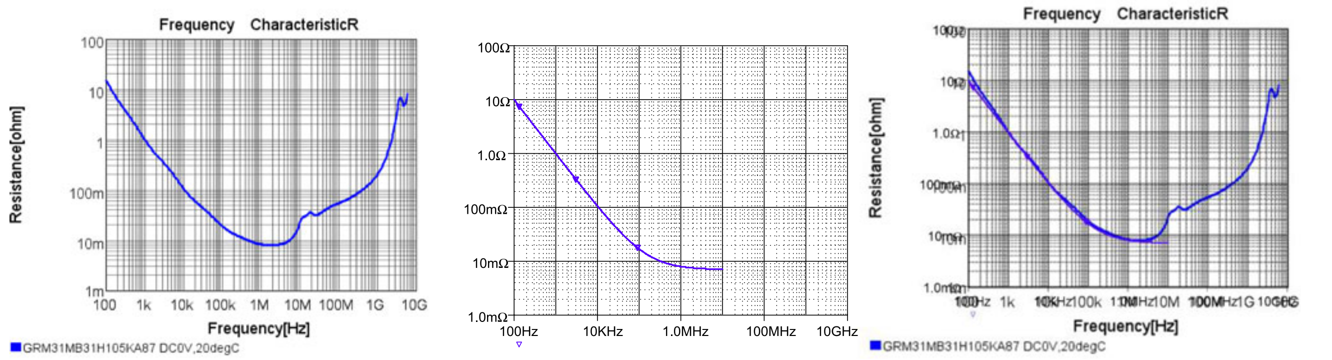
$$\mathrm{ESR} = \frac{K_s}{f} + \mathrm{ESR}_0 \tag{1}$$

where f is the frequency and K_s is a constant ($\Omega\cdot$Hz).

Fitting (1) to the data of Fig. 2(a) results in $K_s = 1\,\mathrm{k}\Omega\cdot\mathrm{Hz}$ and $\mathrm{ESR}_0 = 7\,\mathrm{m}\Omega$. The reconstructed ESR–frequency curve [see Fig. 2(b)] is in excellent agreement with the original curve, as can be attested by placing one over the other [see Fig. 2(c)].

III. Equivalent Parallel Resistor (EPR)

The underlining assumption of the common ESR model is that the losses are a function of the FDCC current. It is well established thought that dielectric losses are a function of the electric fields, and hence the voltage across the FDCC. Hence, a more proper way, from the theoretical point of view, will be



(a) (b) (c)

Fig. 2. ESR versus frequency behavior of a commercial FDCC (Murata GRM31MB31H105KA87). (a) Graph from Murata data sheet. (b) Reconstructed graph by (1). (c) To show the excellent accuracy of fitting, (b) placed on the top of (a).

to represent the losses by an equivalent parallel resistor (EPR), as depicted in Fig. 1(b). The parallel model includes a capacitor C_D for blocking the dc voltage since the losses are evidently a function of the ac component. The value of C_D should be such that the voltage drop across it, at the frequency range of interest, is much smaller than the drop on the EPR. Assuming a sinusoidal excitation, the value of the EPR can be found by equating the power P_C dissipated by ESR_C to the power dissipated by EPR_C

$$P_C = I_{C\mathrm{rms}}^2 \mathrm{ESR}_C = I_{C\mathrm{rms}}^2 \left(\frac{K_s}{f} + \mathrm{ESR}_0\right) = \frac{V_{C\mathrm{rms}}^2}{\mathrm{EPR}_C} \quad (2)$$

where $I_{C\mathrm{rms}}$ is the capacitor's current and $V_{C\mathrm{rms}}$ is the voltage across the capacitor. This equation assumes that the voltage drop across the ESR is small as compared to the voltage drop across the capacitor considering the fact that the dissipation factor (DF) of the capacitor: $\mathrm{DF} = \omega C \cdot \mathrm{ESR} \ll 1$. For example, for the Murata GRM31MB31H105KA87 examined, DF (1 kHz) = 0.6% and DF (1 MHz) = 0.7%.

Also

$$I_{C\mathrm{rms}} = 2\pi f C V_{C\mathrm{rms}} \quad (3)$$

where C is the capacitance of the capacitor C.

Plugging (3) into (2) and solving for the EPR

$$\mathrm{EPR}_C = \frac{1}{(2\pi f C)^2 \left(\frac{K_s}{f} + \mathrm{ESR}_0\right)}. \quad (4)$$

The power loss P_C of the capacitor is found from (2) and (3)

$$P_C = (2\pi C)^2 \left(f K_S + f^2 \mathrm{ESR}_0\right) V_{C\mathrm{rms}}^2. \quad (5)$$

An alternative derivation of (5) is presented in the Appendix.

For the frequency range in which the ESR drops monotonically with frequency [see Fig. 1(a)], the second term in the parentheses of (5) can be neglected and the power loss P_{Cf} can be expressed as a dual to the Steinmetz equation [3]

$$P_{Cf} = K_p f^1 V_{C\mathrm{rms}}^2 \quad (6)$$

where $K_p = (2\pi C)^2 K_S$.

K_p can, thus, be considered as a figure of merit that can help in the comparison of FDCCs of different capacitance, within a given family, and to compare families of FDCCs with respect to power loss.

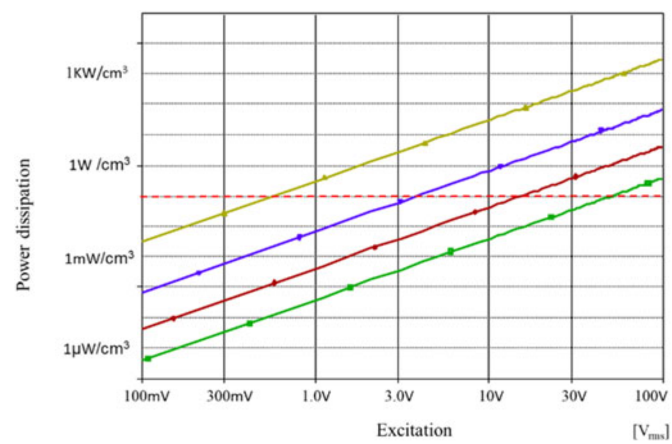


Fig. 3. Power loss (vertical axis) of the FDCC of Fig. 2(a) (Murata GRM31MB31H105KA87), as a function of excitation voltage V_{rms} (horizontal) with frequency as a parameter generated from (5). Curves are for (from top to bottom) 1 MHz, 100 kHz, 10 kHz, and 1 kHz. The dashed horizontal line represents a power dissipation limit of 100 mW.

Based on (5) a parametric plot can be generated to describe the capacitor losses, similar to the way ferrite core losses are normally presented by manufacturers (see Fig. 3). It should be noted that thermal conduction of the FDCC limits the allowable power dissipation of the device to about 100 mW.

IV. Hysteresis

There are few studies on the hysteresis of FDCC, but the question of how the hysteresis curve changes with frequency is still unanswered [1]. Based on the expression of the FDCC EPR developed above, this question can now be answered: *the hysteresis curve of FDCC does not change with frequency.* This is correct for the portion of the ESR–frequency curve, which can be expressed as K_s/f [see Fig. 1(a)]. The rationale of this conclusion is as follows. Given a generic hysteresis curve of an FDCC, the energy lost per cycle E_C is proportional to the area

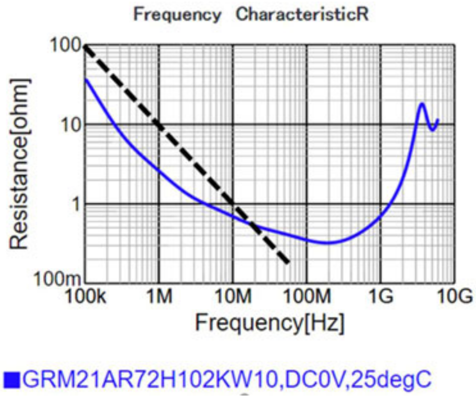


Fig. 4. ESR versus frequency behavior FDCC (Murata) in which the drop of the ESR is monotonic with frequency. Dashed line represents a 1/*f* slope.

encircled by the curve. The power loss per second will, thus, be $E_C f$. That is, the power loss is proportional to the frequency of excitation. Equating $E_C f$ with (6), which expresses the power loss of the FDCC for the frequency range under discussion, yields

$$E_C = (2\pi C)^2 K_S V_{C\mathrm{rms}}^2. \quad (7)$$

This implies that, for a fixed excitation amplitude $V_{C\mathrm{rms}}$, the hysteresis curve is independent of frequency.

V. Nonmonotonic Slope of the ESR

A cursory search reveals that there are few (perhaps in the range of 5%) commercial FDCCs that exhibit a nonmonotonic drop of the ESR with frequency. An example is shown in Fig. 4. In this case, the fitting to (1) cannot be made for the full range. Furthermore, the exponent of *f* in the Steinmetz equation template (6) will not be one for some of the segments. This type of behavior is found also in a ferromagnetic material, and hence, the manufacturer provides a set of Steinmetz constants, to cover the full frequency range of interest [4]. This behavior was also found in the output capacitance of MOSFET transistors [5].

VI. Conclusion

The analysis presented in this letter shows that the losses of FDCCs can be modeled by an EPR, which is linearly dependent on the excitation frequency when the ESR drops monotonically with frequency. It was also found that power loss of the FDCC can be expressed by a dual Steinmetz equation and that the shape of the hysteresis curve of FDCC that exhibits a monotonic drop with frequency is independent of frequency. Based on the presented analysis, a figure of merit K_S can be defined to ease the comparison between FDCC with respect to losses. As much that the loss of an FDCC can be calculated by either applying the ESR and the current through the capacitor or by the voltage across the capacitor and EPR_C, the latter approach could provide a more intuitive understanding of the FDCC loss. For example, examination of Fig. 3 gives a clear picture of FDCC losses due to a voltage ripple.

FDCC losses are due to dielectric losses and contact resistance losses. The fact that the calculated losses follow Steinmetz equation template (6), which assumes only dielectric losses, may suggest that the contact resistance losses are small compared to the dielectric losses in the studied device.

The focus of this letter is the ESR behavior up to the resonant frequency and as such does not include inductive elements. A comprehensive, 19 parameters EPR-based model that covers also the frequency range above the resonant frequency was presented in [6]. That model is based on curve fitting and does not reveal the relationship between the EPR and ESR.

Appendix
Alternative Derivation of the EPR

The following derivation alternative was suggested by one of the reviewer of this letter, for which the author is thankful.

The total power of the FDCC is

$$P_c(j\omega) = \frac{V_{\mathrm{rms}T}^2}{\frac{1}{j\omega C} + \mathrm{ESR}} = \frac{V_{\mathrm{rms}T}^2 j\omega C\,(1 - j\omega C \cdot \mathrm{ESR})}{1 + (\omega C \cdot \mathrm{ESR})^2} \quad (8)$$

where $v_{\mathrm{rms}T}$ is the voltage across the capacitor and ESR assembly [see Fig. 1(a)].

Assuming as aforementioned that $\mathrm{DF} = \omega \cdot \mathrm{ESR} \cdot C \ll 1$, and therefore $V_{\mathrm{rms}T} \approx V_{C\mathrm{rms}}$ and $(\omega C \cdot \mathrm{ESR})^2 \ll 1$

$$\begin{aligned}\mathrm{Re}(P_c(j\omega)) &= V_{C\mathrm{rms}}^2 (2\pi f)^2 C^2 \cdot \mathrm{ESR} \\ &= (2\pi C)^2 \left(f K_S + f^2 \mathrm{ESR}_0\right) V_{C\mathrm{rms}}^2 \quad (9)\end{aligned}$$

which is equal to (5).

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