

# An RC Logarithmic Converter-Digitizer

SHMUEL BEN-YAAKOV AND JACOB CHEN

**Abstract**—Theoretical considerations and experimental data support the suggestion that high accuracy of conversion and long-term stability could be obtained with a logarithmic RC converter-digitizer. The operation of the proposed converter is based on time measurements of the exponential voltage decay across a linear RC network. Linearity error of this converter, built with commonly available and noncritical components, was found to be less than 0.05 percent of full scale for a two-decade operation.

## I. INTRODUCTION

APPLICATIONS of logarithmic amplifiers fall into two groups: (a) applications which use the log function for data compression and (b) those which require a logarithmic function for linearization or unit conversion. As an example of the second group, consider a spectrophotometer which produces an output signal  $e$ :

$$e = A \exp(-\epsilon \cdot d \cdot c) \quad (1)$$

where  $A$  is a constant,  $\epsilon$  the extinction coefficient,  $d$  the optical path, and  $c$  the concentration of the unknown. Hence the unknown can be obtained by a logarithmic conversion of the output signal  $e$ , thereby linearizing the measurement.

The basic requirement of applications of the first group (compression) is a large dynamic range, i.e., the ability to compress many decades of the input signal. On the other hand, applications of the second group (linearization) call for high accuracy and long-term stability of conversion.

For applications of the first group, Paterson's [1]–[3] transdiode connection is an optimal solution as it provides a dynamic range of up to 7 decades. However, poor long-term stability and temperature dependence of BJT transistor parameters deteriorate the performance of this log converter. In this respect, the transdiode connection is not the optimal solution for applications of the second group, which often do not call for wide dynamic range. For these applications, we propose a logarithmic converter based on the exponential decay of a linear RC network. The approach combines both log conversion and digitization and is thus applicable in digital readouts for instrumentation which require log conversion.

Manuscript received November 12, 1976.

The authors are with the Department of Electrical Engineering, Ben Gurion University of the Negev, Beer-Sheva 84120, Israel.

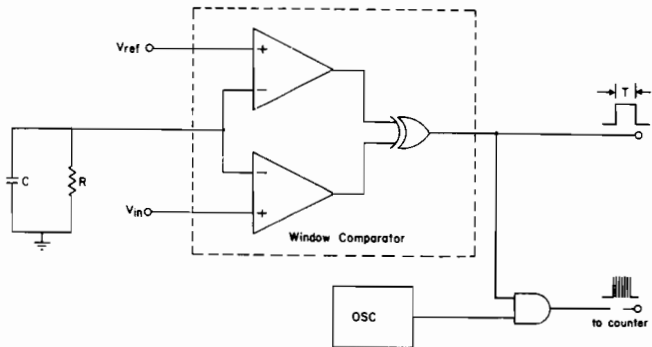


Fig. 1. Basic configuration of proposed log converter/digitizer.

## II. THEORETICAL

Consider a discharging RC network. The voltage across the capacitor is described by

$$V = V_0 \exp(-t/RC). \quad (2)$$

If this voltage is fed to a window comparator (Fig. 1), with reference levels  $V_{ref}$  and  $V_{in}$ , the pulsewidth  $T$  at the output will be

$$T = RC \left| \ln \frac{V_{in}}{V_{ref}} \right|. \quad (3)$$

Digitization is accomplished by gating a stable oscillator with this pulse (Fig. 1).

The conversion error of the proposed log converter/digitizer depends on three factors: (a) stability of the RC network, (b) stability of the oscillator, and (c) errors due to the nonideality of the comparators. Of these, only factor (c) will cause deviation of the conversion from the log function.

The offset error of the window comparator would modify the transfer function (3) to:

$$T' = RC \ln \left| \frac{V_{in} + \Delta_1}{V_{ref} + \Delta_2} \right| \quad (4)$$

where  $\Delta_1$  and  $\Delta_2$  are the equivalent offset voltage errors including errors due to input bias current. Redefining the reference voltage  $V'_{ref}$  as  $V_{ref} + \Delta_2$  one obtains:

$$T' = RC \left| \ln \frac{V_{in} + \Delta_1}{V'_{ref}} \right|. \quad (5)$$

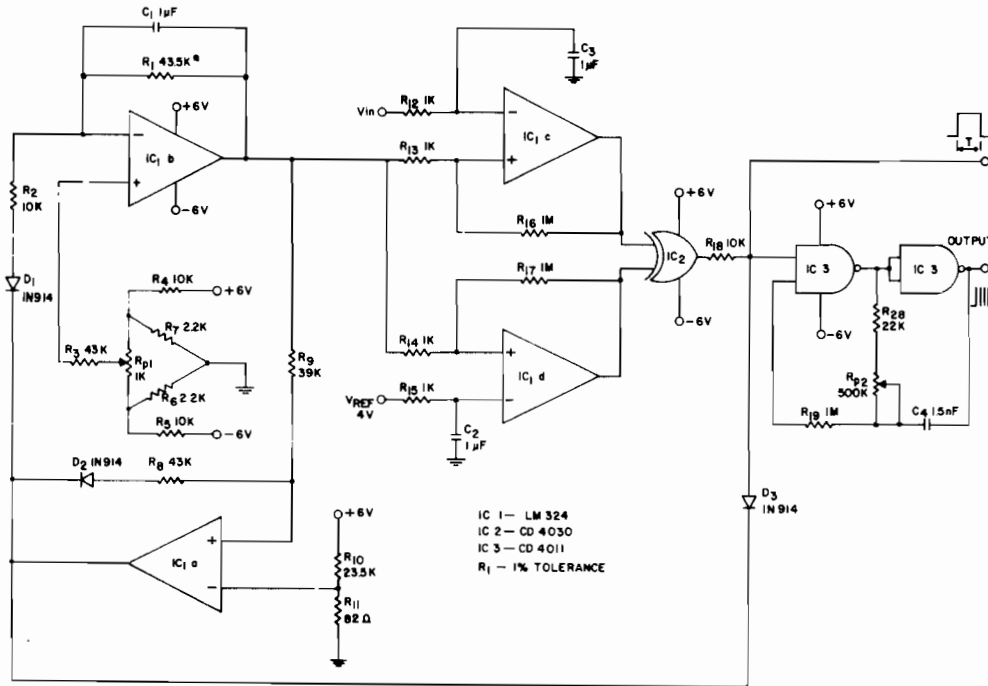


Fig. 2. Circuit diagram of the log converter-digitizer tested during study.

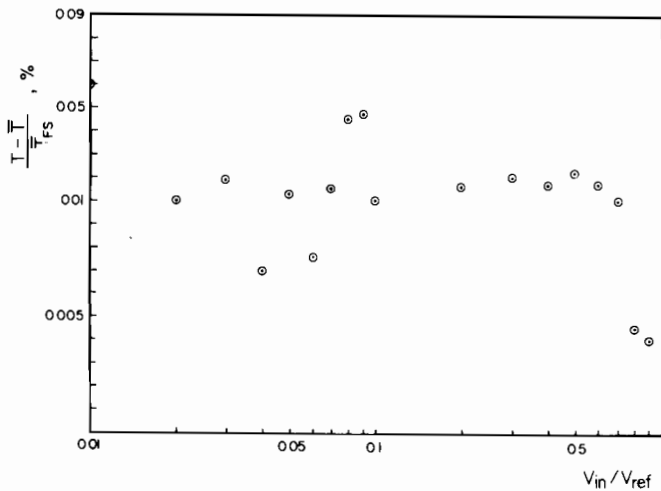


Fig. 3. Conversion error of log converter-digitizer of Fig. 2. Errors are expressed as percent deviation from best fit line—relative to full scale. Full scale taken as two decades.

For any given  $V_{in}$ , the relative error  $ER$  at the output is

$$ER = \frac{T' - T}{T} = \left| \frac{\ln(1 + \Delta_1/V_{in})}{\ln(V_{in}/V_{ref})} \right| \quad (6)$$

which, for  $\Delta_1 \ll V_{in}$ , reduces to

$$ER = \left| \frac{\Delta_1/V_{in}}{\ln(V_{in}/V_{ref})} \right| \quad (7)$$

An appreciation for the expected error can be given by considering a two-decade converter for inputs between 10 and 0.1 V and with an equivalent offset voltage error of 1 mV. We assume  $V_{ref}$  to be set to 10 V. The error for the 10-V input is calculated to be approximately 0.002 percent

of full scale (2 decades) whereas the error for 0.1-V input is approximately 0.2 percent of full scale.

### III. EXPERIMENTAL RESULTS

The proposed log converter/digitizer was realized using a quad operational amplifier and CMOS logic (Fig. 2). The RC network ( $R_1, C_1$ ) is first charged through  $R_2$  and after reaching the trigger level of the toggle ( $A$ ), is left to discharge. The output pulse at the output of the window comparator controls a gated CMOS oscillator [4] producing the desired pulse train. The combined dc offset error of amplifiers  $B$  and  $C$  is zeroed by the offset adjust  $R_{p1}$ .

Using a nominal value of 4 V for  $V_{ref}$ , the linearity over two decades (4 to 0.04 V) was measured. The data were then fitted by the least square method to the function:

$$T = a \ln(V_{in}/V_{ref}) + b. \quad (8)$$

Deviation of the experimental data points ( $T$ ) from the calibration curve ( $\bar{T}$ ) thus obtained are plotted versus  $V_{in}/V_{ref}$  (Fig. 3). It is evident that the maximum error of conversion over two decades was less than 0.05 percent of full scale.

### IV. CONCLUSIONS

The present study suggests that an RC log converter-digitizer should be seriously considered in applications calling for high accuracy of conversion. The converter has distinct advantages over Paterson's transdiode configuration in cases which do not require a large dynamic range. Unlike the transdiode, this converter is essentially insensitive to temperature except for normal temperature errors common to all analog electronic circuits. These include

temperature effects on stability of components and offset drift of operational amplifiers and comparators. One would expect, therefore, that by properly selecting the electronic components, temperature dependence and long-term stability could be maintained at a level comparable to those achieved in commonly used linear digitizers. Since the complexity of the electronic circuit proposed here is comparable to that of linear digitizers [5], the realization of a log converter-digitizer by the proposed method should be more economical than cascading a transdiode log converter and a linear digitizer.

## REFERENCES

- [1] W. L. Paterson, "Multiplication and logarithmic conversion by operational amplifier-transistor circuits," *Rev. Sci. Instrum.*, vol. 34, pp. 1311-1316, Dec. 1963.
- [2] M. V. Šobajić, "A possibility of simultaneous logarithmic-linear direct-current measurement," *IEEE Trans. Instrum. Meas.*, vol. IM-25, no. 1, pp. 34-43, Mar. 1976.
- [3] A. R. Risley, "Designers guide to: Logarithmic amplifier," *EDN*, Aug. 1973.
- [4] RCA Solid State, *COS/MOS Integrated Circuits*. SSD-203C, pp. 531-538, 1975 data book.
- [5] Analog Devices, *Analog-Digital Conversion Handbook*. Analog Devices Inc., MA, 1972.

