A Resonant DC-DC Transformer

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The characteristics of a push-pull parallel resonant converter (PPRC) when operated as a dc-dc transformer were investigated theoretically and experimentally. In the dc-dc transformer region, the voltage transfer ratio of the PPRC was found to be practically constant and independent of the input voltage and load. In this mode, all the switching elements operate in the zero voltage switching (ZVS) condition. Another important feature of the proposed dc-dc transformer is the ability to drive it by an arbitrary switching frequency, provided that it is lower than the self-oscillating frequency. This permits the synchronization of the converter to a master clock. The analytical expressions for voltage and current stresses as well as other key parameters, derived in the paper, are applied to develop design guidelines for the dc-dc transformer. The proposed topology was tested experimentally on a 100 W unit which was run at the 200 KHz frequency region.

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I. INTRODUCTION

High frequency (HF) dc-dc links [1] are widely used in many practical applications. They are applied to convert voltage levels of primary power sources to desirable output voltages and many times to isolate the load side from the ground of the primary power input. HF links can be divided into two basic groups, controllable conversion ratio converters, and dc-dc transformers that provides a constant conversion ratio and isolation, if required.

DC-DC transformers have some advantages over the controllable converters. Hardware simplicity, robustness and a constant electromagnetic interference (EMI) spectrum which is practically independent of the input voltage and output loading, are some of the reasons that a designer might prefer a multiple output dc-dc transformer over a controlled converter. These advantages are enhanced if high conversion efficiency can be realized at a high operating frequency. Such dc-dc transformers can conveniently be used as primary power conditioners and isolators. High frequency of operation permits reduction of the volume and weight of the units to comply with stringent size requirements. Output voltage stabilization can then be carried out independently on each output by a linear or switching regulator such as a Magamp. This concept is not new and has been described and applied in the past. However, previous dc-dc transformers were based on a square-wave modulator such as the classical saturable core power oscillator [2, 3] or the conventional pulsewidth modulation (PWM) power stage.

The objective of the present study is to investigate the characteristics of a push-pull parallel resonant converter (PPRC) when applied as an HF link. This topology is of interest because it has many attractive features such as zero voltage switching (ZVS) and the ability to be synchronized to an external frequency source. Indeed, the results of this investigation suggest that the PPRC is an excellent candidate for realizing constant ratio dc-dc transformers. The proposed approach is similar to the one discussed in [4]. However, we propose a system with a simple square-wave drive rather than the overlapping driving pulses discussed in [4]. Furthermore, our study is specifically focused on dc-dc applications whereas in [4] the authors addressed themselves to the problem of transfer ratio control. The present study is similar, and in fact an extension, of a previous investigation [5] in which a self-oscillating power stage was examined.

II. PPRC TOPOLOGY AND WAVEFORMS

The PPRC power stage (Fig. 1) is built around a push-pull configuration (Q1, Q2), an input inductor (L_{in}), and a resonant network (L_r, C_r). The power stage is driven by a symmetrical square wave (f_S).

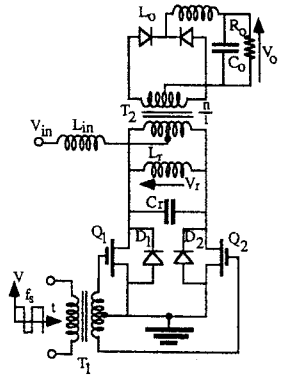


Fig. 1. Proposed PPRC-based dc-dc transformer.

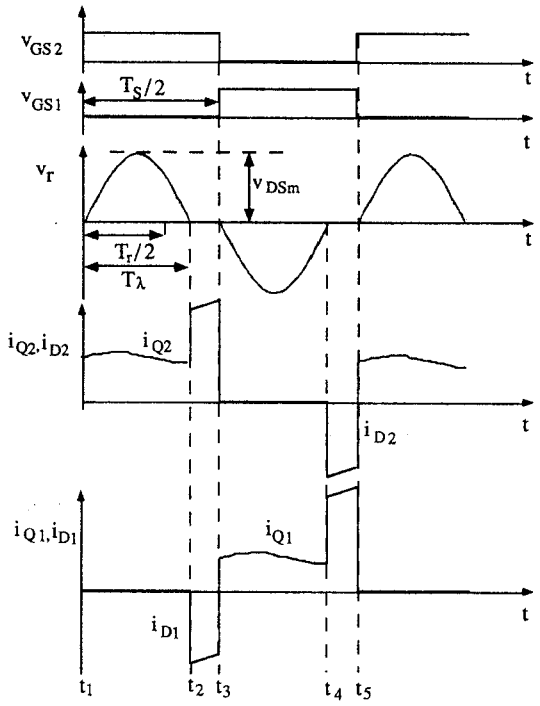


Fig. 2. Basic waveforms of PPRC when operated in dc-dc transformer region.

The signal generated by the power stage is coupled to the secondary side via an isolating transformer (T2), rectified, and filtered by an LC filter (L_0, C_0). Rectification can be carried out by a bridge rectifier or a center-tapped full-wave rectifier as shown.

Steady State Operation: The steady state voltage and current waveforms when the PPRC (Fig. 1) is operated in the dc-dc transformer region are depicted in Fig. 2. The operation of the converter is discussed here by examining the tank voltage (v_r), the drain to source voltage of the transistors (v_{DS}), the drain currents of the transistors (i_Q), and the current of the clamp diodes (D_1, D_2) (i_D), in relation to the gate to source voltages (v_{GS}). Assuming that v_{GS1} goes low and v_{GS2} goes high at t_1 (Fig. 2), v_{DS2} is forced to zero and the tank voltage (v_r) (which is also v_{DS1}) starts to rise in a quasi-sinusoidal shape. When this voltage waveform passes back through zero toward a negative

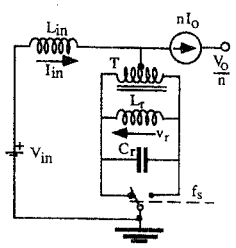


Fig. 3. Generic topology of PPRC in steady state.

value (at t_2), diode D_1 starts conducting, shorting the tank (L_r, C_r) as well as the primary of T2. At t_3, when v_{GS2} goes low, the tank voltage and v_{DS2} starts to rise, repeating the waveforms of the first half cycle. For each half cycle we thus recognize two distinct states, the quasi-resonant period ($T_\lambda = t_2 - t_1$) and the boost period ($t_3 - t_2$). During the quasi-resonant period, power is delivered to the isolated side and the wave shape of the secondary voltage follows that of a quasi-sinusoidal wave shape. During the boost period the resonant tank and the primary of T2 are shorted through a transistor and a diode (which is in parallel to the opposing transistor) and the input inductance (L_{in}) is charged by the power source.

The waveforms of Fig. 2 clearly demonstrate the important fact that, in this continuous current mode (CCM) operational mode, all the switching elements (the transistors, diodes and rectifiers) operate under ZVS condition independent on the power level. To ensure this, the quasi-resonant duration (T_λ) should be shorter then half the driving frequency period ($T_S/2$). That is

$$T_\lambda < \frac{T_S}{2}. \tag{1}$$

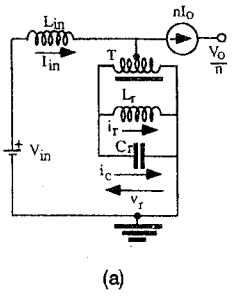
Analytical expressions of the basic parameters of the PPRC were developed under the assumptions that the switches, diodes, rectifiers, and transformer are ideal, that the reflected inductance of L_0 (which is equal to L_0/n^2, where (n) is the transformer ratio) (Fig. 1), is much larger than the tank inductance and that the parasitic inductances and capacitances are negligible small. The generic topology of the PPRC in steady state conditions can be represented by the simplified equivalent circuit of Fig. 3. The current source reflects the assumption that the inductor of the output filter is much larger than the inductance of the tank.

Quasi Resonant State: Under the above assumptions, the relevant network for the quasi-resonant period ($T_\lambda = t_2 - t_1$; Fig. 2) is that of Fig. 4(a). For this period:

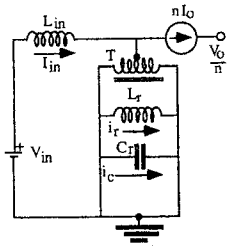
$$V_{in} = L_{in}\frac{di_{in}}{dt} + \frac{1}{2}L_r\frac{di_r}{dt} \tag{2}$$

$$v_r = L_r\frac{di_r}{dt} = \frac{1}{C_r}\int i_c\,dt \tag{3}$$

$$\frac{i_{in}}{2} = i_r + i_c + \frac{nI_0}{2}. \tag{4}$$



(a)



(b)

Fig. 4. Equivalent circuit for (a) quasi-resonant period and (b) for boost period.

By combining the above equations one gets

$$\frac{d^2v_r}{dt^2} + \frac{1+b}{L_rC_r}v_r = \frac{2bV_{\text{in}}}{L_rC_r} \tag{5}$$

where $b = L_r/4L_{\text{in}}$.

The general solution of (5) has the form:

$$v_r = A_1\sin(\omega_r t) + A_2\cos(\omega_r t) + 2V_{\text{in}}\frac{b}{1+b} \tag{6}$$

where $\omega_r = \sqrt{(1+b)/(L_rC_r)}$ is the resonant frequency of the charging current of the capacitor. The integration constants are found by the initial and final conditions constraints which require that $v_r = 0$ at $t = 0$ and when $t = T_\lambda$ (Fig. 2). By applying these relationships we obtain the normalized tank voltage (v_r^*):

$$v_r^* = \frac{v_r}{2V_{\text{in}}} = -\frac{b}{1+b}\left[\frac{1-\cos(\vartheta_\lambda)}{\sin(\vartheta_\lambda)}\sin\vartheta + \cos\vartheta - 1\right] \tag{7}$$

where $\vartheta = \omega_r t$ and $\vartheta_\lambda = \omega_r T_\lambda$.

The quasi-resonant duration (T_λ) is found by applying the fact that in steady state conditions, the average voltage (per cycle) across L_{in} is zero:

$$\frac{T_S}{2}V_{\text{in}} - \frac{1}{2}\int_0^{T_S/2} v_r\,dt = 0 \tag{8}$$

and since $v_r = 0$ for $T_\lambda < t < T_S/2$:

$$\frac{2}{\omega_r T_S}\int_0^{\vartheta_\lambda} v_r\,d\vartheta = 2V_{\text{in}}. \tag{9}$$

By combining (7) and (9) we find

$$\frac{\pi T_S}{T_r}\frac{1+b}{b} - \vartheta_\lambda = -2\tan\left(\frac{\vartheta_\lambda}{2}\right). \tag{10}$$

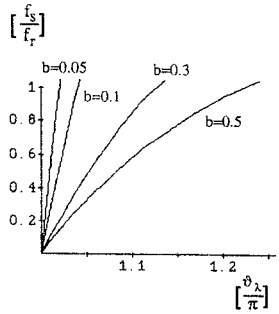


Fig. 5. Relationship between normalized quasi-resonant phase ($\vartheta_\lambda = \omega_r T_\lambda$) and switching frequency ratio ($f_S/f_r = T_r/T_S$) as function of inductance ratio parameter ($b = L_r/4L_{\text{in}}$).

This expression determines the dependence of the quasi-resonant phase (ϑ_λ) on the circuit parameters (b,T_r) and the switching period T_S (Fig. 5). The plot of Fig. 5 implies that the quasi-resonant duration (T_λ) is not only a function of ω_r (the resonant frequency) but also of the inductances ratio (b). However, when the reflected input inductance ($4L_{\text{in}}$) is sufficiently larger than the resonant inductance (L_r), the parameter (b) will be much smaller than unity and the quasi-resonant duration (T_λ) approaches half the natural resonant period (T_r). In general however:

$$T_\lambda > \frac{T_r}{2}. \tag{11}$$

It should be noted that T_λ is not a function of the load as long as the output current can be assumed to be continuous and smoothed by an output inductor (L_0), which is much larger than the tank inductance (L_r) and associated leakage inductances.

DC-DC Transfer Ratio: Aside from the desirable characteristics of ZVS, the ideal PPRC is found to have a constant input-output transfer ratio (M) independent of the switching frequency (f_S). This is a result of the fact that the averaged (dc) output voltage is a linear function of the average voltage developed at the center tap of T2 (Fig. 1). Since the latter is equal to the input voltage (equation (8)), the voltage transfer ratio (M) is identical to the transformer turns ratio:

$$M = \frac{V_0}{V_{\text{in}}} = n. \tag{12}$$

It should be emphasized that this transfer ratio is independent of the load and on the switching frequency (f_S) if the conditions of (1) are met and the current of the output inductance (L_0) is continuous (see below).

Output Filter Inductor (L_0): An output discontinuous conduction mode (DCM) prevails when the output current is insufficient to ensure forward conduction when the current ripple is high. The criterion for CCM boundary can be evaluated by comparing the dc output current to the current ripple of (L_0). The latter is a function of the average output voltage (V_0) and the reflected voltage across

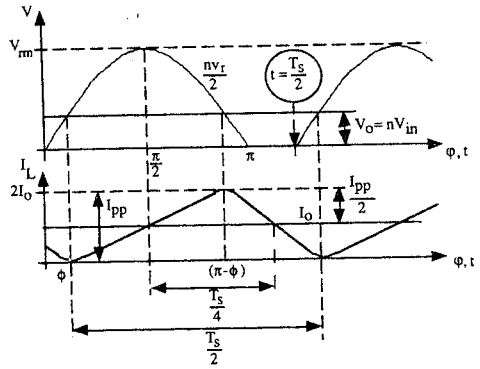


Fig. 6. Terminal voltages (upper trace) and current (lower trace) of output filter inductor (L_0).

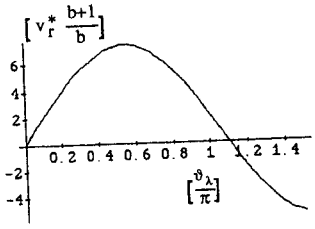


Fig. 7. Trigonometric function of (7) for $\vartheta_\lambda/\pi = 1.1$.

the tank (Fig. 6). The following derivation of the ripple component is based on the fact that the current rising edge is a function of the voltage across (L_0) during the interval $\{(\pi-\phi)-\phi\}$. If the reflected input inductance ($4L_{in}$) is appreciably larger than the resonant inductance (L_r), the parameter (b) is much smaller than unity. Under this condition, the trigonometric function of (7) is close to a sinusoidal function (Fig. 7). It is assumed therefore in the followings, that this voltage waveform can be represented by the approximate expression:

$$v_r = V_{rm}\sin(\varphi) \tag{13}$$

where $\varphi = (\pi/T_\lambda)t$. The sinusoidal voltage at the output side (v_S) is

$$v_S = \frac{nv_r}{2} = \frac{nV_{rm}\sin(\varphi)}{2}. \tag{14}$$

The approximate peak voltage of the tank (V_{rm}) can be derived by substituting the relationship of (13) into the integral relationship of (9):

$$V_{rm} = \pi V_{in}\frac{T_S}{2T_\lambda}. \tag{15}$$

At the boundary between CCM and DCM, the peak-to-peak ripple current is equal to twice the output current (I_0) (Fig. 6):

$$\frac{1}{\frac{\pi}{T_\lambda}L_0}\int_\phi^{\pi-\phi}\left[\frac{n\pi V_{in}}{2}\frac{T_S}{2T_\lambda}\sin(\varphi)-nV_{in}\right]d\varphi = 2I_0 = 2n\frac{V_{in}}{R_0} \tag{16}$$

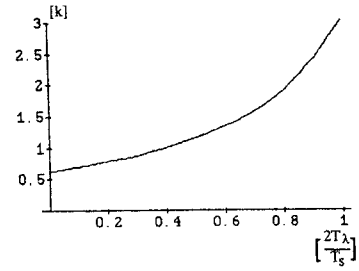


Fig. 8. Relationship between factor (k) (22) and quasi-resonant period ratio $[2T_\lambda/T_S]$.

where the intersection angle (ϕ) is the point at which the voltage across (L_0) is zero:

$$\frac{n\pi V_{in}}{2}\frac{T_S}{2T_\lambda}\sin(\phi) = nV_{in}. \tag{17}$$

Hence:

$$\phi = \sin^{-1}\left(\frac{4T_\lambda}{\pi T_S}\right). \tag{18}$$

Symmetry considerations permit rewriting of (16) as

$$\frac{1}{\frac{\pi}{T_\lambda}L_0}\int_\phi^{\pi/2}\left[\frac{\pi T_S}{4T_\lambda}\sin(\varphi)-1\right]d\varphi = \frac{1}{R_0} \tag{19}$$

and after evaluating the integral:

$$\frac{1}{\frac{\pi}{T_\lambda}L_0}\left[\frac{\pi T_S}{4T_\lambda}\cos(\phi)-\left[\frac{\pi}{2}-\phi\right]\right] = \frac{1}{R_0} \tag{20}$$

which implies that the condition for CCM in the output filter inductor is

$$R_0 \le k2\pi f_S L_0 \tag{21}$$

where

$$k = \frac{\frac{T_S}{2T_\lambda}}{\left[\frac{\pi T_S}{4T_\lambda}\cos(\phi)-\left[\frac{\pi}{2}-\phi\right]\right]}. \tag{22}$$

From the functional relationship between (k) and ($T_S/2T_\lambda$), (Fig. 8), it is evident that the worst case is covered if $R_0 \le \pi f_S L_0$.

Output Filter Capacitor (C_0): The dependence of output voltage ripple on the output capacitor (C_0) is derived under the assumption that the current ripple of (L_0) can be approximated by a triangle (Fig. 6). The peak-to-peak magnitude of this ripple current (I_{pp}) is given by the left side of (16):

$$I_{pp} = \frac{1}{\frac{\pi}{T_\lambda}L_0}\int_\phi^{\pi-\phi}\left[\frac{n\pi V_{in}}{2}\frac{T_S}{2T_\lambda}\sin(\varphi)-nV_{in}\right]d\varphi. \tag{23}$$

Hence:

$$I_{pp} = \frac{V_0}{\frac{\pi}{T_\lambda}L_0}\left[\frac{\pi}{2}\frac{T_S}{2T_\lambda}\cos(\phi)-\left[\frac{\pi}{2}-\phi\right]\right]. \tag{24}$$

Applying the definition of (k) given by (22):

$$I_{pp} = \frac{V_0 T_S}{2\pi L_0 k}. \tag{25}$$

The peak-to-peak output voltage ripple (V_{pp}) can be expressed as

$$V_{pp} = \frac{\Delta Q}{C_0} \tag{26}$$

where ΔQ is the ripple charge increment. This relationship assumes that the impedance of (C_0) at frequencies above (f_S) is much smaller than (R_0) as would be in practical cases.

The approximate expression for (ΔQ) under the assumption of a triangular ripple current (Fig. 6) is

$$\Delta Q = \frac{\frac{I_{pp}}{2}\frac{T_S}{4}}{2} = \frac{I_{pp} T_S}{16}. \tag{27}$$

Or (from (25)):

$$\Delta Q = \frac{V_0}{32\pi f_S^2 L_0 k} \tag{28}$$

which implies

$$C_0 > \left(\frac{V_0}{V_{ppm}}\right)\left(\frac{1}{32\pi f_S^2 L_0 k}\right) \tag{29}$$

where V_{ppm} is a given upper limit of V_{pp}. Since the limiting value of (k) is (0.5) (Fig. 8), the worst case value of the capacitor is

$$C_0 > \left(\frac{V_0}{V_{ppm}}\right)\left(\frac{1}{16\pi f_S^2 L_0}\right). \tag{30}$$

Input Inductor (L_{in}): The terminal voltages of (L_{in}) are a mirror image the terminal voltages of (L_0) shown in Fig. 6. Consequently, the expression for the input current ripple ($I_{in_{pp}}$) can be obtained from (25) by the substitutions: $I_{pp} \rightarrow I_{in_{pp}}$; $V_0 \rightarrow V_{in}$; $L_0 \rightarrow L_{in}$, where $I_{in_{pp}}$ is the input peak-to-peak ripple current. Hence:

$$I_{in_{pp}} = \frac{V_{in} T_S}{2\pi L_{in} k}. \tag{31}$$

It should be noted that input inductor is intimately involved in the resonant process through the inductances ratio (b) as shown in Fig. 5.

Voltage Stresses: The voltage stresses of the transistor and the antiparallel diodes depend on the ratio (f_r/f_S). A decrease in the switching frequency (f_S) causes peaking of the voltage across the tank and hence across the transistors. From (15), the approximate peak voltage of the transistors (V_{DSm}) and the antiparallel diodes (V_{Dm}):

$$V_{DSm} = V_{Dm} = V_{rm} = \pi V_{in} \frac{T_S}{2T_\lambda}. \tag{32}$$

The peak voltage of the rectifier diodes (V_{DRm}) is similar to the above expression except for the added turns ratio (n) of the transformer:

$$V_{DRm} = \pi V_{in} \frac{T_S}{2T_\lambda} n. \tag{33}$$

The above equations imply that the voltage stresses are a function of the input voltage and the ratio (f_r/f_S).

The above equations imply that the voltage stresses are minimal when T_λ approaches $T_s/2$ (Fig. 2) that is, when the boost period vanishes.

Current Stress: The currents of the PPRC include three basic components: the load current, the resonant current, and the boost current. In the following we assume that the reflected inductance of the input inductor ($4L_{in}$) is much larger than the resonant inductor (L_r). Consequently, during the beginning of the quasi-resonant period (Figs. 2, 4(a)) the current of the conducting transistor is mainly that of the load (i.e., we neglect the ac component through L_{in}). For a lossless PPRC, the ratio of the dc input current (I_{in}) to the output current (I_0) is equal to the voltage transfer ratio (M):

$$\frac{I_{in}}{I_0} = M = n. \tag{34}$$

Hence:

$$I_{in} = I_0 n = \frac{V_{in}}{R_0} n^2. \tag{35}$$

At the beginning of the boost period (Figs. 2, 4(b)), the conducting transistor carries both the reflected output current and the current of the shorted resonant inductor. The magnitude of the freewheeling current of the resonant inductor (I_{rm}) can be calculated by considering the requirement that in steady state, the current must exhibit a symmetrical swing around zero level. Consequently, during each half switching cycle, the resonant-inductor current has to change from ($-I_{rm}$) to ($+I_{rm}$) while the voltage across it is v_r (equation (7)). This implies

$$I_{rm} = -I_{rm} + \frac{1}{L_r}\int_0^{T_S/2} v_r\, dt. \tag{36}$$

But since the average voltage of the tank is related to (V_{in}) by (8), we find the freewheeling peak resonant current (I_{rm}) to be

$$I_{rm} = \frac{V_{in} T_S}{2L_r} = \frac{V_{in}}{2L_r f_S}. \tag{37}$$

During the boost period ($(T_S/2) - T_\lambda$), (Figs. 2, 4(b)), the current rise in (L_{in}) is linear and at the end of this period the incremental change in the input current (ΔI_{in}) is

$$\Delta I_{in} = \frac{V_{in}}{L_{in}}\left(\frac{T_S}{2} - T_\lambda\right). \tag{38}$$

While the boost configuration persists, the input current evenly splits between the two arms of the

short (Fig. 4(b)). Consequently the maximum transistor current (I_{Qm}) is (equations (35), (37), (38)):

$$I_{Qm} = I_{rm} + \frac{I_{in}}{2} + \frac{\Delta I_{in}}{2} \tag{39}$$

$$I_{Qm} = \frac{V_{in}}{2}\left\{\frac{n^2}{R_0} + T_S\left(\frac{1}{L_r} + \frac{1}{2L_{in}}\right) - T_\lambda \frac{1}{L_{in}}\right\} \tag{40}$$

or

$$I_{Qm} = \frac{V_{in}}{2}\left\{\frac{n^2}{R_0} + \frac{T_S}{L_r}\left[1 + 2b - \frac{2T_\lambda}{T_S}2b\right]\right\}. \tag{41}$$

It should be noted that the transistors carry the resonant current only during the boost period ($(T_S/2) - T_\lambda$). That is, if the switching frequency (f_S) is chosen to be only slightly lower than that of the quasi-resonant frequency ($1/(2T_\lambda)$), the transistors will carry the resonant current only during a relatively short period of time. This helps to reduce the conduction losses of the PPRC-based dc-dc transformer.

The maximum antiparallel diodes current (I_{Dm}) prevails at the no-load condition and will thus be equal to the maximum freewheeling current (equation (37)):

$$I_{Dm} = V_{in}\frac{1}{2f_S L_r}. \tag{42}$$

Since the current of the rectifying diodes is that of the load, the current stress (I_{DRm}) is the load current:

$$I_{DRm} = I_0 = \frac{V_{in}}{R_0}n. \tag{43}$$

III. RESULTS AND DISCUSSION

The experimental PPRC had the following nominal parameters.

$n = 1$; $L_r = 31\ \mu$H; $L_{in} = 68\ \mu$H; $\rightarrow b = 0.11$.

$C_r = 16.2$ nF $\rightarrow f_r = 237.41$ KHz.

The switching frequency (f_S) was in the range 140 KHz to 180 KHz.

The quasi-resonant period (T_λ) was found to be 2.3 μS, close to $(T_r/2) = 2.1\ \mu$S as expected from Fig. 5 for the nominal experimental conditions. The typical voltage and current waveforms of the transistors were found to be smooth (Fig. 9) except for some ringing at the onset of the boost period. This parasitic ringing seems to be associated with the stray inductances of the transformer.

The experimental waveforms of Fig. 10 support the conjecture that the output rectifiers operate under zero voltage conditions. This will be the case as long as the boost period is longer than the commutation time of the rectifiers. The commutation period is controlled by the secondary leakage inductance and the small voltage which persists during the boost period. This offset voltage is the reflected sum of V_{DS}(on) and the voltage across the conducting antiparallel diode (Figs. 1 and 4(b)).

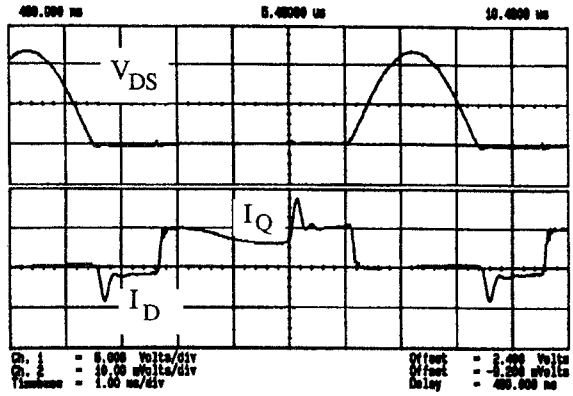


Fig. 9. Typical waveform of experimental PPRC. $f_S = 145$ KHz. Upper trace: 60 V/div. Lower trace: 1 A/div.

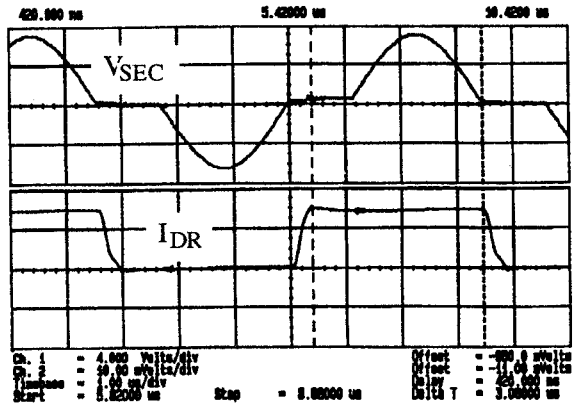


Fig. 10. Typical experimental secondary voltage (V_{SEC}) and rectifier diode current (I_{DR}). $f_S = 145$ KHz. Upper trace: 40 V/div. Lower trace: 1 A/div.

The voltage and current maximum values (ringing excluded) of the converter were found to be close to the theoretical value to within a few percents (Fig. 11). The drop in the output voltage (V_0) (Fig. 12) for small load resistances is attributed to voltage drops across the leakages of the transformer. The efficiency was also found to be dependent on the load resistance (Fig. 13). For light loads the efficiency is rather poor since the voltage dependent losses (such as magnetic losses) are proportionally large. At heavy loads, the efficiency drops again due to the proportional increase in the conduction losses. Similar to other topologies, each design is associated with an optimum load for which the efficiency is maximal. For large input voltage, the efficiency and voltage transfer ratio were found to be good (Fig. 14) even for a relatively high power level (100 W). The increase in output voltage was observed for very small currents (Fig. 15, when the output filter entered the DCM state, as predicted (see (21)).

Design Guidelines: The following procedure is suggested for practical PPRC design.

1) Select (n) to comply with the input to output voltage ratio requirement ($n = M$).

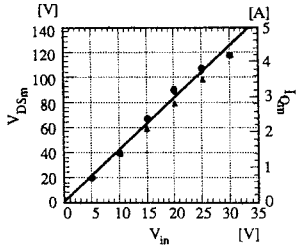


Fig. 11. Theoretical (line) and experimental MOSFETs voltage (triangles) and current (dots) stresses of experimental PPRC. $R_0 = 10\ \Omega$.

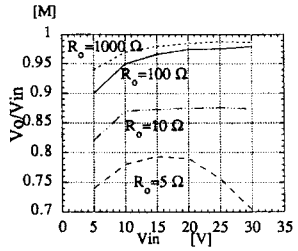


Fig. 12. Measured voltage transfer ratio of experimental PPRC-based dc-dc transformer.

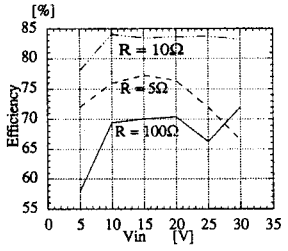


Fig. 13. Measured efficiency of experimental PPRC-based dc-dc transformer.

2) Select the operating frequency (f_S). Switching frequencies up to 1 MHz are practical with common power metal-oxide-semiconductor field-effect transistor (MOSFET) transistors and readily available magnetic materials.

3) Select the freewheeling resonant current and hence (I_{Dm}) to be at least twice the expected maximum input dc current. This is required to ensure an uninterrupted resonance current.

4) Apply (42) to calculate the resonance inductor (L_r), from (I_{Dm}) (step 3), (f_S) (step 2), and minimum expected V_{in}.

5) Select (f_r) so that the ratio (f_S/f_r) will be in the range 0.7–0.8 to ensure proper operation for reasonable tolerance of components.

6) Choose (b) to be in the range 0.1 to 0.3 ($L_{in} = L_r/(4b)$).

7) Check the compliance of the expected input current ripple (equation (31)) against specifications. If the ripple is too high select a larger L_{in} according to (31) and recalculate the factor (b).

8) Calculate (C_r) from (I_r), (f_r) and (b): ($C_r = (1+b)/[(2\pi f_r)^2 L_r]$).

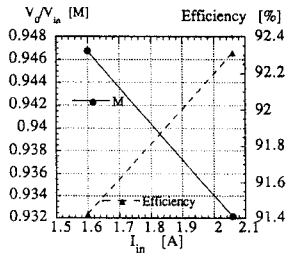


Fig. 14. Measured voltage transfer ratio and efficiency of experimental PPRC-based dc-dc converter for $V_{in} = 50$ V.

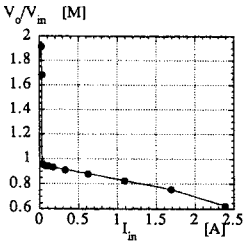


Fig. 15. Measured output transfer ratio of experimental PPRC when operated in DCM and CCM. $V_{in} = 10$ V.

9) Choose (L_0) to be approximately ten times the reflected resonant inductor ($n^2 L_r$) to avoid interaction between the output side and the resonant circuit. If light loads are expected (L_0) should be increased to avoid the DCM operational region (equation (21)).

10) Choose (C_0) to comply with the specified maximum output voltage ripple according to (29).

This procedure was applied to design a PPRC-based dc-dc transformer for a commercial product (a medical instrument). The PPRC topology was chosen because it permits operation at switching frequencies which are much higher than the signal frequency range of the instrument. Furthermore, aliasing problems were circumvented by synchronizing the switching to the master clock of the system from which the digital signal processing clock is derived. The high switching frequency was also beneficial in reducing the overall size and weight of the power stage and in simplifying primary to secondary high voltage (7 KV) isolation.

The main disadvantage of the proposed PPRC-based dc-dc transformer is the relatively large voltage stress of the switches. At minimum, the peak voltage across the switch will be πV_{in} (equation (32)). This implies that the proposed dc-dc transformer is more suitable to low input voltage application. It is interesting to note though that unlike high current stresses, high voltage stresses do not deteriorate the overall efficiency of the system. Since the current stressed of the PPRC appear only during the boost period, the expected efficiency of this resonant converter is theoretically higher than that of the conventional resonant converter in which the resonant current always flows through the switches.

The results of this study and the design experience already gained, suggest that the proposed dc-dc transformer has many favorable features that can make it useful in a variety of practical applications in which the primary power source is a battery or similar low voltage source.

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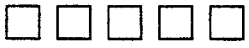

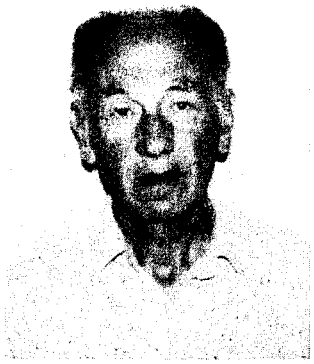

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