PATENT SPECIFICATION

DRAWINGS ATTACHED

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1,152,065

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Date of Application and filing Complete Specification: 21 Nov., 1966.
No. 51952/66.
Application made in United States of America (No. 508918) on 22 Nov., 1965.
Complete Specification Published: 14 May, 1969.

Index at acceptance: —G4 G(2B1, 2B7, 2B14, 2P, 2Q, 3A1, 3A2, 3A10)

Int. Cl.: —G 06 g 7/16

COMPLETE SPECIFICATION

Improvements in or relating to Analog Computing Circuit Arrangements

We, YISSUM RESEARCH DEVELOPMENT COMPANY OF THE HEBREW UNIVERSITY OF JERUSALEM, formerly Yissum Research Development Company, a Company registered under the laws of the State of Israel, of Administration Building, Hebrew University, Jerusalem, Israel, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement: —

The invention relates to analog multipliers and dividers such as the type used for analog computation, measurements and control, and more particularly to an electronic circuit for producing an output proportional to the product or division of its two inputs.

Conventional analog multipliers and dividers in general use one of the following methods, namely nonlinear elements, time division, hall effect devices, or servo amplifiers.

Of these, servo multipliers use negative feedback and thus can be made very accurate. This type of multiplier, however, has many drawbacks. Its operation is slow, it has moving parts which limit its useful life, and it is very hard to miniaturise because of the mechanism involved.

One object of the present invention is to provide the advantages of the conventional servo multiplier in its use of feedback in an arrangement that is simpler in construction and has no moving parts, thus extending its reliability and useful life.

The invention consists in an analog computing circuit arrangement for multiplier-divider apparatus, having at least first and second input signal terminals, wherein a light source is connected to the output of an amplifier whose input circuit includes a first input signal terminal, and in which two photoconductive cells are positioned to respond to said light source, the first one of said cells being connected in a first voltage divider to form an electro-optical feedback loop to said amplifier input circuit by co-operation with said light source, and the second one of said cells being connected in a second voltage divider to form an output circuit, said second input signal terminal either being connected directly to said second voltage divider to provide a multiplier circuit arrangement, or to said first voltage divider to provide a divider circuit arrangement such that an output signal is obtained which corresponds to the product or the quotient respectively of signals applied to said first and said second input signal terminals.

The invention will now be described with reference to the accompanying drawings, in which: —

Figure 1 is a circuit diagram of one embodiment of the present invention showing an analog multiplier for the production of an output voltage proportional to the product of the voltages in the two inputs X and Y, wherein the signal at X remains always with the same sign.

Figure 2 is a circuit diagram of another embodiment of analog multiplier in which there is no restriction as to the sign of the signal at input X.

Figure 3 is a circuit diagram of a divider embodiment.

The multiplier of Figure 1 consists of a differential amplifier A having positive and negative inputs. The amplifier supplies the power to a lamp L. The lamp illuminates

[*Price* 4*s*. 6*d*.]

simultaneously two photo-conductive cells PC1 and PC2, which form parts of two voltage dividers I and II, each consisting of a cell and a series resistor, R1 and R2 respectively. A constant voltage Vc is supplied at point C to the voltage divider I. The analog signals are supplied as voltages Vx and Vy at points X and Y respectively.

The two photoconductive cells are made of the same material, and thus respond to light in the same manner. The resistance of the cells at equal illumination need not be the same, and also the cells need not be equally illuminated by the lamp in the circuit described. The only necessary matching is that for any lamp L illumination the cell resistance will be related by the equation:

$$Rpc2=KRpc1 \quad (1)$$

where

RpcL=Resistance of PC1.
Rpc2=Resistance of PC2.
K=Constant.

Prior to operation the resistors are adjusted so that

$$R2=KR_1 \quad (2)$$

K is the same as in (1).

Amplifier A, the lamp L, and the voltage divider I form a negative feedback loop. It is well known from feedback theory that the voltage at point X' will follow the voltage at point X. The accuracy of the following depends upon the amplifier gain. This gain can be made high enough to maintain the desired accuracy. Thus

$$Vx=Vx' \quad (3)$$

Vx=voltage at point X.
Vx'=voltage at point X'.

But

$$Vx=Vx'=\frac{Vc\ Rpc1}{Rpc1+R_1} \quad (4)$$

Vc=voltage at point C.

and so

$$\frac{Vx}{Vc}=\frac{Rpc1}{Rpc1+R_1} \quad (5)$$

Because of the voltage divider II the voltage at the output is:

$$Vout=\frac{Vy\ Rpc2}{Rpc2+R_2} \quad (6)$$

By using (1) and (2) one can write:

$$Vout=\frac{Vy\ Rpc1}{Rpc1+R_1} \quad (7)$$

and by the use of (5) one gets:

$$Vout=\frac{Vx\ Vy}{Vc} \quad (8)$$

which is the desired result.

In this circuit, however, Vx may be only of one sign, positive (or zero) if the voltage at C is positive, and negative (or zero) if the voltage at C is negative.

Figure 2 is a complete multiplier with no restriction regarding the sign of the signal of Vx.

This circuit incorporates an inverter amplifier B with unity gain. By the use of B both Vy and −Vy are supplied to the voltage divider II. Constant voltages of the same magnitude but of opposite signs are supplied to the two ends of voltage divider I. The same reasoning as above will lead to the conclusion that the voltage output of this multiplier is also proportional to the product of the two input voltages Vx and Vy.

The advantage is, however, that the voltage at point X' and hence at point X may be in the range:

$$-Vc<Vx<Vc \quad (9)$$

The accuracy of the multiplier depends mainly upon the possibility of maintaining relation (1). However, matched pairs of photoconductive cells are readily available, and matching to a given accuracy is only a matter of a proper selection.

The dynamic range of the multiplier can be made large because the resistance of the photoconductive cell can be changed very easily over several orders of magnitude.

Frequency response of channel X is limited mainly by the frequency response of both the lamp L and the cells, and can be improved by finding components having higher frequency response. Several types of photoconductive cells may be used up to the megacycle range.

Although a lamp is described as the light source, it will be understood that the lamp can be replaced by any other light source provided that the light intensity can be controlled by the amplifier. The use of a gallium arsenide optical source, for example, will result in a higher frequency response.

The multiplier stability depends upon the amplifier stability and the matching of the cells with respect to temperature.

The circuit was tested by using a pair of cadmium selenide cells, a No. 40 pilot

lamp and an amplifier having a voltage gain of 5,000, and the following results were obtained:

Dynamic range: 40 db.
Accuracy over the above range: ±1%
Frequency response: 8.5 cps
Noise: 50 MV.

It will be understood that these results represent only a particular example, and do not represent the multipliers best possible specifications, which can be improved as stated above.

The same circuit can also be used as a divider. In Figure 3 points C and Y are inter-changed. One can therefore use the stated equations provided that Vy is replaced by Vc, and *vice-versa*. Equation (8) can be rewritten yielding:

$$(10) \qquad Vout = \frac{Vx}{Vy} . Vc$$

which means that the output in this connection is proportional to the ratio of Vx to Vy.

It will be understood that although a voltage divider is used and the circuit operates in the voltage mode, the results will be the same when the circuit is operated in the current mode.

WHAT WE CLAIM IS:—

1. An analog computing circuit arrangement for multiplier-divider apparatus, having at least first and second input signal terminals, wherein a light source is connected to the output of an amplifier whose input circuit includes a first input signal terminal, and in which two photo-conductive cells are positioned to respond to said light source, the first one of said cells being connected in a first voltage divider to form an electro-optical feedback loop to said amplifier input circuit by co-operation with said light source, and the second one of said cells being connected in a second voltage divider to form an output circuit said second input signal terminal either being directly to said second voltage divider to provide a multiplier circuit arrangement, or to said first voltage divider to provide a divider circuit arrangement such that an output signal is obtained which corresponds to the product or the quotient respectively of signals applied to said first and said second input signal terminals.

2. An arrangement as claimed in Claim 1, in which said amplifier is a differential amplifier.

3. An arrangement as claimed in Claim 1 or Claim 2, in which first impedance means are connected in series with said first photo-conductive cell to form said first voltage divider, second impedance means are connected in series with said second photo-conductive cell to form said second voltage divider, an input of said amplifier being connected to said first input signal terminal and another input of said amplifier being connected to an intermediate point on said first voltage divider, whilst said output signal is obtained from an intermediate point on said second voltage divider when a constant voltage source is connected across one divider and the second input signal is applied to one end of the other one of said dividers.

4. An arrangement as claimed in Claim 3, in which said constant voltage source is connected across said first voltage divider, and said second input signal is applied across said second voltage divider.

5. An arrangement as claimed in Claim 3, in which said constant voltage source is connected across said first voltage divider, the input of an inverter amplifier is connected to said one end of other one of said dividers, and the output of said inverter amplifier is connected to the other end of the same divider.

6. An arrangement as claimed in Claim 3, in which said constant voltage source is connected across said second voltage divider.

7. An analog computing circuit arrangement substantially as described with reference to Figure 1, or Figure 2 or Figure 3 of the accompanying drawings.

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Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1969.
Published by the Patent Office, 25, Southampton Buildings, London, W.C.2, from which copies may be obtained.

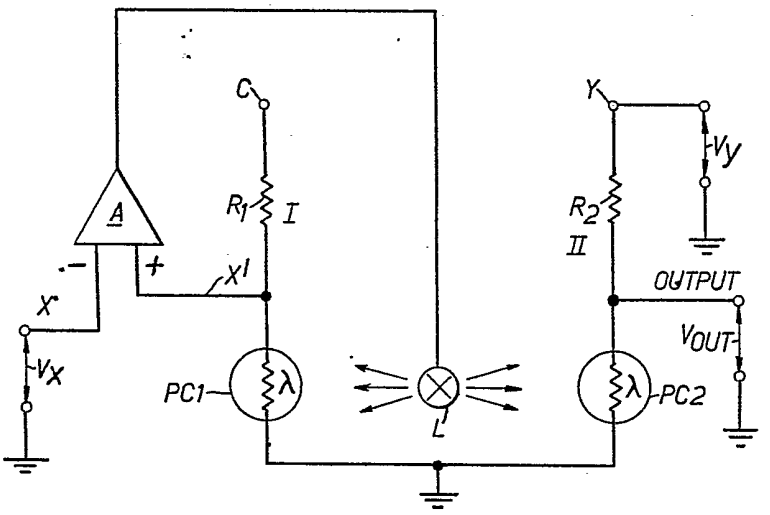
C
Y
A
R1
I
R2
II
Vy
X'
X1
OUTPUT
VOUT
VX
PC1
L'
PC2

FIG. 1.

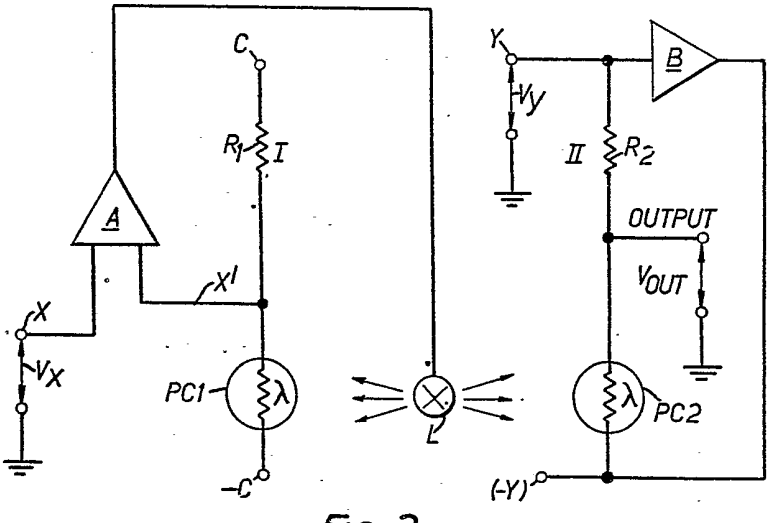
C
Y
B
A
R1
I
Vy
II
R2
OUTPUT
X1
X
VOUT
VX
PC1
L'
PC2
-C
(-Y)

FIG. 2.

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2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheets 1 & 2

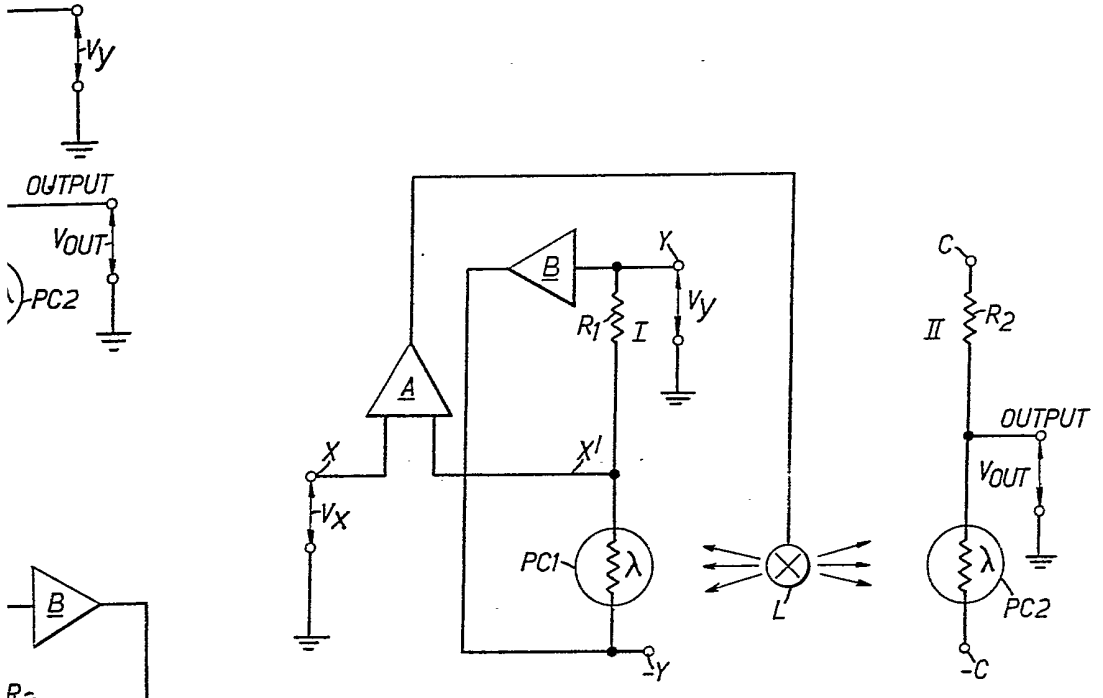

FIG. 3.

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2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheets 1 & 2

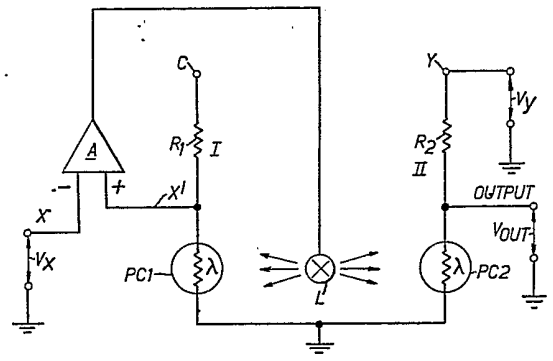

FIG. 1.

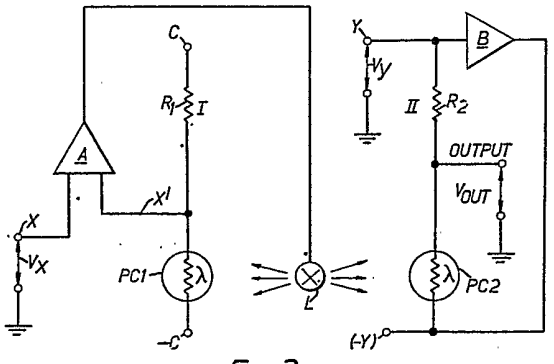

FIG. 2.

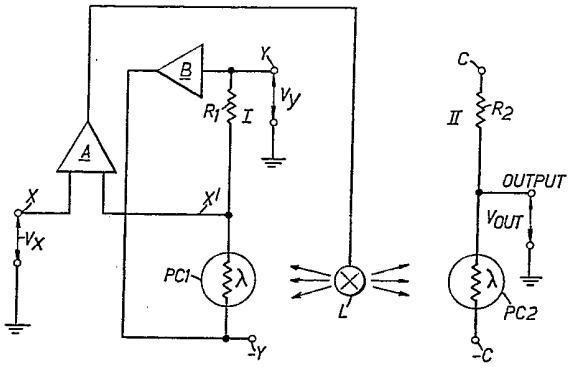

FIG. 3.