

A Merged-Stage High Efficiency High Power Factor HB-LED Converter without Electrolytic Capacitor

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Abstract

This paper introduces a merged converter topology for supplying high-brightness light-emitting diodes for lighting applications. The converter combines a boost-based power factor correction rectifier (PFC) and a resonant converter in a single-stage. In this topology both converters share the same switching components and a bulky electrolytic capacitor, existing in conventional systems, is replaced with a small film capacitor. These modifications result in a smaller volume and number of components, compared to other 2-stage topologies. The intermediate energy storage capacitor is reduced by allowing a large voltage ripple across it and storing a portion of energy in the resonant part of the converter. The converter is regulated by a digital controller implementing a variable-frequency variable-duty-ratio control algorithm. Constant light output and dimming capability are obtained by varying the frequency of the resonant part. The duty ratio control is used at the front end of the converter, to obtain power factor correction. Experimental results with a 15 W prototype verify reliable operation with a small film capacitor, near unity power factor, and high efficiency, varying between 88% and 90% over the entire operating range.

1. Introduction

High-brightness light-emitting diodes (HB LED) are becoming attractive solution for lighting applications because of their superior longevity, low maintenance requirements and high luminance. To supply these devices, cost-effective and reliable power supply solutions, i.e. LED drivers, are highly desirable.

One of the main drawbacks of the present utility line-fed HB LED drivers is the presence of a bulky electrolytic capacitor. It reduces the reliability and also increases the size and cost of the driver [1]. Most existing HB LED lighting supplies are single-stage solutions that provide high power factor and constant lamp current [1-9]. These single-stage drivers, based on flyback, boost or sepic converters, have a large electrolytic output capacitor that stores the energy difference between the constant output and time-varying input, thus eliminating light flickering twice the line frequency. The work presented in [2,4,10-13] demonstrates that two-stage solutions minimize the capacitor value and volume requirements, but they still use electrolytic capacitors and the savings come at the cost of a significant increase in the part count and controller complexity. The two-stage approach presented in [14] eliminates the electrolytic capacitor using bidirectional energy balance, but at the expense of a moderate input power factor, and increased component count. A solution shown in [15] eliminates the electrolytic capacitor but, the savings comes at the price of a significant increase of the filter inductors.

The objective of this paper is to demonstrate a merged boost-resonant converter as an LED driver that does not involve the previously mentioned tradeoffs. In the converter introduced here, the bulky electrolytic capacitor is replaced with a film capacitor and a low-current low-volume inductor having much smaller volume. Similar to topologies introduced in [4,16] the switching network is shared between two merged stages to minimize the component count. In this case the concept is applied to the resonant converter topology and a complete control solution for the converter is presented.

2. Single-Stage Boost-Resonant Converter

The converter configuration is shown in Fig. 1 it combines boost front-end stage with a resonant output. This topology is similar to the one presented in [17,18], used for fluorescent lamps. However, unlike the previous solution, it does not need a big electrolytic capacitor and can operate with high input voltages, i.e. full range of line voltages.

In this converter, both stages share a half-bridge network (Q_1, Q_2). The boost inductor is connected between the full-wave input rectifier and the middle point of the half-bridge while the resonant network is supplying an LED string, through a high-frequency transformer providing galvanic isolation. It can be seen that the chosen anti-parallel connection of LEDs allows direct drive with high-frequency current without rectification [19-22].

The converter is regulated by a digital controller that implements a variable duty ratio variable-frequency control method. To control the resonant output portion of the converter, variable frequency is used. The switching frequency is set above the series resonant frequency, to assure zero-voltage switching (ZVS). The operation of the boost is regulated through duty ratio variation. In this way, both the resonant and boost parts are controlled virtually independently. The frequency and duty ratio control signals are created with two separate compensators and fed to a novel digital block, named *pulse-frequency pulse-width modulator* (PF-PWM), creating variable-frequency variable duty ratio pulses.

The boost converter operates in the discontinuous conduction mode (DCM), to assure relatively high power factor at its input side. The voltage ripple of the intermediate capacitor, i.e. bus capacitor, is allowed to have large variations. Therefore, a low value capacitor can be used. The bus capacitor voltage V_{bus} is regulated with a slow controller such that its average dc value remains constant and the large ripple is not cancelled.

The role of the resonant part is to drive the LEDs by a constant average current to avoid low frequency light flickering under large bus voltage variations. The resonant current is sensed and regulated through average current programmed mode control that varies the drive frequency of the converter. In other words, *the resonant circuit operates such that a portion of the difference between the time-varying input power and the dc-average output power is provided by the resonant tank, easing requirements for the energy storage capacitor.*

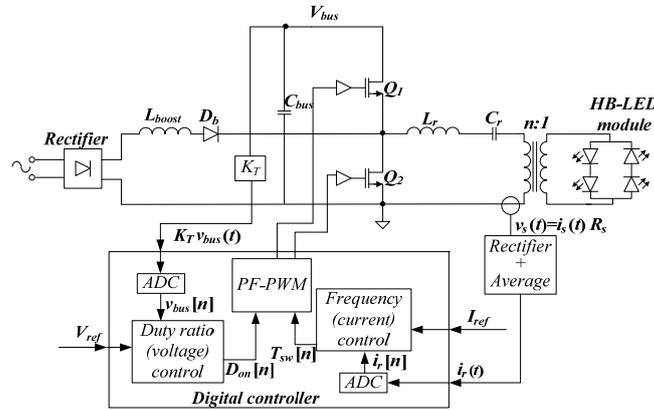


Fig. 1. Single-stage boost-resonant HB-LED driver

The resonant impedance and current as a function of the drive frequency can be expressed as:

$$|Z(j\Omega)| = Z_r \sqrt{Q^2 + \left(\Omega - \frac{1}{\Omega}\right)^2}; \quad (1)$$

$$|i_r(j\Omega)| = \frac{V_{bus_n}}{Z_r} \frac{n}{\sqrt{Q^2 + \left(\Omega - \frac{1}{\Omega}\right)^2}}, \quad (2)$$

where $Q=R/Z_r$ is the network's quality factor, $Z_r=L_r/C_r$ is the characteristic impedance, $\Omega=f/f_r$ is the normalized drive frequency with respect to the resonant frequency, and V_{bus_n} is the normalized bus voltage.

Figure 2 shows the well-known frequency characteristic of the series resonant network [23, 24] described with Equations (1) and (2). It implies that, in order to maintain constant current, the drive frequency of the converter should increase when the bus voltage is high and decrease for low values. To achieve this, the control loop is designed to have a bandwidth higher than twice the line frequency, i.e. bus voltage ripple. The current loop also provides external dimming capability, through changes in the reference input value I_{ref} (Fig.1).

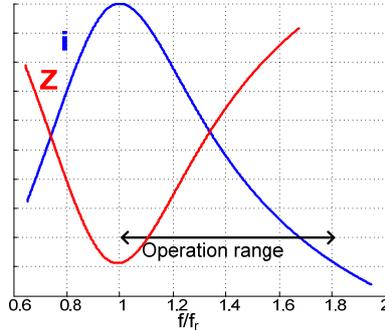


Fig. 2. Normalized impedance and current as a function of the normalized frequency.

3. Design Considerations and Practical Implementation

3.1. LED current control

The power supply drives the LEDs with constant average current. It is achieved through average current programmed mode control scheme where the switching period is changed in accordance to the following discrete-time control law:

$$T_{sw}[n] = T_{sw}[n-1] + k(I_{ref} - i_r[n]), \quad (3)$$

where $T_{sw}[n]$ and $T_{sw}[n-1]$ are the new and present switching periods, respectively, k is the integral gain, I_{ref} is the desired average current value, and $i_r[n]$ is the digital equivalent of the dc average LED-string current reflected to the primary side.

That is, the LED current controller varies the switching frequency of the converter such that the average of the rectified resonant current will match the desired value (I_{ref} , Fig. 1). It should be noted that, since the average of the high frequency current is of interest, the sampling rate of the controller is fixed at a frequency higher than the bus voltage ripple frequency, but significantly lower than the power stage switching frequency.

Figure 3 shows implementation of the rectifying and averaging circuit of Fig.1. The current sensing voltage, $v_s(t) = R_s i_s(t)$, is full-wave rectified and averaged to be measured by the ADC. The reason that the configuration of Fig. 3 was selected over many other possible options is primarily the need to monitor the currents of both LED strings with a single sensing point. Another reason is that the information of the peak current is available and can be used for fault protection.

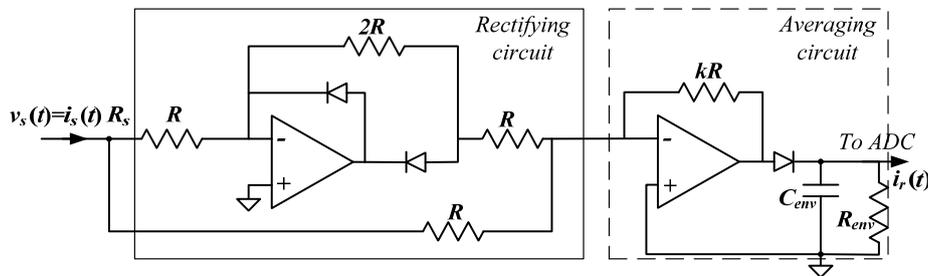


Fig. 3. Rectifying and averaging circuit.

3.2. Power factor correction and bus voltage regulation

To provide a good power factor the controller of Fig.1 regulates the duty ratio such that for a desired light output, i.e. dimming value, appropriate emulated resistance is seen at the input. Theoretically,

cally, regulation of this converter can be obtained with output current loop only. Since the emulated resistance of the boost input stage operating in the DCM depends on both on time and the bus voltage, power factor correction could be achieved by loosely setting transistor on times and allowing the bus voltage to compensate for a mismatch between input and output power. However, such an implementation is not practical due to the bus voltage runaway problem.

The runaway effect can be described as follows: the dc conversion ratio of the boost operating in DCM can be expressed by [23]:

$$\frac{V_{bus}}{V_{in}} = \frac{1}{2} \left(1 + \sqrt{1 + \frac{2D_{on}^2 |Z_L(f_s)|}{L_{boost} f_s}} \right), \quad (4)$$

where V_{in} is the input voltage, V_{bus} is the output voltage of the boost converter, $|Z_L(f_s)|$ is the equivalent impedance magnitude of the resonant network at a given operation frequency (f_s), L_{boost} is the boost inductor value, and D_{on} is the duty ratio, i.e. on time of transistor Q_2 over the switching period.

Assuming now, that D_{on} is constant and the frequency controller is attempting to reduce the output current of the resonant converter. Due to the action of the current control loop, this will result in an increased drive frequency and, consequently, increased impedance seen by the bus capacitor, i.e. boost output. As it can be seen from (4) the increased impedance raises the output voltage causing the output loop to further increase the frequency. This creates a runaway effect of the bus voltage causing overly large voltage stress on the components. To avoid this problem, the bus voltage controller (duty-ratio control, Fig. 1) is implemented.

The task of the voltage controller is to vary the duty ratio such that the average value of the bus voltage will be in a safe operating range that is predefined (V_{ref} , Fig.1). At the same time, as described earlier, the bus voltage is allowed to have a large ripple to allow small capacitor value and the use of non-electrolytic one.

The voltage controller realizes a non-linear control scheme that can be described with the diagram of Fig. 4. It depicts the changes of the bus voltage under typical operation of the voltage controller. The controller compares the dc value of the bus voltage with two threshold values that define the safe operating region, in which the duty ratio does not change. For voltage measurement smaller than the minimum threshold (V_{th_min} , Fig. 4) the duty ratio is increased by a fixed increment whereas measurements greater than the maximum threshold (V_{th_max} , Fig. 4) it decreases the duty ratio by the same amount.

It should be noted that the rate of the voltage control law is slower than the bus voltage ripple to allow average voltage measurement. As a result, twice the line frequency harmonic content is filtered out and does not affect the control command.

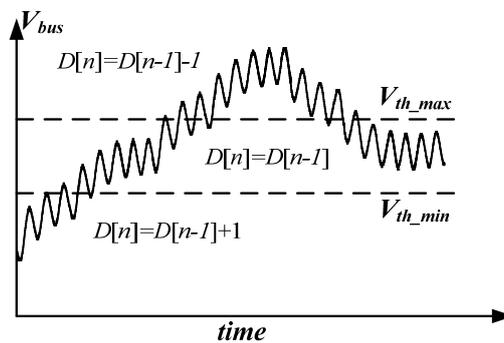


Fig. 4. Typical bus voltage waveform and the voltage control scheme.

3.3. Selection of the Reactive Components

The selection of resonant tank components and the boost inductor in this topology is dependent on multiple criteria. Namely, the values are chosen such that the ZVS condition are satisfied throughout the whole line cycle while maintaining a high power processing efficiency.

3.3.1. Inductors selection

During the transistor Q2 off time, the ZVS is obtained through a resonant circuit formed by the inductor L_r and the parasitic capacitance of the transistor. Similar to a conventional resonant converter, the ZVS condition for Q_2 depends on the resonant inductor value (L_r) and the current value at the commutation instance (I_{r_comm}) [23]. The energy condition can be expressed by:

$$\frac{C_{par_Q2} V_{bus}^2}{2} = \frac{L_r I_{r_comm}^2}{2}, \quad (6)$$

where C_{par_Q2} is the drain-source equivalent parasitic capacitance of Q_2 .

On the other hand, the current path during the conduction interval of Q_2 (when Q_1 is off) involves the input inductor. Therefore, ZVS condition for Q_1 depends on the boost inductance (L_{boost}) and on its current value (I_{boost_comm}) at the commutation point. To find the ZVS condition the following energy balance expression can be used:

$$\frac{C_{par_Q1} V_{bus}^2}{2} = \frac{L_{boost} I_{boost_comm}^2}{2}, \quad (7)$$

where C_{par_Q1} is the drain-source equivalent parasitic capacitance of Q_1 .

To guarantee ZVS conditions for the entire operation range, the selection procedure takes into account the minimum current value when the LEDs are dimmed and the highest instantaneous bus voltage allowed.

3.3.2 Selection of the resonant capacitor for obtaining high power processing efficiency

To obtain high efficiency operation, the switching frequency needs to be in the vicinity of the resonant frequency. A large deviation from the resonant point, either due to current regulation caused by increased bus voltage or lower current reference, results in higher energy that circulates in the resonant tank increasing conduction losses. Since a starting value of the resonant inductor was obtained as explained in the previous subsection the selection of the resonant capacitor is the key to ensure operation near the resonant frequency for given load and bus voltage conditions.

Assuming $Q \geq 1$, and $\Omega = 1.1-1.2$, ie. operation near the resonant frequency, and neglecting the triangular shape of the current due to the boost action, the average current (the LED current), I_{r_avg} can be approximated to:

$$I_{r_avg} = \frac{2}{\pi} I_{r_pk}, \quad (8)$$

where I_{r_avg} is the peak resonant current.

The equivalent ac-resistor [24], R_{ac_LED} , can be approximated by:

$$R_{ac_LED} = \frac{8}{\pi^2} \frac{V_{LED} n^2}{I_{r_avg}}, \quad (9)$$

Substituting (8) and (9) into (2), and after some manipulations, the resonant capacitor, C_r , can be expressed by:

$$C_r = L_r \left[\left(\frac{2QV_{bus}}{\pi I_{r_avg} R_{ac_LED}} \right)^2 - \left(\Omega - \frac{1}{\Omega} \right)^2 \right] / R_{ac_LED}^2. \quad (10)$$

4. Digital Controller

The controller of this converter changes the drive frequency at a high rate, to accommodate the large voltage variations of the bus voltage around the dc value. At the same time, it also varies the duty ratio slowly, to regulate the dc value of the bus voltage and achieve close to unity power factor. This means that a variable-frequency with constant absolute duty ratio control is required. For that purpose, a novel digitally controlled high-resolution *pulse-frequency pulse-width modulator* (PF-PWM) of Fig. 1 is developed.

A simplified block diagram of the modulator is shown in Fig.5. The modulator receives information about the absolute value of the duty ratio, i.e. desired on time over T_{sw} ratio, from the voltage loop. Then, based on the required switching period, which is set by the compensator of the resonant

converter, it adjusts the on-time accordingly. In this way constant duty ratio is maintained for variable frequency. To convert the absolute duty ratio value into appropriate on-time without sacrificing time and frequency resolution a dedicated block, named $D_{on}-T_{on}$ converter, was developed.

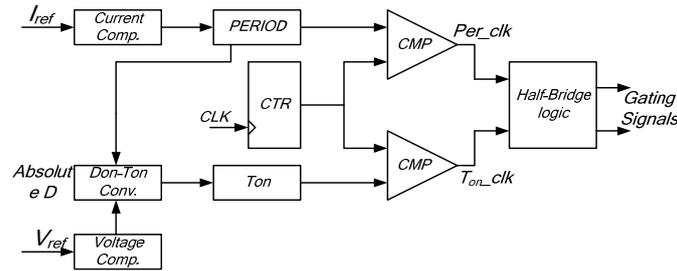


Fig. 5. Digital gating generation for pulse-frequency pulse-width modulator (PF-PWM).

5. Experimental Results

A 15 W prototype of the HB LED driver was designed and built according to the schematic of Fig. 1.

The parameters of the experimental unit were: Input voltage: 110 Vrms; Output load: 2x4.5 V@ 1.6 A high brightness white LEDs at each anti-parallel side; Frequency range: 90 kHz - 300 kHz. The component values are: Boost inductor: 500 μ H @ 0.2 Arms; Resonant inductor: 300 μ H @ 1Arms; Bus capacitor: 2 μ F @ 400VDC (thick film); Resonant capacitor: 10nF @ 630V (polypropylene); Transformer: 4:1, E16 3F3. The digital controller was implemented using an FPGA development board.

The bus capacitor value is 2 μ F, which enables the use of a non-electrolytic capacitor. It should be noted that capacitor used in this work is smaller by two orders of magnitude in comparison with previously reported solutions in the literature (that used electrolytic capacitors) for similar power levels.

The experimental results confirm high efficiency and a good power factor. Performance of the converter was evaluated for two dimming cases, nominal power (15W) and about half power (7.7W). The measured efficiency was 90% and 88%, respectively.

Figures 6 and 7 verify functionality of the system. Fig. 6 shows the lamp current and the drain-source voltage of Q_2 as well as the large bus voltage ripple that is allowed. Fig. 7 shows a zoomed-in view of the lamp current and voltage, as well as, Q_2 drain voltage, confirming ZVS operation of the converter and current balancing (50% conduction of each LED while $D_{on}=20\%$).

Figs. 8 (a) and (b) demonstrate performance of the converter operating at 110Vrms under full load and 50% dimming conditions, demonstrating near unity power factor while the LEDs current envelope is constant. Figs. 9 (a) and (b) show operation of the driver for low line (90Vrms).

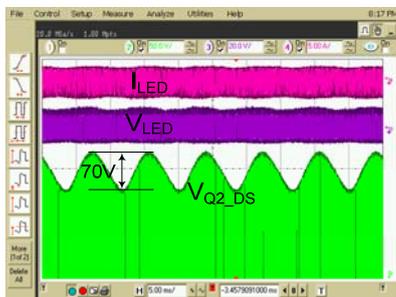


Fig. 6. Experimental results. Regulation capability of the output current of the converter under large bus voltage ripple variations. Lamp current (I_{LED} , 5A/div), Lamp voltage (V_{LED} , 20V/div), Drain-Source voltage of Q_2 (V_{Q2_DS} , 50V/div). Horizontal scale: 5ms/div.

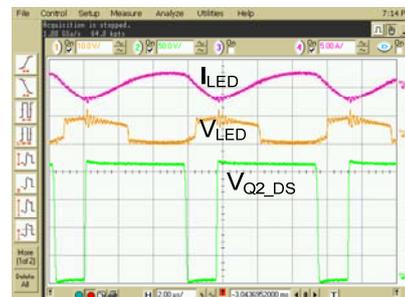


Fig. 7. Experimental results. Balanced lamp current under asymmetrical control operation and ZVS operation of the power transistors. Lamp current (I_{LED} , 5A/div), Lamp voltage (V_{LED} , 20V/div), Drain-Source voltage of Q_2 (V_{Q2_DS} , 50V/div). Horizontal scale: 2 μ s/div.

Measurements of the harmonic contents at the full load are given in Fig. 12. They were obtained for both high and low line input. It can be seen that the harmonics are far below the class-C limits.

The crest factors (I_{pk}/I_{rms}) of the LEDs current (Fig. 7) were calculated to be 1.6 for the triangular part (during the time Q_2 conducts) and 1.45 for the resonant part (during the on time of Q_1).

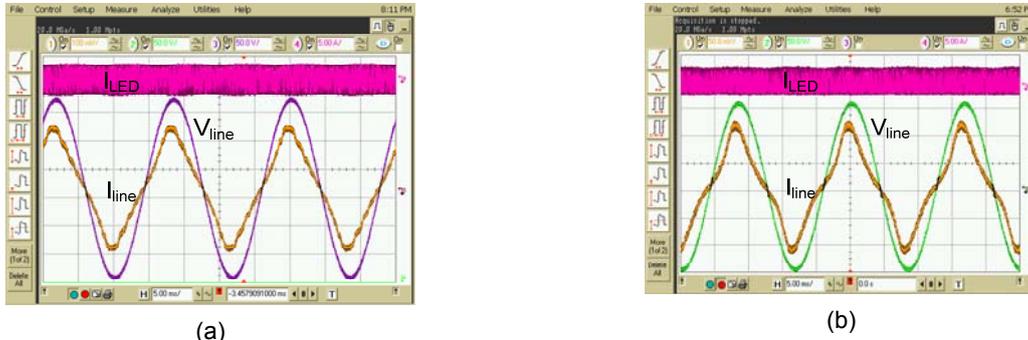


Fig. 8. Experimental results. Performance under dimming in (a) full power and (b) half power (7.7W) at high line input voltage of 110Vrms. Lamp current (I_{LED} , 5A/div), Input line voltage (V_{line} , 50V/div), Input line current (I_{line} , 50mA/div). Horizontal scale: 5ms/div.

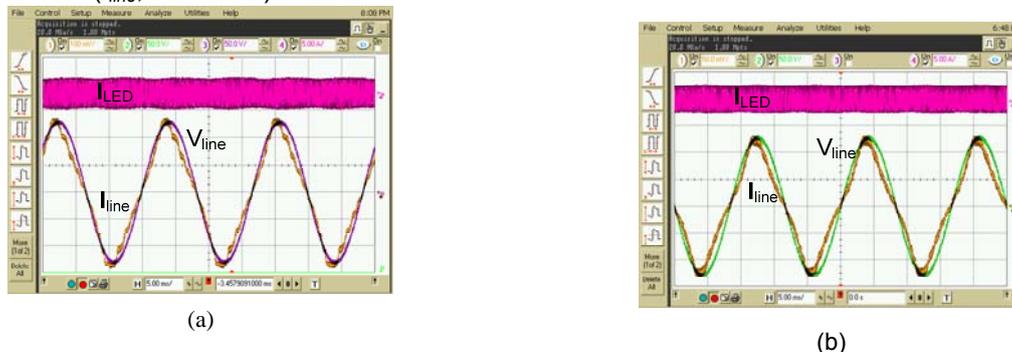


Fig. 9. Experimental results. Performance under dimming (a) full power and (b) half power (7.7W) at low line input voltage of 90Vrms. Lamp current (I_{LED} , 5A/div), Input line voltage (V_{line} , 50V/div), Input line current (I_{line} , 50mA/div). Horizontal scale: 5ms/div.

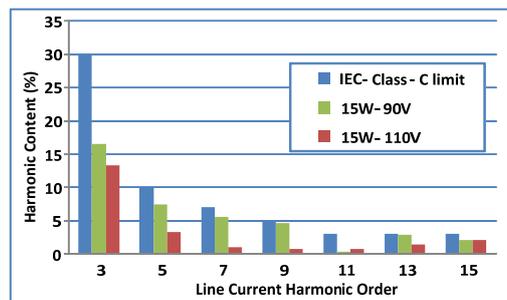


Fig. 10. Measured line current harmonics at high line (110Vrms) and low line (90Vrms).

6. Conclusions

A merged boost-resonant converter is introduced as a HB-LED power supply, i.e. driver with PFC rectification. The supply is designed such that the energy storage capacitor ripple is allowed to have large deviations. Hence, the bulky electrolytic capacitor is eliminated.

The front-end portion of the converter employs a boost converter operating in DCM to achieve high power factor operation. To avoid voltage runaway, the output voltage of the boost converter (input of the resonant part) is regulated by duty ratio control. A digital control

algorithm was developed to carry out the current and voltage control tasks, through variable-frequency variable duty ratio control.

Operation without electrolytic capacitor, high efficiency and high power factor were experimentally verified for different line and load conditions.

Acknowledgment

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7. Literature

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