Plug-and-Play Optimal Transient Mitigation Control Circuitry for High-Power High-Performance VRM

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***Abstract* – This paper introduces a plug-and-play sensing circuitry and controller to enable optimal transient recovery in high-end single-phase and multiphase buck converter VRMs. The control circuitry provides transient detection and charge balance point identification independently of parameters variations. Detailed circuit operation is provided as well as component selection consideration for practical implementation. The time-optimal response operation is verified via simulation and experiments on a 12V-to-1V, 100A multiphase buck prototype.**

I. Introduction

A target feature of high-power, high-performance, VRMs is the ability to maintain a well-regulated, virtually constant, output voltage under wide and rapid load changes while maximizing power density. A key consideration to achieve this goal is an immediate and accurate detection and identification of the load transient. The predominant solution to sustain and satisfy the high current load requirement is phase paralleling and/or interleaving of multiple lower power converters. The distribution onto multitude of converters is done to achieve higher steady-state efficiency (by optimization of components to the operating conditions as well as advanced current sharing features) [1]-[4], increase the overall power density with utilization of smaller magnetics [5]-[7], and accommodate the extremely demanding requirements of load transient without significant increase of the output capacitance [8]-[10]. Since a multiphase solution inherently dictates spread hardware and distributed sourcing of the load, transient mitigation, and in general the load management, have become more complex on concept as well as the practical implementation.

As of present-day, two control approaches are predominant for operating multiphase-based VRMs (each with many derivatives and implementation flavors). One is a droop control [11]-[15] which implements voltage regulation as well as current sharing by manipulating the effective per phase target voltage and equivalent resistance as prescribed by the load-line requirement. The second method employs current-programmed mode control with inner per-phase current control, in addition to the voltage loop [16]-[17]. Load transients are handled by either linear control with dual or multiple compensators [18]-[19], phase synchronization and non-linear time-optimal control (TOC) [20]-[24]. In several controllers descriptions, the transient mitigation is tightly connected to the operation mode, requires information of the current (either total or per-phase). In many cases the transient mitigation unit has to be fitted onto the specific circuit parameters, which is quite tedious and complex.

Regardless of the general controller core, to minimize the output voltage deviation during load transients, the common practice is to enhance the control bandwidth which results in fast ramp up/down of the total current to the load so that minimal charge mismatch between the load current and the source is facilitated. Other goals associated with the load transients in the context of multiphase sourcing are to maintain current sharing between the phases, synchronization during and more importantly at the settling period.

To achieve the minimal voltage deviation under load changes, either TOC or minimum-deviation control [22]- [25] is essential. This requires a transient detection unit and some information of the loading event, ideally the load current information. Since to achieve the latter is quite complex, an alternative approach that identifies the output capacitor charge balance point based on information of the output voltage alone has been widely studied in the context of single-phase converters [25]-[29]. The majority of the approaches rely on either knowledge of the system parameters, or present calibration procedures to select the sensor's parameters for accurate results. Furthermore, as opposed to single-phase applications (or generally lower load currents), where the effect of the output capacitor's ESR on the output voltage is quite substantial, and is utilized for both detection and identification of the load information, in the case

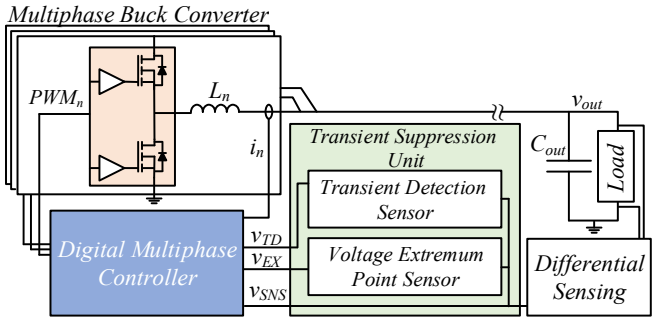

Fig. 1. Simplified schematic diagram of a multiphase buck system.

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of high-power multiphase the output capacitor's ESR is extremely low, and extremely hard to estimate or calibrate based upon. As a result, optimal transient suppression for multiphase operation needs to be revised according to the actual (more ideal) output voltage response.

The additional layer of complexity is that commercial VRM applications rely on the well-established compensation scheme to guarantee reliability, performance and above all reduced complexity and cost. It would be extremely advantageous, and potentially better absorbed by the industry, if transient suppression unit (TSU) could be integrated as an add-on unit to the VRM without the need to interfere, calibrations, replace or modify the original design.

The objective of this paper is therefore to introduce a plug-and-play circuitry and controller to facilitate time-optimal and minimum deviation control for high-performance VRM under large and rapid load changes. In particular, the control approach is suitable for multiphase buck regulators where the load transient requirements are extremely stringent, the output voltage deviation is primarily resulted by the charge mismatch at the output capacitor, without significant information that can be obtained from the output capacitor's ESR. As presented in Fig. 1, the TSU comprises load transient detection as well as its information (signal's extremum point), which extracted directly from the output voltage measurement, without the need for further manipulations neither calibrations of the sensing circuit to comply with the board parameters. This paper further highlights several practical challenges and constraints that are associated with the signal acquisition in multiphase VRMs, such as differential measurement requirement and hardware bandwidth limitations, a plug-and-play solution of these is delineated as well.

The rest of the paper is organized as follows: Section II revises the fundamentals of time-optimal recovery and describes the main challenges in execution of the control. The plug-and-play circuitry and control are thoroughly described in Section III, which also includes a detailed discussion on the practical aspects of the implementation. Section IV details a simulation case study of the controller and is followed by experimental validation on a multiphase buck VRM platform. Section V concludes the paper.

II. Time-Optimal Recovery for High Energy Loads

In buck converters, TOC achieves minimum voltage deviation within the minimum possible convergence time [24]. These ultimately lowers the overall output capacitance that is required and increases power density. In some cases to lower the peak inductor current without compromising the voltage deviation, minimum-deviation approach [22] is preferred, at the cost of slightly longer convergence time. Both methods employ single on-off cycle and rely on the same information, but with slightly different convergence profile, beyond the charge balance point. To facilitate either method, the following information is required: (a) an indication of load transient event and its direction (the corresponding transistor is turned on), and (b) the time duration from the start of transient until the point that charge balance is obtained. Typical TOC operation can be viewed in Fig. 2 (a) which presents waveforms of a single-phase buck converter operation under loading transient event with load variation between two steady-state currents I_{ss} and $I_{ss\text{-}new}$. The transient recovery divides into two main sections, the first section is the initiation of the inductor current ramp up T_0 while the second is the charge balance point, denoted by T_{min}. In a system with non negligible output capacitor ESR, the actual capacitor voltage v_C differs from the v_{out}. When the inductor current reaches $I_{ss\text{-}new}$, the output capacitor voltage is at V_{min} and the output capacitor charge recovery phase begins.

The recovery phase comprises an extended on-time portion which is then followed by an off phase. This is done to fully recover the capacitor charge balance, which is manifested by output voltage at its original steady-state value at T_{end}. The reminder T_{on} and T_{off}, beyond T_{min} can be expressed as:

$$T_{on} = T_{peak} - T_{min} = (T_{min} - T_0)\sqrt{D}\,; \tag{1}$$

$$T_{off} = T_{end} - T_{peak} = (T_{min} - T_0)\left(\frac{1}{D} - 1\right)\sqrt{D}\,, \tag{2}$$

where D is the system average steady-state duty-cycle ratio.

One method to determine the exact location of T_{min} has been presented in [22] by mimicking the output capacitor voltage behavior using R_sC_s network that matches to $R_{esr}C_{out}$ and the sensor is presented in Fig. 2 (b). This method has been found extremely effective in cases that the ESR is significant such as in single-phase or lower current VRs. It should be noted however that, the circuit of Fig. 2 (b) requires on-board calibration, which in some cases may be found quite complex. In addition, as in the case on-hand, with high-current multiphase converter, where the effect of R_{esr} is negligibly small, the output voltage equals the capacitor's voltage, and there is a need for an alternative method to obtain T_{min}.

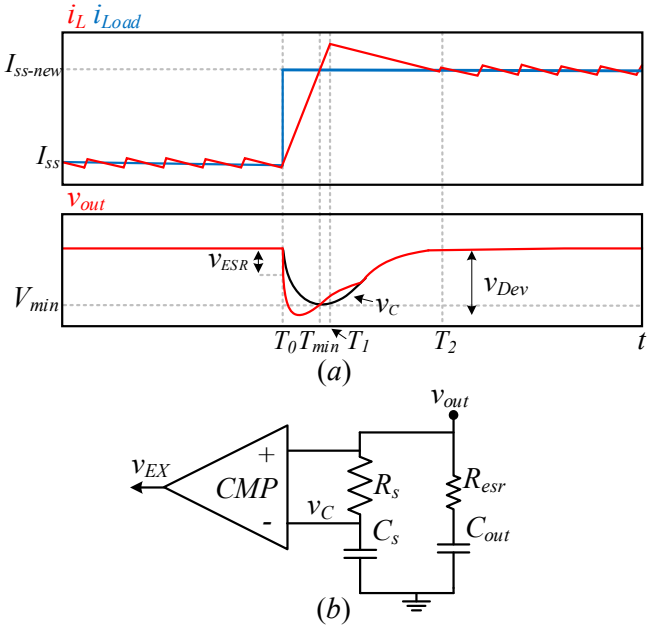


Fig. 2. (a) Typical waveforms of Time-Optimal recovery in single-phase buck for loading transient, with the presence of relatively high ESR. (b) Circuit for output capacitor voltage reconstruction and minimum voltage detection.

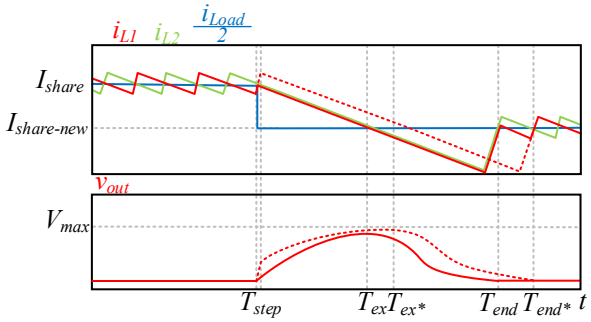


Fig. 3. Two phases interleaved buck converter operation with Time-Optimal Control during unloading transient. Recovery patterns for: (a) Synchronized operation. (b) Asynchronous, all-aligned ramp down.

TOC with multiphase buck VRM further increases the system's transient performance as can be seen in Fig. 3. Since the current slew during ramp up is quite steep (due to the high voltage that is applied on the inductor during the on time), charge balance at loading transient is achieved relatively fast and with small voltage drop. Fig. 3 demonstrates a more challenging scenario where the system slopes are more moderate. The TOC operation is shown for an unloading transient event in two-phase multiphase buck for two recovery options. The first option is to force both phases to ramp down together upon detection of a transient event, paralleling the converters operation which results in smaller voltage deviation. The second option is to retain the synchronized operation of the interleaved converters, which comes at the cost of larger voltage deviation. Within the context of this study, which focuses on the detection circuit and aims to support any prescribed transient mitigation scheme, since the voltage maximum point occurs when the summed inductor current reaches the new load current, then the TSU is oblivious to the chosen method.

III. Plug-and-Play Transient Mitigation Circuit

As indicated in the previous section, to facilitate TOC, two timing points are required for the controller, commencing of transient T_0 (and its direction) and the charge balance point T_{min}. In the context of multiphase VRM, the information can be extracted directly from the output voltage signal by evaluation of change in value and extremum point, respectively.

The operation of the transient mitigation circuit is detailed for a case of loading transient (unloading case requires few minor modifications). It identifies the critical points (T_0 and T_{min}) in the absence of output capacitor ESR and does not require calibration to the system's parameters. As can be seen in Fig. 4, loading transient is detected at T_0 where v_{SNS} drops below a detection threshold, marked by v_{TDL} goes high, signaling the controller to ramp up the inductors current. This signal also triggers a counter for the duration of T_{min}. The charge balance point T_{min} is identified by the minimum point of v_{out}, stopping the counter by v_{EX} rising edge signal. The minimum point is detected using a valley detection circuits (as detailed later) which is reset slightly after the valley point for preparation for the next transient. Following is specific description of the sensor's hardware for implementation.

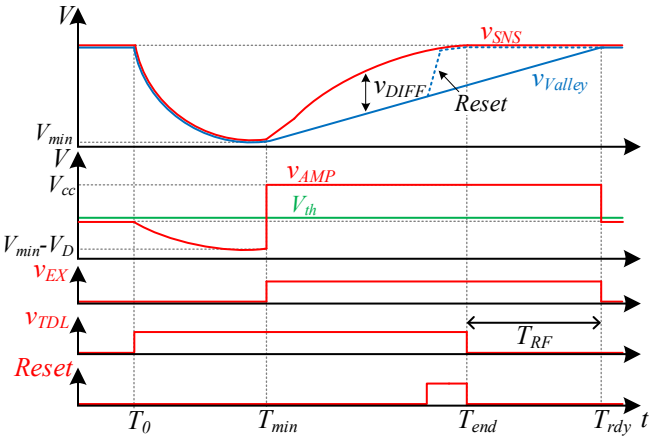


Fig. 4. Operation of the transient mitigation unit describing loading transient recovery.

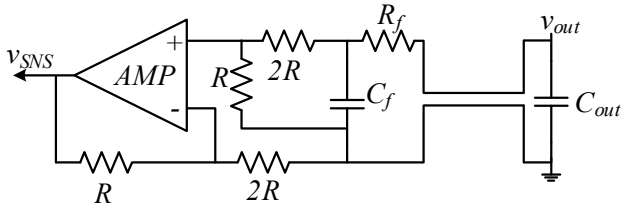


Fig. 5. Differential v_{out} sensing to single-ended interface.

In spread hardware setup as in multiphase supply, the output voltage sensing point can be located a fairly long distance away from the controller, accumulating noise and other potential errors. Therefore, it is quite impractical to sense v_{out} using a single-ended sensor, and the common practice is to use a lengthy differential pair and a differential to single-ended amplifier (Fig. 5) to provide the controller with as clean as possible v_{SNS} signal accurately representing the v_{out} signal at it sensing point. The differential to single-ended front-end sensor is realized using an op-amp differential amplifier and a R_f C_f low-pass filter to remove any high-frequency noise that may be added to the v_{out} signal.

Fig. 6 and Fig. 7 show the tracking window transient detection circuit and its operation waveforms, respectively. During steady-state operation, v_{SNS} is within the steady-state window between the two threshold voltages $V_{th\text{-}H}$ and $V_{th\text{-}L}$. The threshold voltages can be adjusted by selecting different relations between $R_{1\text{-}3}$ according to the system specification. These can be expressed as:

$$V_{th-H} = v_{SNS}\frac{R_2 + R_3}{R_1 + R_2 + R_3}; \quad (3)$$

$$V_{th-L} = v_{SNS}\frac{R_3}{R_1 + R_2 + R_3}. \quad (4)$$

In many cases, high-performance loads require droop load-line voltage profile, i.e., slightly lower output voltage as the load increases. As a result, the steady-state point of the output voltage changes, and the sensor tracks the average state of the output voltage. This is facilitated through the dependency of $V_{th\text{-}H}$ and $V_{th\text{-}L}$ in v_{SNS} , as expressed in (3-4), where the thresholds track

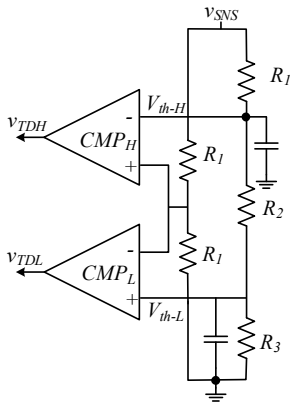


Fig. 6. Output voltage tracking window transient detection circuit.

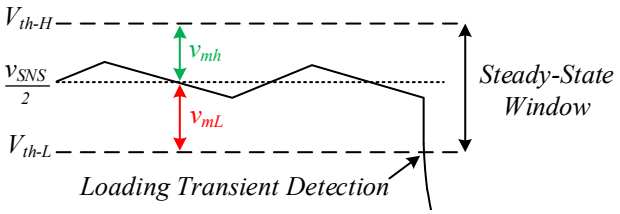


Fig. 7. Illustrative waveforms of window tracking and transient detection operation.

around v_{SNS} to its new nominal value after transient. While a straightforward approach is to create an even-sized margins v_{mH} and v_{mL}, an alternative option is to space the margins unevenly for better compensation of unloading transients. Ultimately, the threshold voltages are desired to be as close as possible to V_{nom} without false triggering due to the steady-state ripple or any switching noise. Since in such applications, the output voltage ripple is negligibly small, the window width is designed within that range of few mV, excluding any noise.

The output voltage minimum point V_{min} is sensed by the extremum point sensor showed in Fig. 8 and its related waveform shown in Fig. 4. At the period between T_0 and T_{min}, v_{SNS} fall below the nominal value, reaching minimum value (V_{min}) at T_{min}. During this time, v_{Valley} (Fig. 8) follows v_{SNS}. Once the output voltage reached V_{min}, while the output voltage start to rise back towards V_{nom}, the signal v_{Valley} rises slower, or clamped at its V_{min} value. This difference can be identified via several methods, one is using a difference amplifier, however, the gain-bandwidth limitation of any difference amplifier renders this method impractical. An alternative approach that has been employed in this study is by looking at the large signal at the peak detector amplifier output, v_{AMP}. In this way, the signal swing is substantial and the transition can be detected by a simple comparator. It should be noted however, that to facilitate fast detection, the peak detector gain bandwidth is of importance, as analyzed by Fig. 9. Still this method is of significantly lower complexity and high immunity to noise compared to the former.

To complete the sensor operation and output charge recovery phase the controller can now use T_0-T_{min} when v_{SNS} return to nominal value a refresh time T_{RF} is required in order to allow

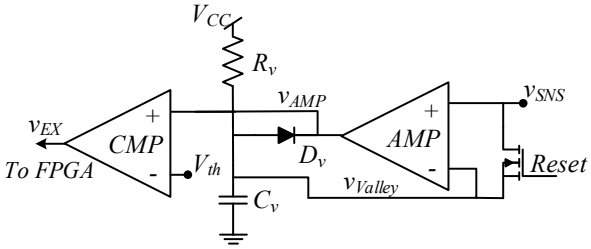


Fig. 8. Circuit description of extremum point detection; demonstrated for loading transients (valley point detection).

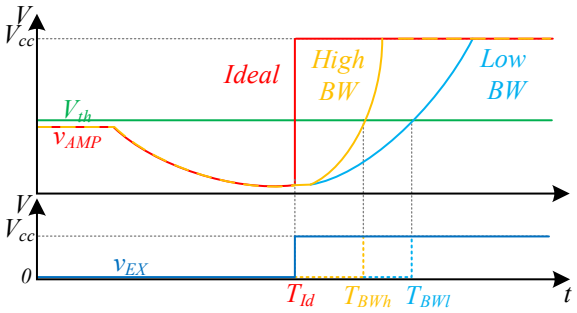


Fig. 9. Illustration of the impact of the sensor BW on the detection performance.

v_{Valley} to return to v_{SNS} at T_{rdy}. When the refresh phase is complete the sensor is ready for the next transient event. Rapid consecutive transients may occur in high-performance systems, therefore it is essential to reset the detector as soon as the required values are read. The peak detector reset is facilitated by a transistor, pulls v_{Valley} back to v_{SNS} (Fig. 4).

Since the accuracy of the time information is essential to satisfy accurate TOC, and since the entire load transition under this scheme is very short, reducing the potential delays and properly defining the sensor's components is of importance. A key consideration is the bandwidth of the peak detector op-amp. Depicted in Fig. 9 is the behavior of an idealized detection, alongside detection with lower bandwidths. It can be seen that the detection accuracy of the minimum point is proportional to the amplifier bandwidth. Assuming first order response of the op-amp, the delay time, T_{Delay}, can be expressed as:

$$T_{Delay} = 1 - 0.1 \cdot ln\left(BW_{MHz}\right)[\mu sec], \quad (5)$$

where BW_{MHz} is the operational amplifier bandwidth in MHz.

IV. Simulation and Experimental Validation on Multiphase Buck Conv

The transient mitigation operation has been validated using 12V to 1V four-phase multiphase buck converter on simulation and two-phase multiphase buck for the experimental prototype. The converter parameters are presented at Table I. The extremum sensor operation is validation in loading transient event as explained in section III is shown in Fig. 10 using PSIM simulation. A loading transient of 40A (10A per phase) causes the output voltage to drop and enter Time-Optimal transient suppression. The extremum sensor successfully senses the

TABLE I – EXPERIMENTAL PROTOTYPE PARAMETERS

Parameter	*Value/Type*
Input voltage V_{in}	12V
Average output current $I_{out,AVG}$	10A,35A
Power Stage	SiC620A, 60A
Inductor	1µH
Output capacitance, C_{out}	1.3mF
Switching frequency ,f_{sw}	500KHz
Amplifier bandwidth	100MHz

minimum voltage point marked by v_{EX} rising edge. Additionally, Fig. 10 shows the reduction in refresh time with sensor reset is showed by $v_{EX\ Reset}$, inducing the minimal time before next transient by T_{RF} of approximately 10µs.

The impact of amplifier bandwidth on the extremum sensor accuracy is shown in Fig. 11, comparing different bandwidth influence on the rising of v_{AMP} under the same transient conditions in Fig. 10. The ideal case represents the optimal sensor response using unlimited bandwidth amplifier providing zero delay extremum detection, lower amplifier bandwidth provides deviation from the ideal case, which increases sensor's delay. In practice, implemented amplifiers have limited bandwidth because of die area and power-consumption considerations, thus the sensor delay needs to be considered.

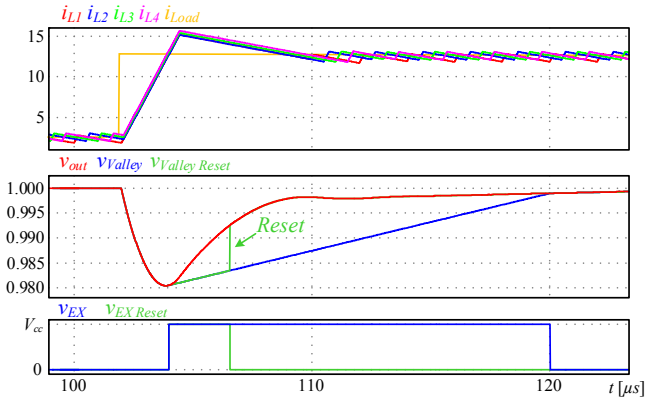


Fig. 10. Simulation results of the transient mitigation unit in case of loading transient.

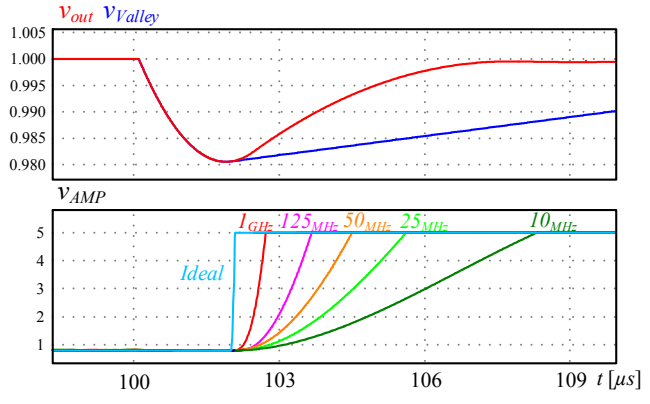
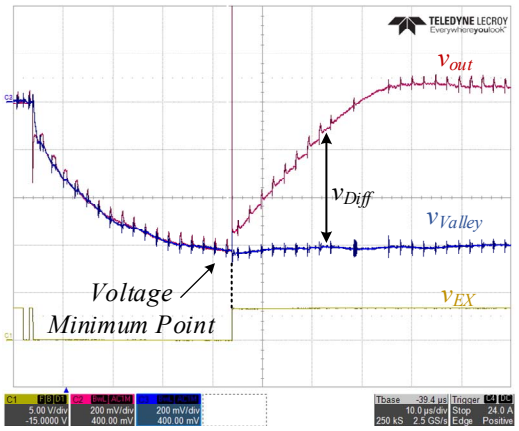
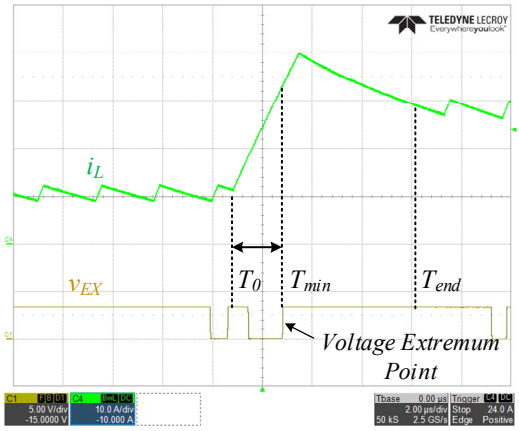


Fig. 11. Effect of sense amplifier bandwidth on extremum point detection.



(a)



(b)

Fig. 12. Transient mitigation unit experimental results (a) two-phase multiphase buck converter 10A → 64A loading transient output voltage waveform (b) single phase operation 10A → 30A loading transient current waveform.

The experimental prototype realized with all the related peripherals and a multiphase controller implemented on Altera Cyclone IV FPGA. Experimental results shown in Fig. 12 (a) and (b) demonstrate the operation of the transient mitigation unit executing time-optimal control. Fig. 12 (a) shows a loading transient response from 10A to 64A load step. The signal v_{EX} indicates the minimum point as v_{out} and v_{Valley} split. In Fig. 12 (b) the inductor's current waveform is depicted for 20A load step, marked on v_{EX} here the period T_{min}-T_0.

V. CONCLUSION

A Plug-and-Play optimal transient mitigation control circuitry for high-power high-performance VRM has been presented, and verified in simulation and on experimental 12V-to-1V multiphase buck prototype. The new TSU provides all the necessary information for successful TOC operation in near ideal remotely sensed high-performance systems with non-quantifiable ESR. The TSU does not require on board calibration and accommodates any number of either interleaved or paralleled phases.

ACKNOWLEDGEMENTS

This research is supported by Vishay Ltd., Siliconix IC division.

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