Thermal stability of Pt Schottky contacts to 4H–SiC

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Depth profiles by x-ray photoelectron spectroscopy have been used in conjunction with current–voltage measurements to study the thermal stability of a 50-nm-thick Pt contact to *n*-4H–SiC substrate. A reaction between the Pt and the SiC substrate is observed at temperatures of 600 °C and above. Annealing below that temperature improves the ideality and the uniformity of the Schottky characteristics, while annealing above this temperature degrades the electrical performance and uniformity. Thermodynamic stability is not reached even after annealing for 1 h at 900 °C. A local improvement of the characteristics at 800 °C is correlated with the formation of a second graphite film in the Pt–SiC reaction. © *2000 American Institute of Physics.* [S0021-8979(00)00523-5]

I. INTRODUCTION

Silicon carbide has received growing attention during the last decade for being the most mature and promising candidate material for high temperature and high power electronic device applications.[1] Out of the three commercially available polytypes (3C–, 4H–, and 6H–SiC), 4H–SiC offers the widest band gap, highest electron mobility, and the lowest micropipe densities.[2] The ability to utilize these qualities for high temperature electronic devices will mostly depend on the stability of the contacts to these devices. Knowledge of the thermal stability of metal contacts and their electrical properties is therefore of crucial importance for device makers. Yet, very few studies have been reported on the thermal stability of Schottky barriers to 4H–SiC.[3] In this article, we report on the thermal stability of Pt Schottky contacts to *n*-type 4H–SiC. We compare depth profiles obtained by x-ray photoelectron spectroscopy (XPS) with the electrical parameters of the contacts, before and after isochronal 1 h heat treatments in vacuum up to 1000 °C.

II. EXPERIMENT

A. Sample preparation

The 4H–SiC wafer (CREE Research, Inc.) used in this work was *n* type, 280 μm thick, with a 10-μm-thick *n*-type epilayer grown on its Si face. The substrate and the epilayer were doped with nitrogen to levels of 7.3×10^{17} and $1\times10^{16}/\mathrm{cm}^3$, respectively. Prior to deposition, the samples were degreased in organic solvents in an ultrasonic bath (trichlorethylene, acetone, and methanol, sequentially). Immediately prior to deposition, the samples were etched in an aqueous solution of 10% HF for 10 s and then blown dry with N_2 gas.

The 50-nm-thick Pt films were deposited by electron beam thermal evaporation in vacuum. The substrate holder was neither cooled nor heated externally. The evaporation system is equipped with a cryopump and a cryogenic baffle that yields a background pressure of 1×10^{-8} Torr prior to the deposition. Diodes with area of 0.0005 cm^2 were defined by photolithography and liftoff. Post-deposition heat treatments were done in an evacuated tube furnace (5×10^{-7} Torr).

B. Sample characterization

The current–voltage ($I-V$) characteristics, were measured at room temperature with an HP 4140B picoampermeter/dc voltage source. An indium–gallium alloy was used as a back contact. The saturation current density, J_s, and the ideality factor, *n*, were obtained by least square fit of the linear part of the semilogarithmic $I-V$ curves. With the saturation current density thus established, and assuming the thermionic emission model, the barrier height was calculated from the equation:[4]

$$\Phi_B=\frac{kT}{q}\ln\left(\frac{A^{**}T^2}{J_s}\right),$$

where $A^{**}=142\ \mathrm{A/cm^2\,K^2}$ is the effective Richardson constant for 4H–SiC.[5] The Schottky barrier height and the ideality factor of 30 individual diodes were extracted from $I-V$ measurements before and after thermal annealing. The annealing of the diode sample was accumulative, i.e., the same diodes were annealed at several steps and their $I-V$ characteristics measured after each step. The annealing steps were 1 h long at 200, 400, 500, 600, 700, 800, 900, and 1000 °C.

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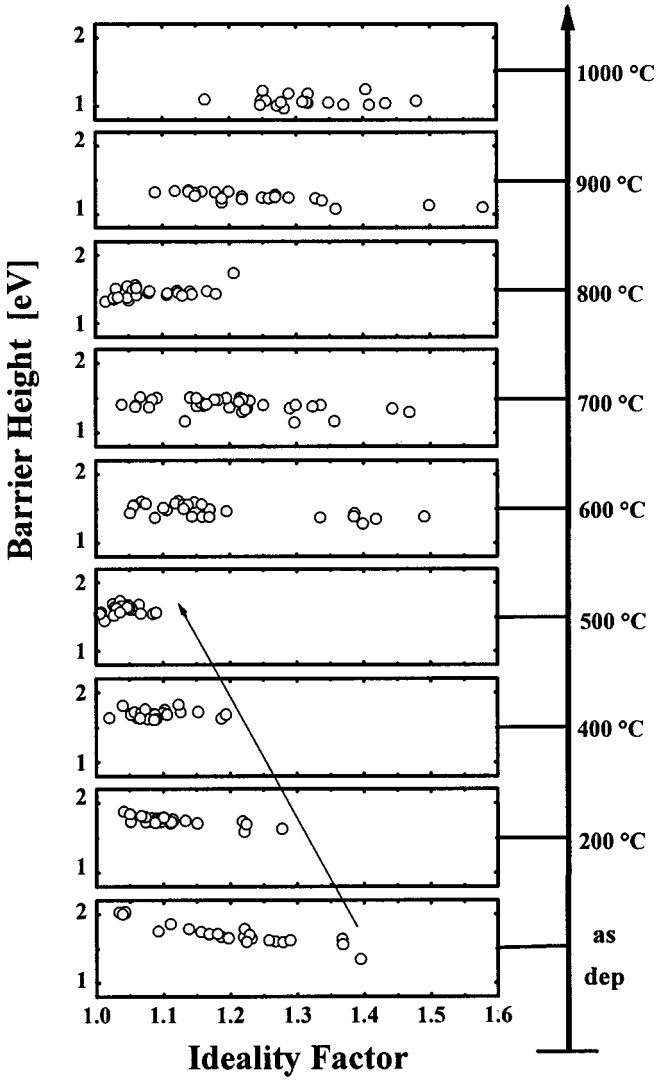

FIG. 1. Schottky barrier height obtained from $I-V$ measurements of 30 ⟨4H–SiC⟩\Pt(50 nm) diodes presented as a function of their ideality factor for various 1 h accumulated annealing steps.

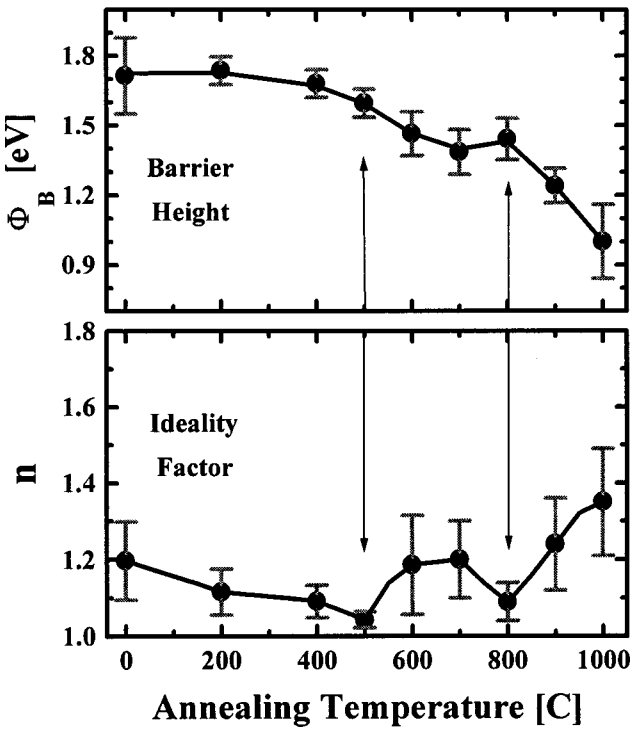

FIG. 2. $I-V$ mean Schottky barrier height and mean ideality factor as a function of the annealing temperature (the annealing steps are accumulated). The error bars are the standard deviation.

Nonpatterned samples were characterized by XPS to determine compositional profiles and to monitor interactions in the samples. XPS measurements were carried out in ultrahigh vacuum (3×10^{-10} Torr) using a 5600 Multitechnique System (PHI, USA) with spherical capacitance analyzer and monochromatized Al $K\alpha$ radiation ($h\nu=1486.6$ eV) source at a pass energy of 117 eV and an energy interval of 0.125 eV/step. Photoelectron spectra were acquired over a 400-μm-diameter spot. The C($1s$) peak position at the surface before the sputtering at 284.8 eV was used as an energy reference throughout this work.

III. RESULTS

Figure 1 shows the Schottky barrier height of each of the characterized diodes as a function of their ideality factor. Separate graphs are given for as-deposited diodes and for diodes annealed at 200, 400, 500, 600, 700, 800, 900, and 1000 °C for 1 h. As-deposited, the diodes show various barrier heights and the corresponding ideality factors are spread over a wide range up to a value of ~1.4. The results for the various diodes are well described by a linear curve of the form $\Phi_B=a\,n+b$, where Φ_B is the barrier height, n is the ideality factor while a and b are the slope and bias of the line, respectively. For the as-deposited diodes this fitting yields $a=-1.46\pm0.14$ and $b=3.46\pm0.17$ eV.

Annealing of the same diodes at 200, 400, and 500 °C results in consecutive narrowing of the ideality factor range, until at 500 °C the range is 1.05 ± 0.05. Further annealing at 600 and 700 °C increases the ideality factor range, which narrows again only after annealing at 800 °C. After annealing at higher temperatures the ideality factors increase in both their average value and their spread.

In Fig. 2, the average values of the Schottky barrier height [Fig. 2(a)] and the ideality factors [Fig. 2(b)] are given as a function of the annealing temperature. Arrows pointing at the 500 and 800 °C data points mark the two minima of the average ideality factors measured. The magnitude of the error bars is the standard deviation. The general trend of the barrier height is to decrease with temperature, with a local maximum at 800 °C. The average ideality factor first decreases up to 500 °C, after which it increases again with a local minimum at 800 °C.

After the annealing at 1000 °C, the diodes lost their metallic shine. Examining the samples with an optical microscope revealed a nonuniform surface with what seemed to be solidified droplets.

To gain a better understanding of the changes in the electrical parameters we applied XPS to samples that had been deposited and treated concurrently with the diode

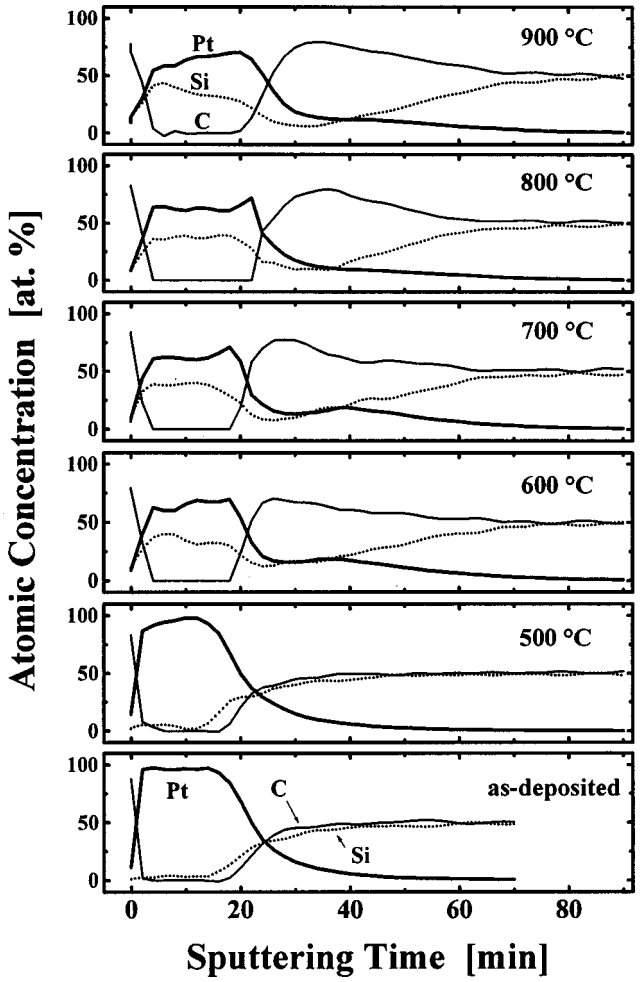

FIG. 3. Atomic concentration x-ray photoelectron spectroscopy depth profiles of ⟨4H–SiC⟩\Pt(50 nm) after 1 h annealing at various temperatures.

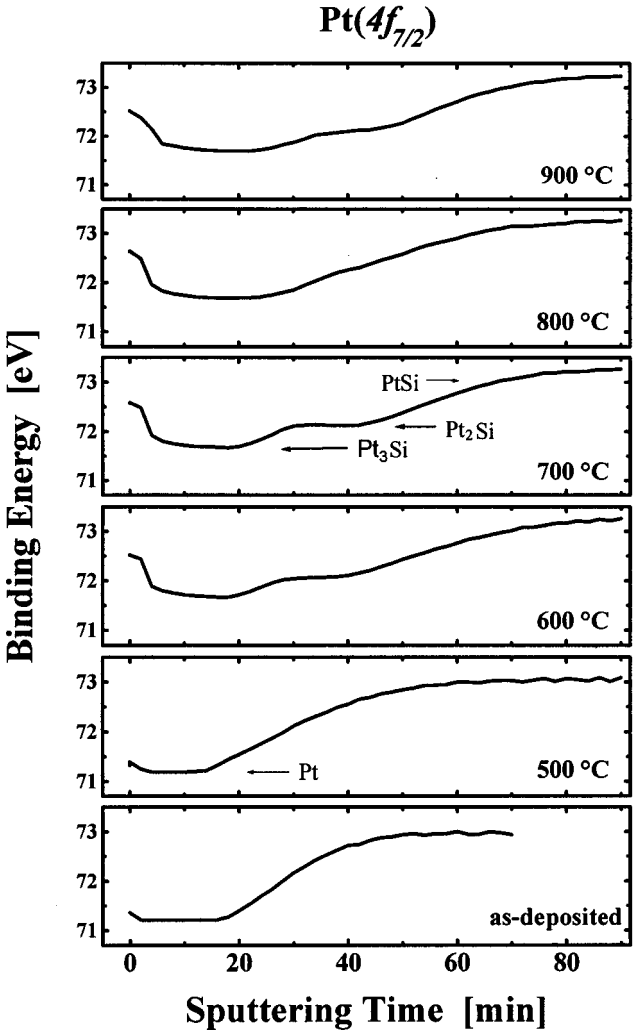

FIG. 4. Pt($4f_{7/2}$) binding energy x-ray photoelectron spectroscopy depth profiles of ⟨4H–SiC⟩\Pt(50 nm) after 1 h annealing at various temperatures.

samples. Figure 3 presents XPS depth profiles of Si($2p$) (dotted curve), C($1s$) (thin solid curve), and Pt($4f$) (thick solid curve) as a function of the sputtering time for as-deposited samples and for samples annealed at 500, 600, 700, and 900 °C. O($1s$) profiles were obtained for all the samples but were omitted in Fig. 3 for being mostly lower than the sensitivity limit of the method.

Only slight changes are observed between the depth profiles of the as-deposited sample and the one annealed at 500 °C, while a major reaction is observed after annealing at 600 °C. The reaction is manifested in pileup of carbon just below the original interface and diffusion of both Si outward into the original Pt layer and of Pt from the top layer past the original interface inward towards the substrate. No major differences are observed in this reaction picture up to 900 °C, although the interfaces seem to move slightly inward into the substrate as the temperature increases. The atomic concentrations suggest the formation of Pt-rich silicide phase above the original interface and a Si-rich phase or phases below it in the SiC–Pt reaction.

To further investigate the formation of silicide phases, the depth profiles of the Pt($4f_{7/2}$) binding energy are plotted for the various temperatures (Fig. 4). In the profile of the as-deposited sample, the Pt($4f_{7/2}$) peak is centered at a value that fits the reported binding energy of pure Pt (71.2 eV),[6] in the depth range that matches the Pt layer. Below the Pt layer, this value gradually shifts to a value that fits reported values of the PtSi phase (73 eV).[7] Deep Pt penetration may be caused by a knock-in effect during the sputtering process: Pt atoms knocked deep into the substrate by the sputtering atoms. The Pt atoms are later detected at the depth of the substrate, at which range the only possible silicide phase is the most Si-rich, PtSi.

Starting at 600 °C, the Pt($4f$) depth profile assumes a three-step form, after about 5 min of sputtering. The first step lies at ~71.7 eV, which is between the binding energy range reported for Pt (71.2 eV) and that reported for Pt_2Si (72.5 eV),[7] and is therefore highly likely to represent Pt_3Si. However, Pt_3Si is not formed in the Pt–Si reaction and therefore there are no reports of its binding energy in the literature. The next step appears at the inner side of the original interface and is close to the binding energy of Pt_2Si. After the second step, the curve gradually deviates until it reaches a binding energy value, which is around the value of PtSi. Roughly the same image is observed at temperatures higher than 600 °C. Hence, the change of trend observed in the ide-

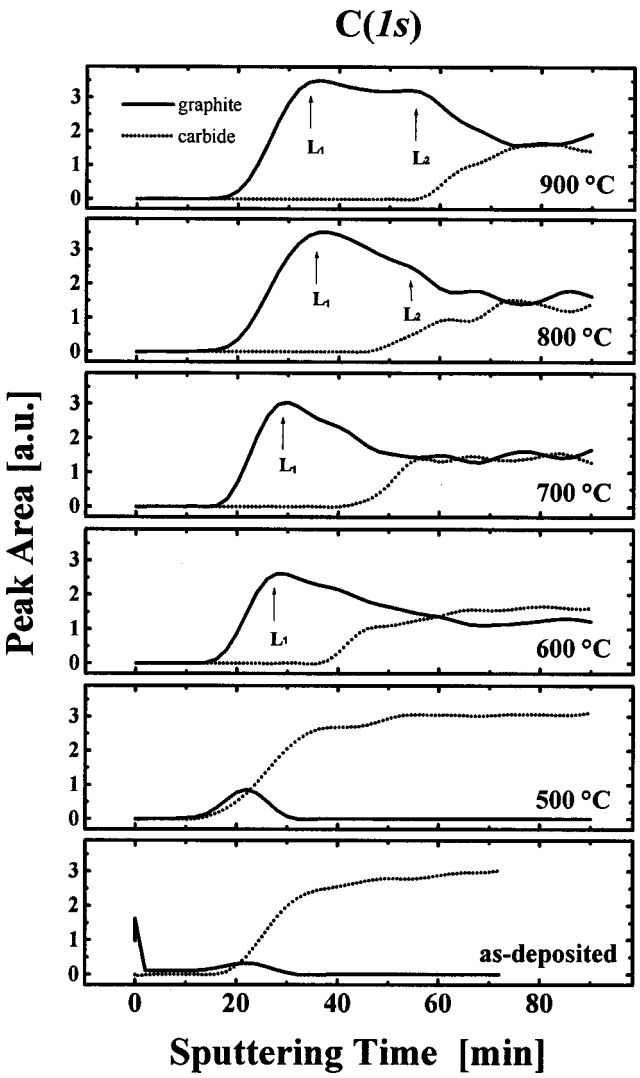

FIG. 5. X-ray photoelectron spectroscopy depth profiles of the graphite and the carbide ingredients of the C($1s$) peak of ⟨4H–SiC⟩\Pt(50 nm) after 1 h annealing at various temperatures.

ality factor values between 500 and 600 °C clearly correlates the onset of the Pt–SiC reaction. However, these results do not offer any clue to account for the significant changes in the electrical parameters at 800 °C.

The differences in the binding energy of Si($2p$) between the various possible silicides are too small to be analyzed here. We now turn to the C($1s$) binding energy profile. Using Gaussian fitting, the C($1s$) peak was decomposed to a carbide (~283.6 eV)[8] and graphite (~284.6 eV).[6] The peak area depth profile for each of these components was plotted for the various annealing temperatures (Fig. 5). In the as-deposited sample, a small peak of graphite is observed around the metal–semiconductor interface, while most of the carbon in the sample assumes the binding energy of carbide correlating the depth of the substrate. This image is not much altered after annealing at 500 °C. After annealing at 600 °C, a peak of graphite (marked L_1) is observed just below the original metal–semiconductor interface, while the carbide signal starts after about 30 min of sputtering deeper as compared to the 500 °C profile. Annealing at 700 °C mainly deepens the carbide signal. However, after annealing at 800 °C, a second graphite peak (marked L_2) evolves and is made distinct after annealing at 900 °C.

IV. DISCUSSION

Since the advent of laterally resolved methods for the evaluation of Schottky barrier heights (e.g., ballistic electron emission microscopy),[9] it has been established that the most practical metal–semiconductor contacts possess some degree of lateral nonuniformity. The effect of a nonuniform contact composed of patches with different Schottky barrier heights was theoretically established by Tung.[10] His model easily accounts for barrier height and ideality factor variations. Based on Tung's model, Schmitsdorf *et al.*[11,12] have shown experimentally and explained theoretically the existence of linear relations between effective barrier heights and ideality factors in ensembles of identically prepared diodes.

The diodes prepared for this study possess a range of barrier heights and ideality factors whose relation is well described by a linear curve (Fig. 1). According to the above-mentioned model, it may be explained as a manifestation of a nonuniform contact. In the case of our as-deposited diodes, this nonuniformity may be accounted for by the well-known shortcomings of the cleaning process. In Si technology, the dependence on surface preparation has been overcome by employing a solid–state reaction between a transition metal and the Si substrate. The silicide thus formed has a new interface with the substrate that is formed *in situ* and away from the original interface. Annealing of our ⟨4H–SiC⟩\Pt diodes indeed results in an improvement. The distributions of barrier heights and ideality factors seem to be narrowed as the annealing temperature is raised. This trend continues up to 500 °C. However, a detectable reaction between Pt and the SiC substrate is observed only after annealing at 600 °C. Therefore, it seems more likely that minor thermally induced interfacial atomic rearrangements occurring at temperatures below the onset of Pt–SiC reaction, are responsible for the observed improvement of the contact ideality. Such rearrangements may be too small to be observed by XPS depth profiling while sufficient to affect the transport at the metal–semiconductor interface.

Annealing at 600 °C initiates a reaction between the Pt and the SiC substrate, as clearly observed in the depth profiles. The reaction of Pt with Si is known to commence in a laterally nonuniform manner.[13,14] The same was also observed using transmission electron microscopy in the 3C–SiC–Pt system.[15] The irregularity of the contact is further indicated by the formation of a multiphase contact in the case of SiC, containing both silicides and carbon. It is therefore reasonable to expect the same for the 4H–SiC–Pt system. According to Tung, if the contact becomes laterally nonuniform, the ideality factor should increase. An increase is indeed observed starting at 600 °C (Figs. 1 and 2) and this general trend continues further at higher temperatures. However, at 800 °C a local deviation from this trend is observed in the form of a local minimum in the ideality factor, accompanied by a local maximum of the Schottky barrier height.

Figure 4 suggests that annealing at temperatures between 600 and 900 °C produces a sequence of the three congruent

phases of Pt and Si:Pt_3Si, Pt_2Si, and PtSi. This is indicated by the three binding-energy steps in the Pt depth profile. However, the PtSi appears to be formed in a depth that is within the SiC substrate, while similar such transition of the binding energy is also observed at the as-deposited and 500 °C annealed samples, where clearly no reaction has taken place. It is therefore not clear whether this last step represents an artifact, or whether a thin layer of PtSi was indeed formed and its profile is only smeared.

The formation of Pt_3Si in Pt–SiC reaction is well known,[15,16] in contrast to its absence in the Pt–Si reaction. The difference between the systems is the presence of C in the Pt–SiC system. Indeed, presence of C is known to favor the formation of metal rich silicides, even in the case of refractory metals, where in the absence of C only disilicides are formed.[17,18]

The local improvement of the Schottky barrier observed at 800 °C does not correlate with any significant change in the atomic concentration depth profiles of Fig. 3 or the Pt binding energy depth profiles of Fig. 4. It does, however, correlate the onset of a second graphite peak in the carbon ingredient profiles of Fig. 5. Alternating layers of graphite and silicides have been observed in diffusion couples of SiC and Pt.[16] When thin films of metal are used, typically one layer of carbon is formed.[19,20] This pileup of carbon is a common observation in reactions of SiC and near-noble metals, since thermodynamically, these metals are not expected to form carbides.[21] Rijnders *et al.* suggested that carbon piles up at the interface with the substrate, and that the carbon layer thus formed experiences opposing stresses on each of its sides due to vacancy flux. The stresses are built up until at a certain stress a crack appears, the carbon layer is separated from the substrate, and a new layer starts to form.[16] Thus, it may be that adjacent to the separation of a new carbon layer, the contact is less irregular than before. A separation of a second carbon layer seems to have taken place after annealing at 800 °C and therefore may account for the observed local improvement of the electrical parameters. The actual microstructure of the contact and its correlation to the electrical characteristics remain a subject for further investigation.

V. CONCLUSION

The reaction of a 50-nm-thick Pt layer with 4H–SiC substrate is shown to set between 500 and 600 °C. The reaction creates a thin graphite layer interposed between a Pt_3Si top layer and a Pt_2Si mixed with graphite, contacting the substrate either directly or through a thin layer of PtSi. Annealing of the contact below that temperature is shown to improve the ideality of the Schottky contact and to decrease the variance of the Schottky characteristics among identically prepared diodes. This improvement is attributed to minor interfacial atomic rearrangements at the interface. Annealing at temperatures above the reaction onset temperature reverses this trend, degrades the ideality, and increases the variance between the diodes. This is attributed to the well-known laterally nonuniform manner of the Pt–SiC reaction. At 800 °C a local deviation from the general trend is observed. This deviation is shown to correlate the separation of a second graphite layer from the substrate. Although the depth profiles do not seem to change significantly between 600 and 900 °C, the interface with substrate is seen to continuously deepen and the Schottky characteristics to continuously change, which means that the ⟨4H–SiC⟩ Pt(50 nm) system does not reach thermodynamic equilibrium up to 1 h annealing at 900 °C. Annealing at 1000 °C results in a liquidation of the contact, probably due to the PtSi–Pt_2Si eutectics at 970 °C. This eutectic point sets a limit to the annealing temperature range. Therefore, to reach thermodynamic equilibrium, if at all possible, would require a much thinner Pt layer.

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